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DOTTORATO DI RICERCA IN FISICA - XXXV CICLO

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DEFECT CHARACTERIZATION AND RELIABILITY EFFECT ON 4H-SIC POWERMOSFET

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SUMMARY

INTRODUCTION

The semiconductor chip shortages took hold in 2020, largely due to significant swings in demand caused by the COVID-19 pandemic as far back as Spring 2020 [1]. Some customers reduced production and chip purchases as the virus spread across the globe. In addition, several countries and regions went into lockdown in early 2020, which significantly interrupted semiconductor supply. Chipmakers, meanwhile, saw surging demand for semiconductors in other sectors used to enable remote healthcare, work-at-home, and virtual learning, which were needed during the pandemic. The shortage continues to affect a range of downstream sectors, including cars, consumer electronics, home appliances, industrial robotics, and many other key goods. The semiconductor industry has worked diligently to ramp up production to meet renewed demand during the shortage. First, the semiconductor industry worked hard to keep operations running globally, especially during the start of the pandemic in Spring 2020 when many foreign and state governments-imposed lockdown orders on businesses. Some anti-COVID measures adopted at the beginning of the pandemic - such as lockdowns and restrictions on circulation - have led to a drastic drop in air pollution with consequent benefits also for health. This is the evidence of an international study on air quality trends in 47 European cities, including Rome, Milan, Paris, London and Barcelona, published in Nature and carried out by numerous research institutions, including ENEA [2]. This has led to new attention on the importance of reducing man-made pollution. At present, climate change represents a threat not only to specific regions around the world but to the entire world ecosystem. Therefore, there is an urgent need to deal with this situation and numerous initiatives have been developed to help in the cutting emissions mission [3]. Renewable energies (REs) have a crucial role in helping the world meet its future energy needs. As part of the European Green Deal, the European Commission proposed in September 2020 to raise the 2030 greenhouse gas emission reduction objective, including emissions and removals, to at least 55% compared to 1990. This objective should be achieved by means of the following key targets: at least 40% cuts in greenhouse gas emissions (from 1990 levels), 32% share for renewable energy and 32.5% improvement in energy efficiency [4]. To achieve the 2030 targets for RE it is necessary to maintain the current growth levels. On the other

hand, energy efficiency requires an inverse correlation with the RE need to achieve these targets. If energy efficiency is increased in 5%, the final requirement for the installation of RE will decrease in 7.5% approximately to achieve the same RE goal [5]. Thus, efforts to reduce greenhouse gas emissions made in both ways, RE share and energy efficiency, are equally valuable.

Besides, cutting greenhouse emissions could be achieved by substituting fossil fuel power plants by RE power plants or by means of using RE sources to provide energy to other applications such as heating and transport, leading to a great growth of the energy sector electrification. In this regard it is expected that the current renewable energy gather efficiency of 40% will transition to approximately 60% efficiency by 2040. Thus, the semiconductor industry will have to adapt to meet the exponentially these growing needs.

In this scenario Silicon (Si), which over the last four decades has been adopted in power electronics as the mainstream technology, continues dominating market and today, silicon power transistors and diodes are so widespread and pervasive that equipment based on this material is closely intertwined with our everyday lives. This adoption has allowed silicon to enjoy continuous technology and process improvements, supported by innovative packaging and interconnect technologies, that have enhanced thermal management and reduced parasitic effects for higher frequency operation. By virtue of this unrelenting quest for improvement, silicon technology is about to reach a plateau. Then power electronics design has taken an interesting turn toward the adoption of wide-bandgap (WBG) devices such as gallium nitride (GaN) and silicon carbide (SiC) which will soon direct technology toward new, more efficient power solutions. Yole Développement, a group of companies providing marketing, technology and strategy consulting, estimates that revenue from SiC devices will account for more than 10% of the market by 2025, while revenue from GaN devices will claim more than 2% of the market by 2025. As a key supplier of power solutions, STMicroelectronics has heightened efforts to complement its offer with wide bandgap materials such as SiC and GaN. The two technologies owe their appeal essentially to their capability to operate at higher voltages without compromising their on-state performance. They can handle far higher temperatures more safely and can work at higher frequencies. Their physical and electrical characteristics make it possible to reach unrivalled levels of miniaturization, reliability and power density. Environmental concerns so widely debated in the media and under the

spotlight to drive governments' policies over our energy future, can therefore be addressed by a large-scale rollout of the new compound semiconductors. To better understand the potential performance benefits, the following table summarizes the main properties of silicon vs. SiC (4H polytype) and GaN.

Property	GaN	4H-SiC	Si
Energy Band Gap $[eV]$	3.40	3.26	1.10
Electron Affinity $[eV]$	1.84	3.70	4.05
Thermal Conductivity $[W/cm-K]$	1.3 - 3.0	3.0 - 4.0	1.50
Intrinsic Carrier Concentration $[cm^{-3}]$	10^{-9}	10^{-7}	10^{10}
Satured Electron Drift Velocity $[10^7 cm/s]$	2.5	2.0	1.0
Breakdown Field $[MV/cm]$ @ $N = 10^{17}\ cm^{-3}$	3.0	$\|\| 3.20 \perp 1.00$	0.30
Electron Mobility $[cm^2/Vs]$	990-2000	800	1200
Relative Dielectric Constant	9.0	10.00	11.90

TABLE 1. COMPARISON BETWEEN MATERIAL PROPERTIES.

The employment of SiC MOSFETs and JBS diodes provide superior dynamic performance compared with Si IGBTs and PIN diodes; therefore, they can clearly improve power efficiency and power density. In fact, cost issues for SiC devices should be looked at from two aspects [6]. First, the cost of SiC MOSFETs decreases with volume production [7]. With larger volumes, better manufacturing processes with larger wafers, and improved device performance, the cost per amp of SiC devices will drop. Second, it is known that the absolute cost of SiC devices is higher than the cost of Si devices because of intrinsic higher material costs. However, the per-watt cost of the overall system could potentially be reduced with a better balance-of-plant system design. The savings may come from developments such as a smaller passive component, lower cooling requirements, and a higher absolute power rating. It is demonstrated in [8] that the cost of a 17 kW solar inverter could be reduced by 20% with SiC JFETs and SiC diodes. Additionally, the operational cost reduction gained from efficiency

improvements could justify the higher capital cost. Nowadays SiC devices are already used in wide variety of different applications:

A. *SiC Solar Inverter*
B. *Uninterrupted Power Supply*
C. *Railway Traction Inverter*
D. *Electric Vehicle*
E. *Induction Heating*
F. *High-Voltage SiC Device Applications*

In many of the afore mentioned applications the *reliability* and *availability* of power devices play a key role:

RELIABILITY

It is the probability that one article performs a required function under the conditions indicated for a certain period of time. The "required function" must include a definition of satisfactory operation and unsatisfactory or faulty operation. For an IC, the requested function is generally defined by a test program. The program output simply states "good" or "bad". The "indicated time period" is the time during which satisfactory operation is required. This will vary depending on the use of the system. In some cases, the time can be relatively short, as in the case of an emergency transmitter on an aircraft. Often the period of use is preceded by a long period of disuse [9]. Other systems are in continuous use. For such continuous operating systems another concept is defined:

AVAILABILITY

It is the probability that one article works in case of need or the average fraction of time in which a system should be in an operational condition.

The field reliability of SiC devices must be demonstrated for various applications, and a voltage-derating design guideline needs to be established. This is very important for applications in which reliability is extremely critical, such as aviation systems [10]. On the one hand, a power conversion system with SiC device potentially provides a higher current rating than one with a Si device, which leads to a larger thermal jump due to a higher thermal conductivity On the other hand, the higher temperature operation of the SiC device indicates

more stringent requirement for the package materials, whose design can be guided by an in-depht study of deformation mechanisms and the relationship between temperature and failure mechanisms. In this framework, to improve reliability modeling and prediction, recently has been proposed a direct method to evaluate the mechanical stress due to the repetitive quick increasing of temperature during high current pulses cycling, that wears out the gate oxide layer, the metal and the bonding [11] [12] [13] [14].

Although SiC devices show promising advantages, many challenges exist from both the device and application perspectives. These guide future research and development trends.

While high switching frequencies could be reached by unipolar devices like Si-based metaloxide-semiconductor field-effect transistors (MOSFETs), they can only provide low rated voltage and current capabilities. WBG materials have demonstrated to be an attractive solution to Si limitations providing powerful characteristics as shown in figure 1.

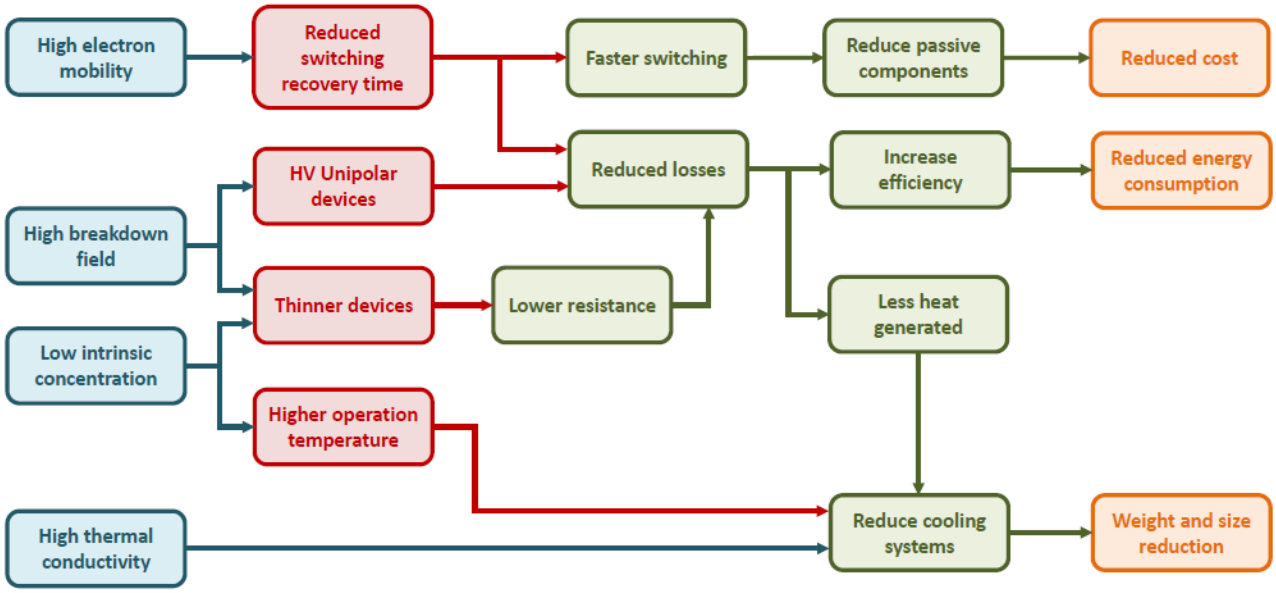

FIGURE 1. WBG SEMICONDUCTOR PARAMETER CAPABILITIES (BLUE); PHYSICAL PROPERTIES AFFECTED BY WBG ADVANTAGES (RED); POWER ELECTRONICS CHARACTERISTICS (GREEN); AND PRODUCT BENEFITS (ORANGE).

For instance, they offer a higher electric breakdown field that enable greater voltage blocking capability, thinner layers, and allows deeper doping concentration. Therefore, it results in lower conduction losses and a low drift resistance. Thus, an on-resistant reduction in comparison with Si-based devices. In accordance, same on-resistance WBG can have smaller area implying less capacitance. Likewise, less capacitance and a high saturation drift velocity allow higher switching speeds and lower losses per switching cycle [3] [15]. Additionally, the low intrinsic carrier concentration of WBG materials enables reduced leakage currents and robust high-temperature performance [16]. Figure 2 shows the Fermi energy level as a function of temperature for different concentrations of impurities.

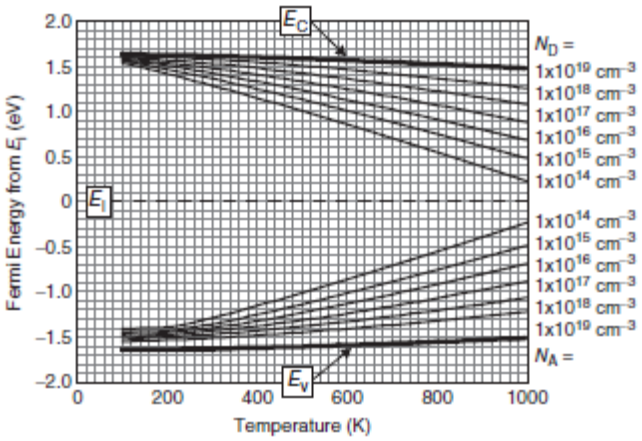

FIGURE 2. FERMI ENERGY LEVEL FOR NITROGEN- OR ALUMINIUM-DOPED 4H-SIC AS A FUNCTION OF TEMPERATURE AND IMPURITY CONCENTRATION. THE BANDGAP TAKES INTO ACCOUNT THE TEMPERATURE DEPENDENCE AND THE INCOMPLETE IONIZATION OF DOPANTS.

Let's see in detail advantages and disadvantages of using silicon carbide and gallium nitride rather than the common silicon.

ADVANTAGES

LESS ON-RESISTANCE

Let's consider a power VD-MOSFET device; in figure 3a is shown that for each layer can be defined an appropriate resistance whose sum constitute the on-resistance of drift:

$$\boldsymbol{R_{ON} = R_{CS} + R_{N+} + R_{CH} + R_A + R_{JFET} + R_D + R_{SUB} + R_{CD}}$$

EQUATION 1

For silicon carbide components this resistance, which depend on the working temperature (3b), is about 10 times lower than that one would have in silicon devices.

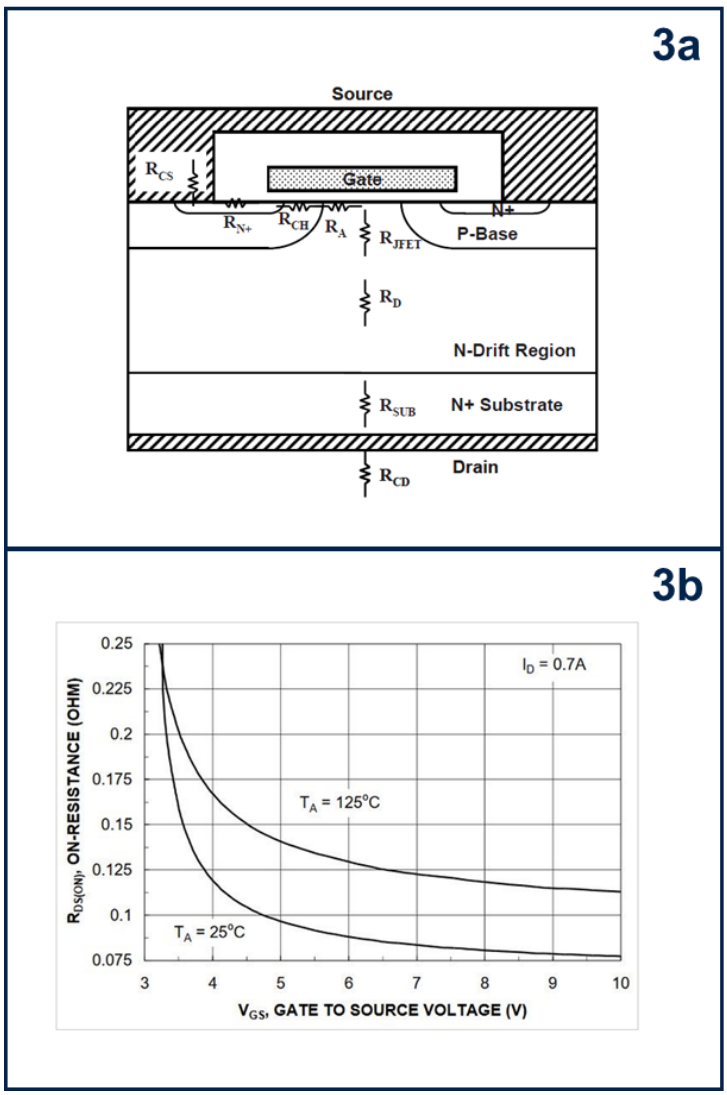

FIGURE 3. (A) POWER VD-MOSFET STRUCTURE WITH ITS INTERNAL RESISTANCES. (B) R_{ON} AS A FUNCTION OF V_{GS}.

INCREASED BREAKDOWN VOLTAGE

It is an effect is due to the greater width of the forbidden band comparing with the silicon one. The breakdown voltage is the voltage at which the current begins to flow between Source and Drain multiplying by an avalanche effect, while gate and source are short-circuited.

$$V_{TH} = \frac{t_{OX}}{\varepsilon_{OX}} \sqrt{4\varepsilon_S KTN_A ln\left(\frac{N_A}{n_i}\right)}$$

EQUATION 2

Increased Thermal Conductivity

The high thermal conductivity allows to better dissipate the heat and therefore makes the device suitable to manage higher current flows at lower temperatures.

Increased Reliability

Reliability is one of the main aspects to take into account in power electronics projects.

Excellent Recovery Behavior

A higher saturation drift speed is equivalent to a faster removal of the charges in the area of space charge, this results in a shorter recovery time and a more contained reverse recovery current.

High-Level Performances At High Frequencies

The ability of a semiconductor to switch to high frequency is directly proportional to its saturation drift speed. The drift velocity of silicon carbide is about twice that of silicon, see table 2. It follows that WBG-based devices can operate with excellent performance at higher frequencies.

Properties	Si	4H-SiC	GaAs	GaN
Crystal Structure	Diamond	Hexagonal	Zincblende	Hexagonal
Energy Gap : E_G (eV)	1.12	3.26	1.43	3.5
Electron Mobility : μ_n (cm^2/Vs)	1400	900	8500	1250
Hole Mobility : μ_p (cm^2/Vs)	600	100	400	200
Breakdown Field : E_B (V/cm) X10^6	0.3	3	0.4	3
Thermal Conductivity (W/cm°C)	1.5	4.9	0.5	1.3
Saturation Drift Velocity : v_s (cm/s) X10^7	1	2.7	2	2.7
Relative Dielectric Constamt : ε_S	11.8	9.7	12.8	9.5
p, n Control	○	○	○	△
Thermal Oxide	○	○	×	×

TABLE 2. COMPARISON OF SOME PHYSICAL PROPERTIES AMONG THE PRINCIPAL MATERIALS OF ELECTRONIC DEVICES [17].

Disadvantages

- *Defects and dislocations in SiC and difficulties in the industrial procedure for the manufacture of GaN.*

- *High costs.*
- *Relatively limited availability.*
- *No standard packaging technology for high temperatures SiC-devices* [18].

The GaN, came ofter the SiC, and it is not widely used because of the cost, yield and reliability issues [19]. Although GaN-based devices offer a very high switching speed, thanks to the considerable mobility of the electrons. Nevertheless, the lower thermal conductivity, the limited power density potential and the lack of robustness make their use still not preferable to the SiC based devices. Moreover, the reduced natural dissipation capability, fundamental characteristic for high power converters, makes these devices unsuitable unless fluid cooling procedures are used. This makes trickly their industrial production by requiring a more cumbersome and more expensive assembly. It seems clear that these devices, that must operate at high frequency and temperatures, require additional innovative design solutions to become effective from an industrial point of view.

SiC occurs in many (100) crystalline structures, named *polytipes*. Polytypes are made up of atoms with 50% carbon and 50% silicon. Within a SiC crystal the Si and C atoms form very strong tetrahedral covalent bonds (bond energy=4.6 eV) via sharing of electron pairs in sp^3 hybrid orbitals (figure 4).

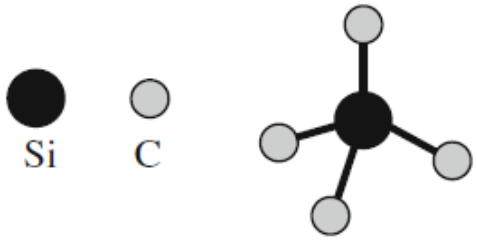

FIGURE 4. SKETCH OF TETRAHEDRAL COVALENT BONDS IN A SIC CRYSTAL

The polymorphism of SiC is characterized by different crystalline structures of the same chemical compound that are identical in two dimensions and differ in the third. Thus, they can be viewed as layers stacked in a certain sequence. Clearly, each polytype has distinct electronic structures and distinct electrical and optical properties.

The most common hexagonal polytypes are 2H-SiC, 4H-SiC and 6H-SiC.

The difference between these arises from the different SiC bilayer stacking sequences. Stacking sequences can be ABAB ..., ABCBABCB ... e ABCACBABCACB ... See figure 5.

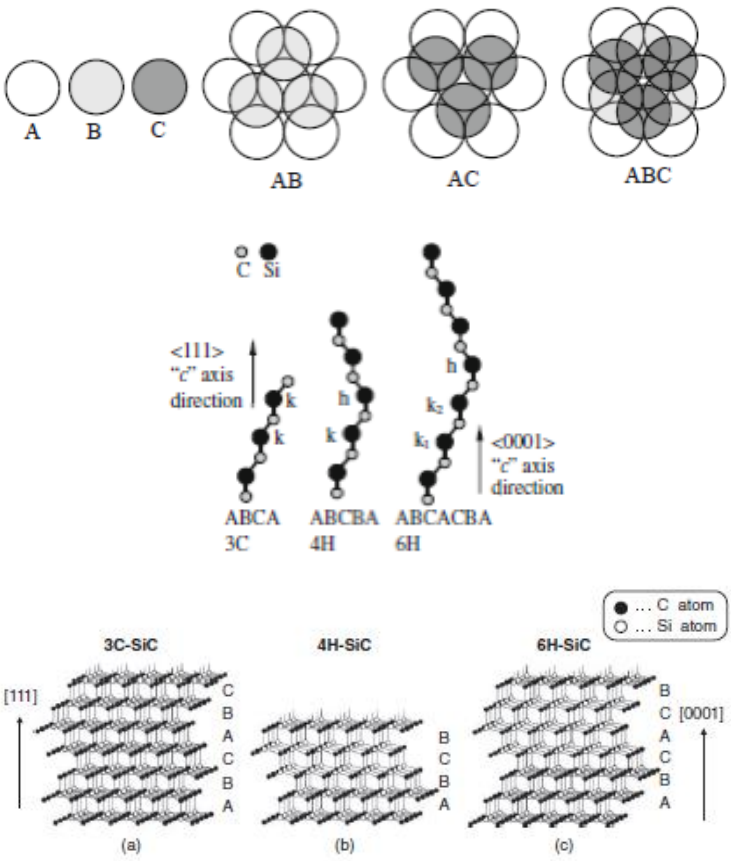

FIGURE 5. STACKING SEQUENCES.

The letter *H* refers to the hexagonal crystal structure, the number refers to the number of atomic bi- layers. Each atom, within a double layer, has 3 covalent chemical bonds.

The polytype used in electronics is the 4H-SiC.

The 4H-SiC stacking sequence is characterized by a unit that is repeated every 4 bilayers and, in each layer, the Si (or C) atoms have a hexagonal arrangement (figure 6).

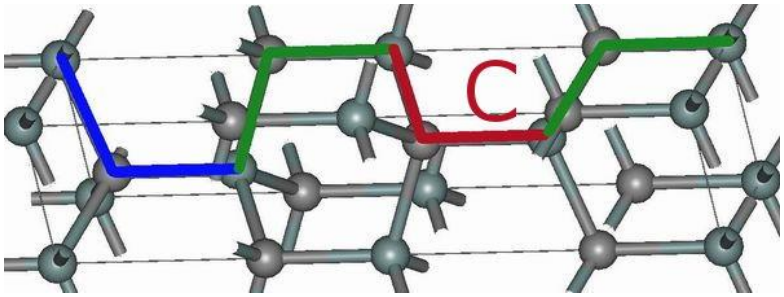

FIGURE 6. 4H-SIC STACKING SEQUENCE.

Its energy gap is *3.23 eV* and it is interesting to point out that the energy gap increases with increasing hexagonality. The energy bandgap, E_g, decreases with increasing temperature because of thermal expansion, and its temperature dependence can be semi-empirically expressed as:

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{T + \beta}$$

EQUATION 3

where E_{g0} is the bandgap at 0 K, T the absolute temperature, and α and β are fitting parameters.

The figure 7 shows the temperature dependence of the bandgap for several SiC polytypes.

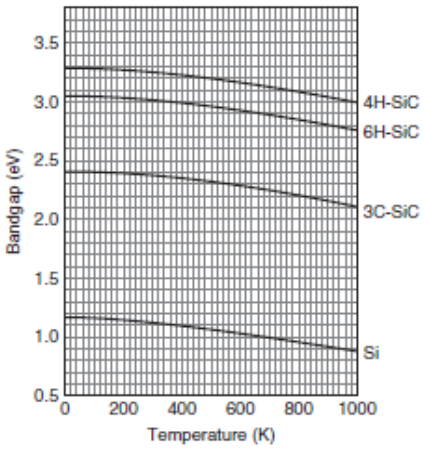

FIGURE 7. TEMPERATURE DEPENDENCE OF THE BANDGAP FOR DIFFERENT SIC POLYTYPES.

It is well known that the properties of a semiconductor mainly depend on the valence and conduction band and by their relative position.

The energy required to move one electron from the valence to the conduction band in a WBG semiconductors is greater than that which, for example, is required in Si. This greater energy request, in the case of WBG devices, leads to a higher breakdown voltage than the common Si based devices.

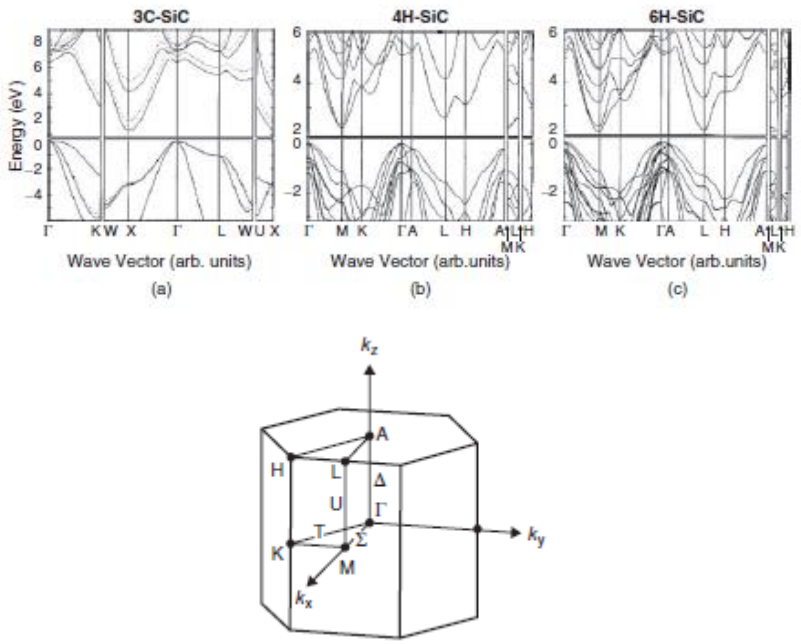

FIGURE 8. BAND STRUCTURE OF DIFFERENT POLYTYPES.

Another important consideration must be made: all the SiC polytypes have an *indirect band structure* (see figure 8), as is also the case for Si. The top of the valence band is located at the *Γ* point in the Brillouin zone, whereas the conduction band minima appear at the Brillouin zone boundary.

PHYSICAL PROPERTIES

Many and relevant are the physical properties of SiC but in this chapter, we focus on electric and thermal transport properties that have made this material a reference point in designing modern semiconductor devices.

MOBILITY

Mobility is defined as the modulus of the drift rate of a charge carrier per unit of electric field, it is defined positive both for the electrons and for the holes (even if their speed of drift, under the action of an electric field, is opposite).

In SiC the mobility of electrons is far greater than that which characterizes the holes and for this reason it is more convenient to realize the active regions of the components with a n-type doping rather than a p type.

Mobility decreases as the concentration of the doping species increases and this situation is essentially due to the increase in the scattering of charge carriers by the donor atoms or ionized acceptors. Similarly, this parameter decreases with increasing temperature due to the greater scattering of phonons.

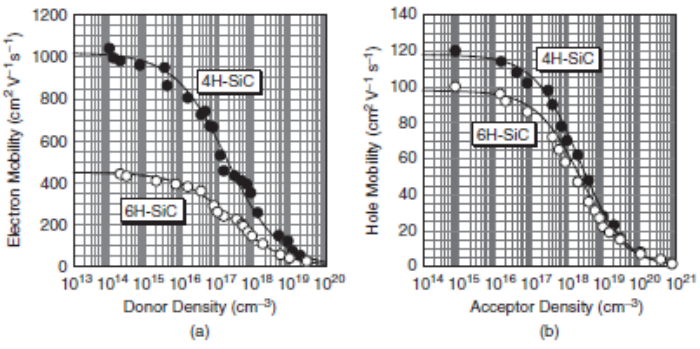

FIGURE 9. ELECTRON AND HOLE MOBILITY FOR TWO DIFFERENT POLYTYPES.

Figure 9 shows the low-field electrons mobility versus donor density (a), and the holes mobility versus acceptors density (b), for 4H-SiC and 6H-SiC at room temperature. The electrons mobility of 4H-SiC is almost double that of 6H-SiC at a given dopant density, and 4H-SiC exhibits a slightly higher holes mobility than 6H-SiC. The low-field mobility for electrons and holes can be expressed by Caughey–Thomas empirical equations as follows

$$\mu_h = \mu_{h,min} + \frac{\mu_{h,max} - \mu_{h,min}}{1 + \left(\frac{N_D + N_A}{N_{REF}}\right)^{\alpha}} \quad [cm^2 V^{-1} s^{-1}] \quad (h = n, p)$$

EQUATION 4

where $\mu_{h,max}, \mu_{h,min}, \alpha, N_{REF}$ are fitting parameters and N_D, N_A are the doping concentration of donors and acceptors.

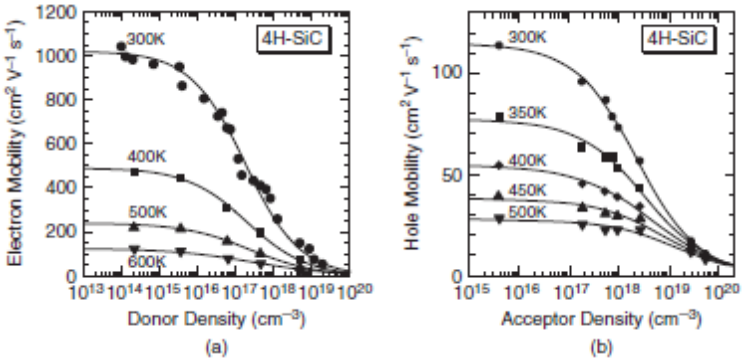

FIGURE 10. ELECTRON AND HOLE MOBILITY FOR 4H-SIC FOR DIFFERENT TEMPERATURES.

Figure 10 shows low-field electron mobility versus donor density (a), and hole mobility versus acceptor density (b), for 4H-SiC at different temperatures. At this stage is crucial to define also the coefficient of diffusion of the charges, which can be obtained using the *Einstein relation*:

$$D = \frac{kT}{q}\mu_h$$

EQUATION 5

Where *q* is the elementary charge and *T* is the absolute temperature.

At high temperature, the doping dependence of mobility becomes small, because the influence of impurity scattering decreases. In general, the temperature dependence of mobility is discussed by using a relationship of $\mu_h \sim T^n$, where the value *n* strongly depends on the doping density, since the dominant scattering mechanism varies for SiC with different doping density.

DRIFT VELOCITY

The drift of the carriers is proportional to the intensity of the electric field, when this is weak. But if the electric field is high the dependence is no more linear, because the accelerated carriers transfer more energy to the lattice causing the emission of more phonons. Drift velocity is expressed by:

$$v_d = \frac{\mu E}{\left\{1 + \left(\frac{\mu E}{v_s}\right)^{\gamma}\right\}^{1/\gamma}}$$

EQUATION 6

where, v_s is the sound velocity in a semiconductor and γ the parameter. In figure11 we can see the behaviour of v_d for two different polytypes as a function of electric field and for different temperatures. At sufficiently high electric fields, carriers start to interact with optical phonons, and finally the drift velocity becomes saturated:

$$v_{sat} = \sqrt{\frac{8\hbar\omega}{3\pi m^*}}$$

EQUATION 7

where $\hbar\omega$ is the energy of the optical phonon and m^* is the reduced electron mass.

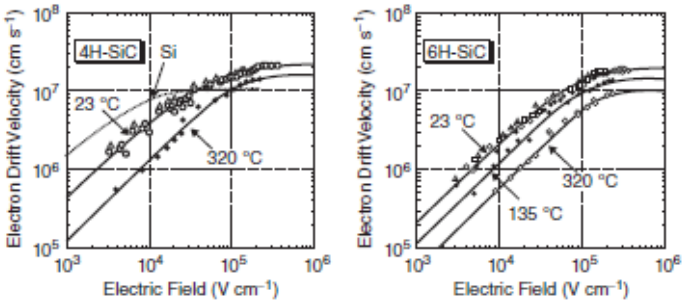

FIGURE 11. ELECTRON DRIFT VELOCITY VERSUS ELECTRIC FIELD STRENGTH AT DIFFERENT WORKING TEMPERATURES.

BREAKDOWN ELECTRIC FIELD STRENGTH

In reverse polarization, the current in a p-n junction (or a Schottky diode) tends to increase with the increasing of the applied electric field due to the presence of minority carriers thermally excited inside the depletion region. If the amplitude of the electric field is very high, the p-n junction eventually breaks. Failure mechanisms can be classified into:

AVALANCHE EFFECT (AVALANCHE BREAKDOWN)

Avalanche consists of a process of multiplication of the electric current under the effect of very intense electric fields. The charge carriers are accelerated from the field at very high speeds and during their run inside the material they hit against the atoms. If the field is sufficiently strong, therefore, the energy of the particles is sufficiently high to ionize the lattice atoms (impact ionization). At this point both the starting carriers and the carriers coming from the atom ionization will participate to the conduction process and will be accelerated, resulting in an avalanche if the field is sufficiently high. If the field is not sufficiently intense,

the speed of the carriers is not high enough to maintain the avalanche breakdown and the carriers are reabsorbed by the atoms. This effect is dominant when dealing with slightly doped junctions (small regions of depletion) [20] [21] [22].

ZENER EFFECT (TUNNELING)

It is an effect that occurs in p-n junctions, heavily doped, in reverse polarization. The applied electric field favors the tunnel effect of the semiconductor charge carriers: the electrons pass from a valence band to a conduction band. This generates a sudden increase in reverse current.

Although both effects concern the minority charge carriers, the two effects differ for the physical reasons that arise from them. The two effects can also occur simultaneously. The Zener breakdown is temperature-dependent, so it is particularly inversely proportional to T: as the temperature increases, the gap decreases, therefore the Tunneling barrier; for the same reasons we have the opposite reasoning for the avalanche effect [23].

The breakdown field can be expressed in terms of voltage applied as follows [24]:

$$V_B = \frac{E_{cr}^2}{2qN_d}\varepsilon_r\varepsilon_0$$

EQUATION 8

where N_d is the n-type doping, q is the electron charge, $\varepsilon = \varepsilon_r \varepsilon_0$ is the dielectric constant of the vacuum multiplied for the relative constant of the semiconductor used to realize the diode, E_{cr} is the critical field, that is the maximum value of the electric field applicable to a junction of a given material.

THERMAL CONDUCTIVITY

Figure 12 shows the temperature dependence of thermal conductivity for SiC and Si, with its significant contribution from phonons, has a much higher thermal conductivity than Si. It has been reported that the thermal conductivity is not sensitive to the SiC polytype but depends on the doping density and the crystal direction.

Silicon carbide has a high thermal conductivity. This is an advantage with regard to heat dissipation, as the thermal resistance is defined as:

$$R_{th-jc} = \frac{d}{\lambda A}$$

EQUATION 9

where λ is the thermal conductivity, d is the thickness of the device and A is the section. Therefore, the thermal resistance for the same thickness, is much lower than that of Silicon, and this allows a greater transfer of heat from the junction to the case, therefore towards the heat sinks, and finally towards the external environment.

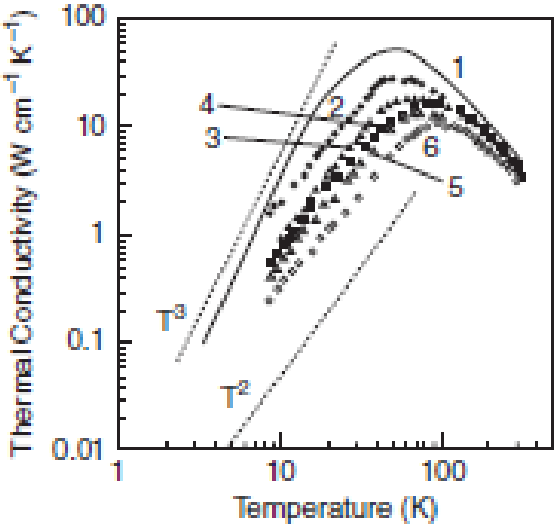

FIGURE 12. TEMPERATURE DEPENDENCE OF THERMAL CONDUCTIVITY FOR SIC AND SI.

INTRINSIC CONCENTRATION

One of the fundamental characteristics of SiC is the low intrinsic concentration of carriers, n_i, which is the result of the compensation of the two following effects:

GENERATION OF ELECTRON-HOLE PAIRS

The higher is the thermal energy supplied to the crystal, the higher is the electron leap process from the valence band to the conduction band due to electron hole pair generation

RECOMBINATION OF ELECTRON-HOLE PAIRS

The greater the number of conduction electrons and holes, the higher is the recombination probability.

The intrinsic concentration is linked to the width of the E_g bandgap through the relation:

$$n_i = \sqrt{N_c N_v} e^{-E_g/2kT}$$

EQUATION 10

where *k* is the Boltzmann constant, *T* is the temperature expressed in Kelvin, while N_c and N_v are the densities of the states respectively in the conduction band and in the valence band, which are calculated with the relations:

$$N_c = 2\left(\frac{2\pi kT m_n^*}{\hbar^2}\right)^{3/2}$$

EQUATION 11

$$N_v = 2\left(\frac{2\pi kT m_p^*}{\hbar^2}\right)^{3/2}$$

EQUATION 12

where $\hbar$ is the Planck constant, m_n * and m_p * are the mean values of the effective mass on the density of the states of electrons and holes, respectively.

The Varshni equation (equation 3) can be used to derive the energy gap for any semiconductor up to 800 K, provided that appropriate values of $E_g(0)$ are used for the specific structure considered [24].

The intrinsic concentration of carriers is highly temperature dependent and increases with the temperature.

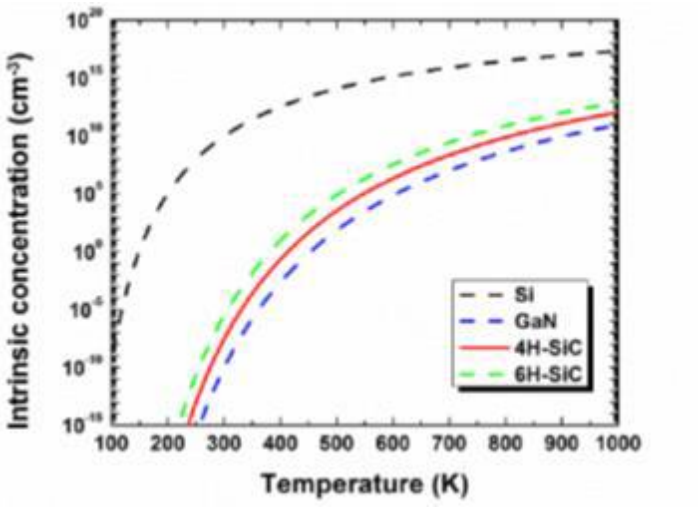

FIGURE 13. INTRINSIC CONCENTRATION TREND (CM^{-3}) VS THE TEMPERATURE (K) FOR SI, GAN, 4H-SIC AND 6H-SIC [25].

Increasing the density of intrinsic carriers with increasing temperature is one of the problems that limits the functionality of p-n junctions in high temperature silicon devices. Usually for commercial silicon-based devices, the temperature of 125°C is specified as the upper limit for correct operation. In fact, when the temperature increases from 25°C to 300°C, in silicon the density of intrinsic carriers increases from 10^{10} cm^{-3} to 10^{16} cm^{-3}, the latter value very similar to that of the density of the dopant. In these conditions, obviously most devices will not work properly.

However, at 300°C the intrinsic carrier density for 4H-SiC settles at only 10^{5} cm^{-3} and therefore the device can still properly work.

Thanks to its characteristics, SiC represents today the main protagonist on which are designed the power devices of our automotive. The basic device fundamental for very large-scale integration is the MOSFET, that we are going to briefly introduce in the following pages, starting from the MOS diode.

MOS Diode

The MOS diode is constituted by a metal-semiconductor junction. The metal layer forms the anode of the diode while the semiconductor is the cathode. The choice of the combination of the metal and the semiconductor determines the threshold voltage of the diode, the limit voltage that must be applied to the device so that it begins to conduct. As the concentration of dopants in the semiconductor increases, the width of the depletion region decreases. Below a certain width the charges can be tunnelled through the emptying area. The ideal MOS is characterized by:

Flat Energy Bands at $\Delta \mathbf{V} = \mathbf{0}$

In the absence of polarization, the energy difference between the extraction work of the metal $q\varphi_m$ and the semiconductor extraction work $q\varphi_s$ is zero, i.e. for a p-type semiconductor the difference of the extraction works is null

$$q\varphi_{m,s} = (q\varphi_m - q\varphi_s) = q\varphi_m - \left(q\chi + \frac{E_g}{2} + q\varphi_B\right) = 0$$

EQUATION 13

where $q\chi$ is the electron affinity of the semiconductor and $q\varphi_B$ is the energy difference between the Fermi level E_F and the intrinsic Fermi level E_i.

INFINITE RESISTIVITY OF OXIDE

When a continuous polarization is applied, there is no transport of charges through the oxide.

CARRIER CHARGES

For every polarization, the carrier charges are those in the semiconductor and those, with opposite sign, at the metal-oxide interface.

Figure 14 (a) and b shows a perspective view of a MOS diode. In figure 14 (c) we report the energy band diagram of an ideal p-type MOS diode when V=0.

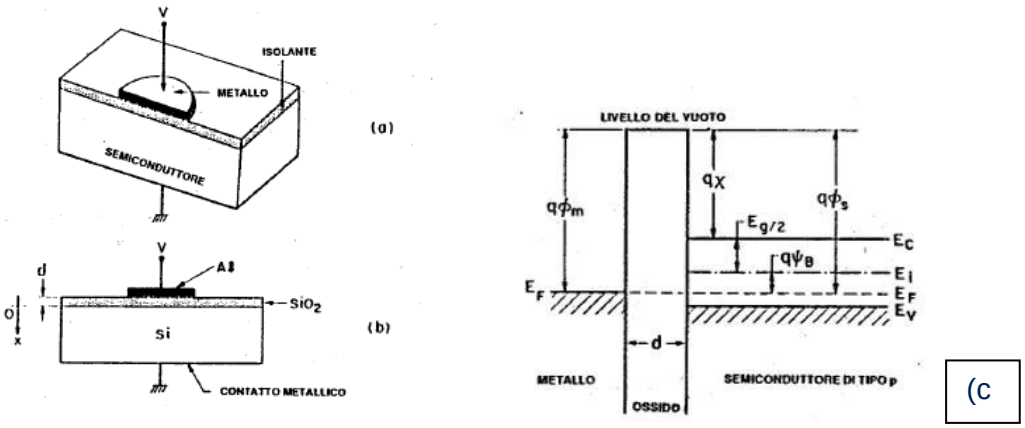

FIGURE 14. PERSPECTIVE (A) A LATERAL (B) VIEW OF MOS DIODE. IDEAL ENERGY BAND IN ABSENCE OF EXTERNAL POLARIZATION.

When an external polarization is applied to the diode, it can occur two different phenomena depending on the applied positive or negative voltage.

INVERSE POLARIZATION (V<0)

By applying a negative voltage to the metal electrode, the energy bands will tend to bend upward, close to the semiconductor surface: in the device there is no current passing, regardless of the applied voltage. This happens because the electric field generated by the battery has the same direction of the built-in field (voltage that is created at the edges of the depletion region) and this produces an enlargement of the depletion region [26]. The density of carriers in the semiconductor depends exponentially on the E_i-E_F energy difference, ie:

$$p_p = n_i e^{(E_i - E_F)/kT}$$

EQUATION 14

The upward curvature of the energy bands near the surface of the semiconductor produces an increase in the energy difference E_i-E_F, and consequently causes an increase in concentration, i.e. an accumulation of holes near to the oxide-semiconductor interface. This situation is called ***accumulation***, the corresponding charge distribution is shown on the right side of the figure 15.

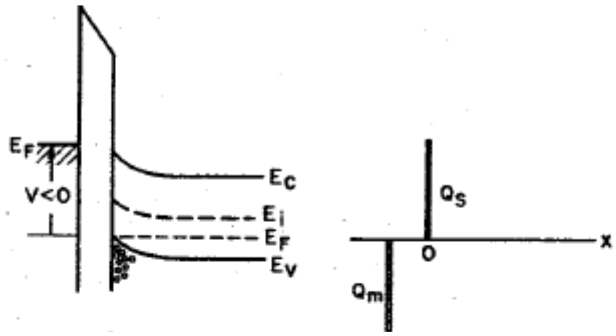

FIGURE 15. ENERGY BAND AND CHARGE DISTRIBUTION FOR V>0.

DIRECT POLARIZATION (V>0)

By applying a small positive voltage to the device, the energy bands will tend to bend downwards, and the emptying of the majority carriers (holes) occurs, leading to a ***depletion*** of the depletion region, as shown in the figure 16:

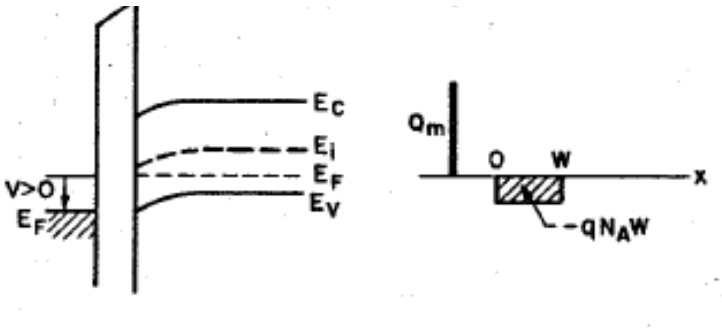

FIGURE 16. ENERGY BAND AND CHARGE DISTRIBUTION FOR V>0.

The space charge per unit area Q_{sc} in the semiconductor is formed by the charge in the depleted zone [26]:

$$Q_{sc} = -qN_A W$$

EQUATION 15

where *W* is the thickness of the surface depleted zone.

DIRECT POLARIZATION (V>>0)

If a higher positive voltage is applied, the energy bands undergo to further bending, see figure 17 and the intrinsic energy level E_i crosses the energy Fermi level E_F.

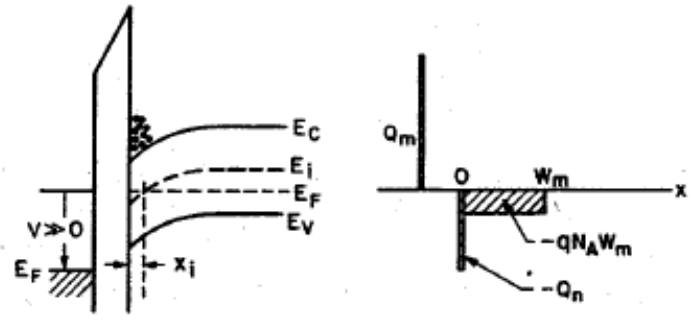

FIGURE 17. ENERGY BAND AND CHARGE DISTRIBUTION FOR V>>0.

The electron concentration depends exponentially on the energy difference E_F-E_i and is given by:

$$n_p = n_i e^{(E_F - E_i)/kT}$$

EQUATION 16

In the situation shown in the figure above (E_F-E_i)>0; hence, the concentration of the electrons near Fermi surface is greater than the holes concentration causing a further decrease in the holes number. The number of electrons (minority carriers) is greater than the number of holes (majority carriers): a *population inversion* has occurred. If the bands are further inflected, the conduction band limit ends up approaching the Fermi level, in which case the electron concentration near the surface increases very quickly [26]. In addition to this point, most of the additional negative charges in the semiconductor is constituted by the charge Q_n of the electrons of the narrow n-type inversion layer with thickness x_i. Typical values of x_i are between 10 Å and 100 Å, smaller than the thickness of the surface emptying layer.

Once an inversion layer has formed, the thickness of the surface emptying layer reaches a maximum value. This is due to the fact that when the bands are bent downwards sufficiently to produce a strong inversion, any further downward curvature, even if very small (such as to cause a very small increase in the thickness of the layer of inversion), causes a large increase in the Q_n charge of the inversion layer. Therefore, in conditions of strong inversion the charge per unit area is given by:

$$Q_s = Q_n + Q_{sc}$$

EQUATION 17

where:

$$Q_{sc} = -qN_A W_m$$

EQUATION 18

and W_m is the maximum thickness of the surface emptying region.

Figure 18 shows, in greater detail, the diagram of the energy bands at the surface of the semiconductor. The electrostatic potential φ is zero within the semiconductor. At the surface of the semiconductor, it is $\varphi=\varphi_s$ where φ_s is the surface potential.

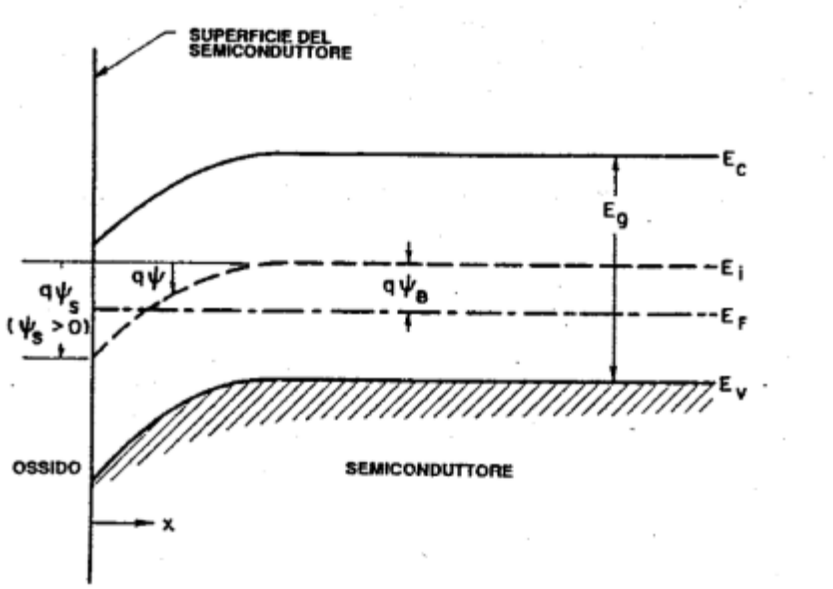

FIGURE 18. ENERGY BAND FOR V>>0.

The concentrations of electrons and hole can be expressed as:

$$n_p = n_i e^{q(\varphi-\varphi_B)/kT}$$

EQUATION 19

$$p_p = p_i e^{q(\varphi_B-\varphi)/kT}$$

EQUATION 20

where it is assumed that φ_s is positive when the band diagram has a downward curvature. Consequently on the surface the concentrations are:

$$n_s = n_i e^{q(\varphi_s-\varphi_B)/kT}$$

EQUATION 21

$$p_s = n_i e^{q(\varphi_B - \varphi_s)/kT}$$

EQUATION 22

Based on these equations, we can distinguish different situations regarding the surface potential:

- $\phi_s < 0 \rightarrow$ holes accumulation (bands curve upwards)
- $\phi_s = 0 \rightarrow$ flat band condition
- $\phi_B > \phi_s > 0 \rightarrow$ holes depletion (bands curve downwards)
- $\phi_s = \phi_B \rightarrow$ center of the forbidden band with $n_s=n_p=n_i$ (intrinsic concentration)
- $\phi_s > \phi \rightarrow$ population inversion (bands curve downwards)

It is possible to establish a criterion to fix the point of strong inversion. For this purpose, we define the concentration of the electrons at the surface equals the concentration of the impurities in the substrate

$$n_s = N_A$$

EQUATION 23

Since $N_A = n_i e^{q\phi B/k\mathrm{T}}$ we obtain:

$$\varphi_s(inv) \cong 2\varphi_B \frac{2kT}{q} ln \frac{N_A}{n_i}$$

EQUATION 24

Therefore, a potential equal to φ_B is needed to curve down the energy bands up to the intrinsic condition ($E_i=E_F$), then a further φ_B is necessary to obtain the strong inversion condition.

MOSFET

Silicon carbide MOSFETs are unipolar components capable of blocking a very high reverse voltage with a low drift resistance. It is a three-terminal device consisting of a p-type semiconductor substrate within which two regions of type n^+, source (source) and drain (collector) are formed. The metallic contact on the oxide is called gate (gate). Polysilicon and strongly doped polycrystalline silicon can also be used as a gate electrode. Moreover, having a wider band gap, in silicon carbide there is a concentration of charge carriers much lower than silicon and a specific on-resistance equal to 1% of that of silicon; this contributes to having a lower leakage current at higher temperatures. These devices also have no residual current after switching off and the recovery time is extremely short. They therefore allow more efficient operation at high frequencies and a reduction in size and volume with consequent reduction in material costs. The main issue of the SiC MOSFET is the creation and stability of the oxide layer: at the moment the reliability of the latter for long times and above all at high temperatures has yet to be confirmed. With silicon carbide MOSFET it is difficult to create the interface with the metal oxide: for example, during oxidation, coal clusters are formed. This is more a side effect of the process than a fundamental part; however, this mechanism worsens the interface causing an increase of channel resistance and therefore low mobility and a threshold voltage The characteristics of the silicon carbide MOSFET degrade slightly with temperature and are able to achieve better performance than its silicon counterparts.

The basic parameters of the device are the *length of the L channel*, which is the distance between the two metallurgical junctions n^+ -p, the *width of the Z channel*, the *thickness of the oxide d*, the *depth of the junction* r_j and the *doping of the* N_A *substrate*. The source contact is used as a voltage reference. When there is no voltage applied to the gate, the device can be considered as two junctions p-n in series opposite to each other. The only current that can flow is the with reverse polarization (closed channel).

When a sufficiently large positive polarization is applied to the gate, the central MOS structure undergoes inversion, in this way an *inversion layer* is formed between the two regions n +, i.e. a *"channel"*. The source and the drain are now connected by a n-type conducting channel

through which an intense current can flow [26]. In figure 19 we can see the sectional representation of a MOSfet.

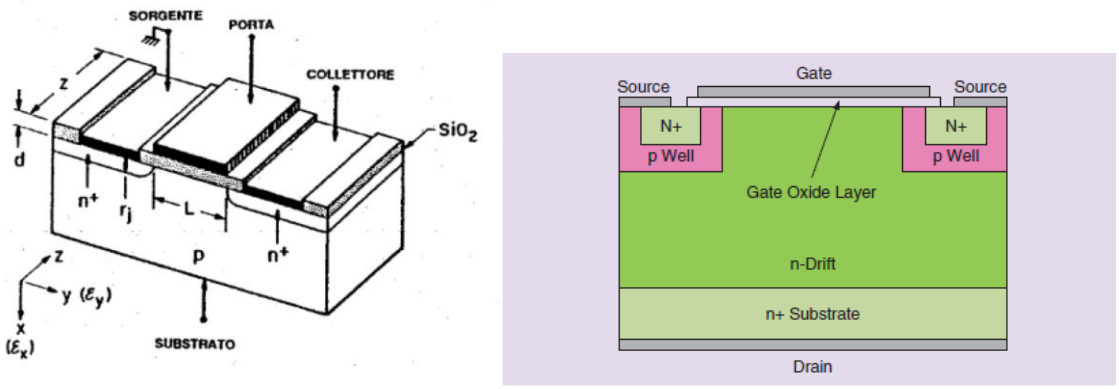

FIGURE 19. SKETCH OF A MOSFET DEVICE.

In figure 20a we show the characteristic drain current-tension ($I_D - V_D$) for different gate voltage, V_G. In the following we describe the inversion layer formation and the different operating areas of MOSFET (see figure 20b).

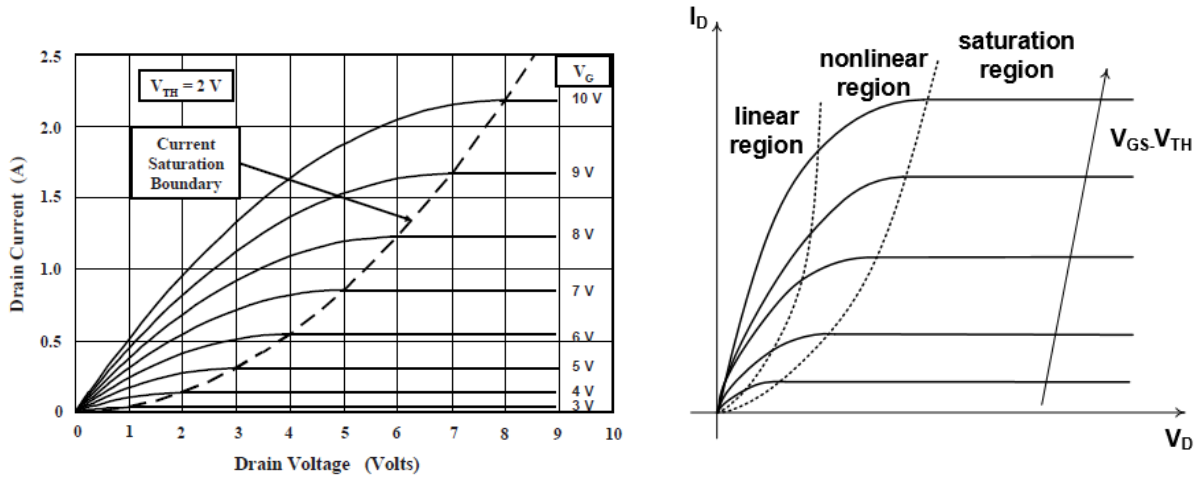

FIGURE 20. (A) DRAIN CURRENT – TENSION CHARACTERISTICS AT DIFFERENT THRESHOLD VOLTAGE. IN (B) THE DIFFERENT OPERATING AREAS ARE INDICATED.

The gate voltage V_{TH}, named threshold voltage, is the voltage for which the inversion layer is formed. It can be expressed as [27]:

$$V_{TH} = V_{FB} + 2\varphi_B + \frac{\sqrt{2\varepsilon_{SiC} q N_A (2\varphi_B)}}{C_{OX}}$$

EQUATION 25

The general expression for the drain current is the following:

$$I_D = \frac{W}{L}\mu_n C_{OX}\left\{\left(V_G - V_{FB} - 2\varphi_B - \frac{V_{DS}}{2}\right)V_{DS} - \frac{2}{3}\frac{\sqrt{2\varepsilon_0 \varepsilon_{SiC} q N_A}}{C_{OX}}\left[(V_{DS} + 2\varphi_B)^{3/2} - (2\varphi_B)^{3/2}\right]\right\}$$

EQUATION 26

where μ_n is the mobility of the carriers (electrons in this case) in the inversion channel, C_{OX} is the capacity of the oxide, V_{DS} is the voltage between drain and source, ε_{SiC} is the dielectric constant of the SiC epilayer [27].

SUBTHRESHOLD REGION, $V_G < V_{TH}$

When the gate voltage is below the threshold one but sufficient to create a weak inversion on the surface, and if a small drain voltage is applied, a small drain current flows through the channel:

$$I_D = \frac{W}{L}\mu_{eff}\left(\frac{kT}{q}\right)^2 \sqrt{\frac{\sqrt{2\varepsilon_0 \varepsilon_{SiC} N_A}}{2\varphi_s}}\left(\frac{n_i}{N_A}\right) e^{\left(\frac{q\varphi_s}{kT}\right)}\left(1 - e^{\left(\frac{-qV_{DS}}{kT}\right)}\right)$$

EQUATION 27

where μ_{eff} is actual mobility.

Figure 21 shows the process of formation of the depletion region and inversion layer.

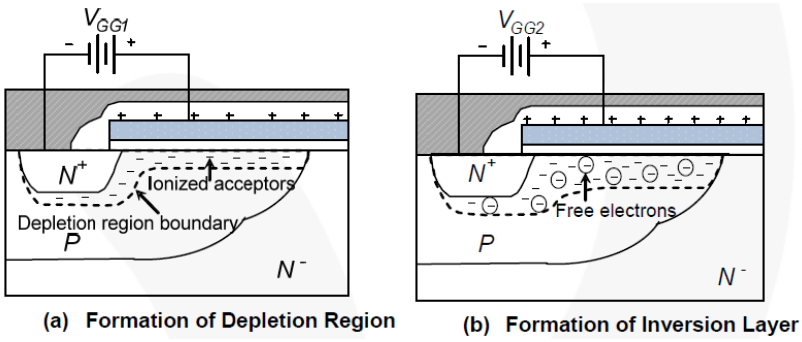

FIGURE 21. PROCESS OF FORMATION OF INVERSION LAYER.

LINEAR REGION, $V_{DS} \ll (V_{GS}-V_{TH})$

The channel induced by the gate voltage has a uniform thickness and behaves like a variable ohmic resistance; for a small drain I_D voltage it is proportional to V_{DS}:

$$I_{D,lin} = \frac{W}{L}\mu_n C_{OX}(V_{GS} - V_{TH})V_{DS}$$

EQUATION 28

Figure 22 shows the process of formation of the inversion layer.

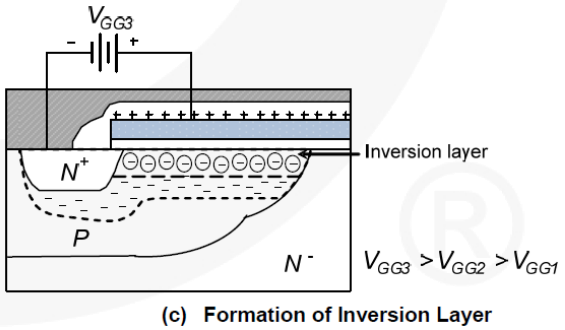

FIGURE 22. PROCESS OF FORMATION OF INVERSION LAYER.

NON-LINEAR REGION, $V_{DS}<(V_{GS}-V_{TH})$

As the V_D increases, the space charge region around the drain junction extends further into the channel region, repelling the mobile charge carriers. The point where the Q_n inversion charge is zero is called a *pinch-off point*. The drain current takes the form:

$$I_{D,nonlin} = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_{TH} - \frac{V_{DS}}{2}\right)V_{DS}$$

EQUATION 29

SATURATION REGION $V_{DS}\gg(V_{GS}-V_{TH})$

Beyond the pinch-off point the drain current saturates because the pinch-off point moves towards the source, but the voltage at this point remains the same. The drain current is given by:

$$I_{D,sat} = \frac{1}{2}\frac{W}{L}\mu_n C_{OX}(V_{GS} - V_{TH})^2$$

EQUATION 30

Figure 23 shows the IDSS current trend, for a different regions described before.

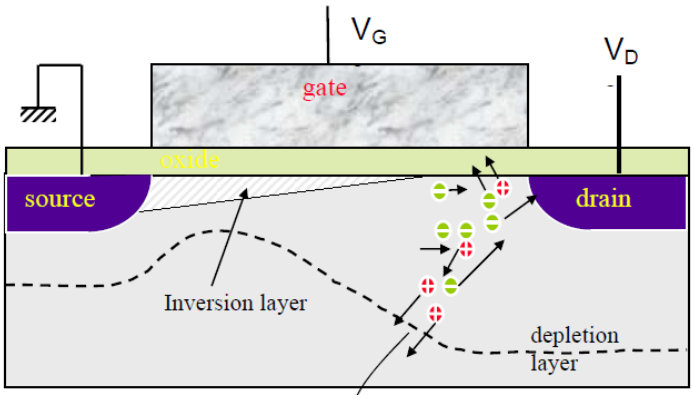

FIGURE 23. THE TREND OF THE DRAIN CURRENT, AS THE VOLTAGE VARIES, FOR THE DIFFERENT REGIONS DESCRIBED BEFORE.

The highest electric field encountered in a MOS semiconductor is located in the gate-oxide region. Nowadays, the gate oxide is becoming thinner and thinner; therefore, the electrical field is getting higher and higher.

A good gate oxide can stand up to 10 MV/cm. However, during manufacturing, a certain defect density will be unavoidably introduced that will degrade the time-dependent dielectric breakdown (TDDB) lifetime. With a high electric field, holes injection can occur on the anode side that will generate traps that gradually degrade the oxide ~~for TDDB~~. Many different models have been reported, but the two most popular models are called E model, equation 31, and 1/E model, equation 32:

$$TF = A_0 e^{-\gamma E_{ox}} e^{Q/K_B T}$$

EQUATION 31

where TF represent the time to failure, γ is the field acceleration parameter and Q is the activation energy.

$$TF = \tau_0(T) e^{G(T)/E_{ox}}$$

EQUATION 32

where τ_0 is the temperature dependent pre-factor, *G(T)* is the field acceleration parameter (temperature dependent).

For any new process development and process change, if the gate-oxide integrity may change, the full TDDB characterization must be done to ensure the reliability of the MOS device.

Usually this is done by using test structures and doing the accelerated test by using a high electric field and high temperature. However, the formal TDDB tests still take a long time. The voltage ramping, often called VRAMP, can be used to do a quick assessment between different process conditions. The VRAMP method uses a small voltage step to stress the oxide for a short time at each step until the oxide breakdown.

GROWTH TECHNIQUES

This chapter deal with both the growth techniques and the associated problems, as well as the oxidation and nitriding processes of SiC.

Modern semiconductor devices are build performing a growth process from high-quality crystalline substrate. Due to chemical-physical nature of SiC substrate, unlike other semiconductors, it is not easy to find a suitable growth process that does not cause defects both in the bulk and on the surface. A noticeable advantage, however, is that like Silicon, Silicon Carbide has a native oxide, SiO_2 (insulator), easily obtained through oxidation processes. These processes are crucial for the realization of integrated circuits since the oxides separate different active zones in the devices.

The reason why the oxidation process is so important is that the silicon oxide (SiO_2) is identified as a distinctive element of the microelectronics and MOSFET technology revolution. The $Si0_2$ has some remarkable and peculiar properties such as a high resistivity, an excellent dielectric resistance, a wide bandgap (Eg=9 eV) and a high point of fusion [28].

There are two different oxidation processes:

- Thermal oxidation
- Deposition oxidation (DCS-HTO)

Following the oxidation process, the oxide is subjected to a nitriding process named POA (Post Oxidation Annealing) using a gas containing nitrogen (NO or N_2O). This process leads to improvements in the device's performance, on the stoichiometric (the deposited oxides are sub-stoichiometric, ie SiOx) and on the interface between the oxide and semiconductor, since it reduces the density of the states of the defects.

CHEMICAL VAPOR DEPOSITION (CVD) AND DOPING

One of the main techniques for obtaining high quality SiC wafers, starting from SiC substrates where defects and dopants are not properly controlled, is the Chemical Vapor Deposition (CVD), which allows the epitaxial growth of thin films on a monocrystalline substrate.

This technique uses a chamber in which gases containing Carbon and Silicon flow. Upon decomposition, the gases are deposited on a wafer. Deposition leads to the formation of a crystalline SiC layer at temperatures between 1400°C and 1600°C.

There are different types of gas used as silicon and carbon precursors: SiH_4, $SiH2Cl_2$, SiCl4 and SiH6 for Silicon, C_3H_8, C_2H_4, CH_4 for Carbon. The procedure of CVD is represented in the figure 24.

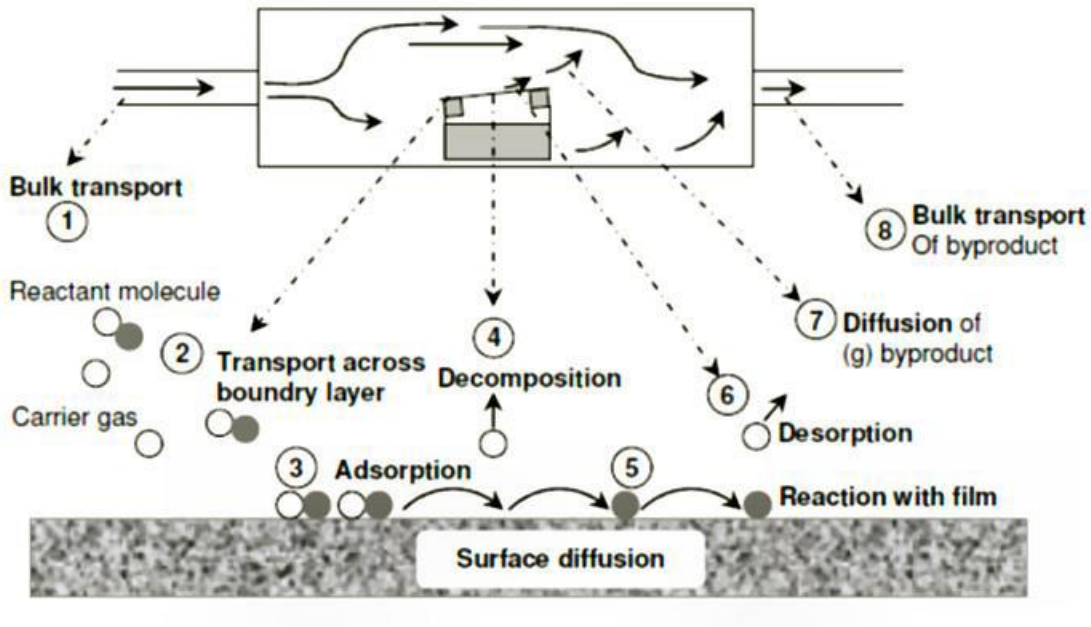

FIGURE 24. THE FIGURE SHOWS THE PHASES PRESENT IN THE CVD PROCESS.

Figure 25 shows the typical SiC homoepitaxial growth process using SiH_4 and C_3H_8. The first phase is called *etching*: in this phase HCl is introduced at a temperature of 1200/1300°C, which makes active the surface of the substrate, eliminating contamination and impurities. When the etching finish, the temperature is reduced and the H_2 flow is increased; the latter ensures the removal of residual HCl in the reaction tube. After this phase, the reactor temperature is increased to the value suitable for crystal growth while the hydrogen flow is kept constant. Once a uniform temperature is obtained, the precursor gases are inserted into the reactor.

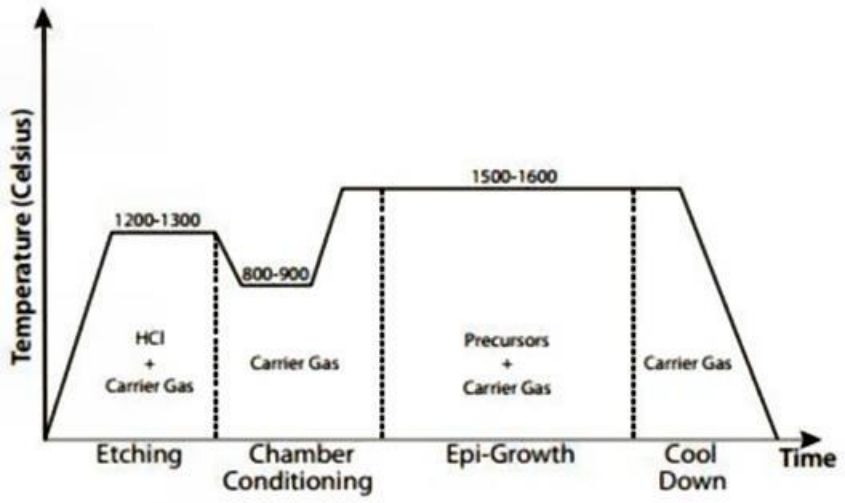

FIGURE 25. TEMPERATURE PROFILE FOR THE DIFFERENT PHASES OF SIC HOMOEPITAXIAL GROWTH PROCESS.

After the crystal has grown, the precursor gases are expelled from the reactor, and the temperature is kept constant for a few minutes to prevent the inclusion of low temperature polytypes.

The doping procedure is performed during the growth of epitaxial layers through the CVD technique. The effect of doping with nitrogen is greater when a low C/Si ratio is maintained and lower in high C/Si conditions. This is since nitrogen atoms replace those of carbon in SiC. A lower concentration of carbon atoms on the growth surface favors the incorporation of nitrogen atoms into the lattice.

Nitrogen doping also depends on growth pressure, it is limited when the growth pressure decreases. This is because the C/Si ratio increases on the growth surface, due to an increase in desorbed silicon atoms, see figure 26.

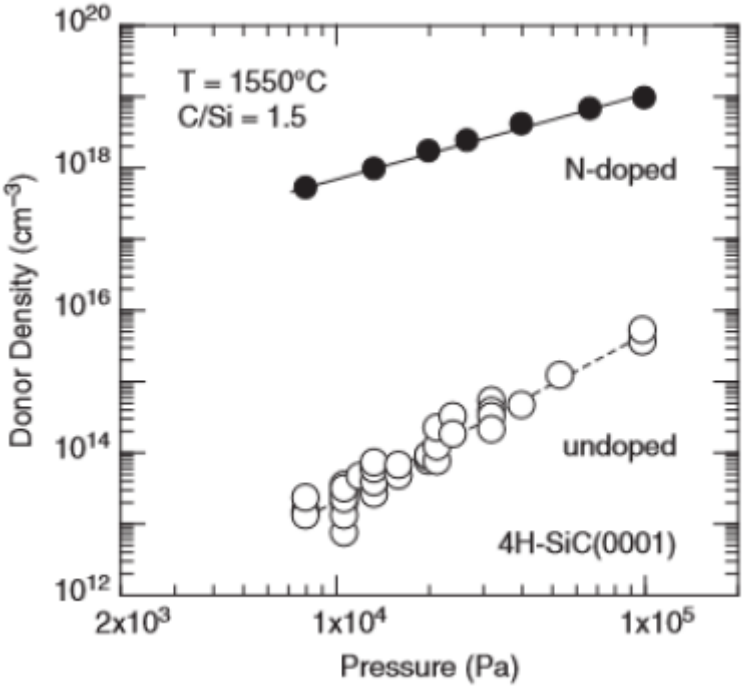

FIGURE 26. DONOR DENSITY DEPENDENCE ON GROWTH PRESSURE [29].

THERMAL OXIDATION

The thermal oxidation of SiC is described by the Deal-Grove model used for Si [30] [31] with some modifications to consider the diffusion of CO/CO_2 molecules from the growth front since half of the oxidized atoms must be removed [32]. The mechanism is described by the equations of linear-parabolic rate of growth, which describe the oxidation process in five phases [27]:

- transport of oxygen on the surface of the oxide
- diffusion of O_2 through the pre-existing oxide film
- chemical reaction of O_2 with SiC at the SiC/SiO_2 interface
- out diffusion (diffusion towards the outside) of the reaction by-products (CO, CO_2) through the oxide film
- removal of these gases from the surface of the oxide

The SiC surface reaction involves an oxygen atom that breaks the chemical bond of a SiC molecule. The insertion of oxygen creates a Si-O-C species, which then splits into a CO

molecule and a Si atom with a free bond. These CO molecules diffuse through the oxide and react with an oxygen atom, creating CO_2. These last two steps are not part of the silicon oxidation model. To form SiO_2, the Si atoms react with the oxygen that reaches the SiC surface. The general process that takes place on the SiC surface is governed by the following chemical reaction [27]:

$$2SiC + 3O_2 \rightarrow 2SiO_2 + 2CO$$

EQUATION 33

In the Deal-Grove model for silicon oxidation, the thickness of the grown oxide layer $X(t)$ follows the equation [27]:

$$X(t) + AX = B(t + \tau)$$

EQUATION 34

where t is the oxidation time, τ is the time required to grow an initial oxide thickness $X0$ and A and B are constants dependent on diffusion and oxygen reaction coefficients, oxidation temperature and oxygen partial pressure [30] [31]. In the case of SiC, these two constants also depend on the diffusion and the CO reaction coefficients. The solution of the quadratic equation indicated above is:

$$X = \frac{A}{2}\left(\sqrt{1 + \frac{t + \tau}{A^2/4B}} - 1\right)$$

EQUATION 35

For short oxidation times, i.e. for thin oxides, the step that limits the oxidation process is the reaction that takes place at the SiC interface with oxygen. When $(t+\tau) \ll A^2/4B$, equation becomes [27]:

$$X = \frac{B}{A}(t + \tau)$$

EQUATION 36

and B [$\mu m/2h$] is called a parabolic speed constant. In this case the limiting process is the diffusion of oxygen through the grown oxide since the oxidation rate is determined by the availability of oxidant on the SiC surface [27]. However, the Deal-Grove model is not directly applicable to SiC since it does not include the out-diffusion phase and the formation of CO_2. In Si the constants A and B are defined by these two expressions, in the case of a first order reaction [30]:

$$B = \frac{2D_{eff}C^*}{N}$$

EQUATION 37

$$A = 2D_{eff}\left(\frac{1}{k} + \frac{1}{h}\right)$$

EQUATION 38

where D_{eff} and C^* are the actual diffusion coefficient and the equilibrium oxygen concentration in the oxide, N is the number of oxygen molecules incorporated in a unit volume of the oxide layer, k is the coefficient of the reaction rate at Si surface, and h is the transport coefficient for oxygen gas. According to the models presented in [32] [33] [34], the linear velocity constant for SiC oxidation becomes:

$$\frac{B}{A} \approx \frac{C^*}{N}F_f$$

EQUATION 39

Where K_f is the direct reaction rate constant. As far as the parabolic speed constant is concerned, there are two cases, depending on whether the speed limiting step in this regime is the diffusion in O_2 or the diffusion of CO, a topic still debated in the literature. Therefore, B is expressed respectively by [27]:

$$B = \frac{2C^*}{1.5N}D_{O_2}$$

EQUATION 40

$$B = \frac{2C^* K_f}{NK_r} D_{CO}$$

EQUATION 41

where Kr is the inverse reaction rate constant and D_{CO} is the diffusion coefficient of the CO gas through the oxide.

Also, for SiC, the rate of oxidation strongly depends on the orientation of the crystal much more than in the case of silicon [35]. In particular, the oxidation rate for the face C (0001) is almost one order of magnitude higher than that for the face Si (0001), while the face a (1120) is in the middle (see figure 27).

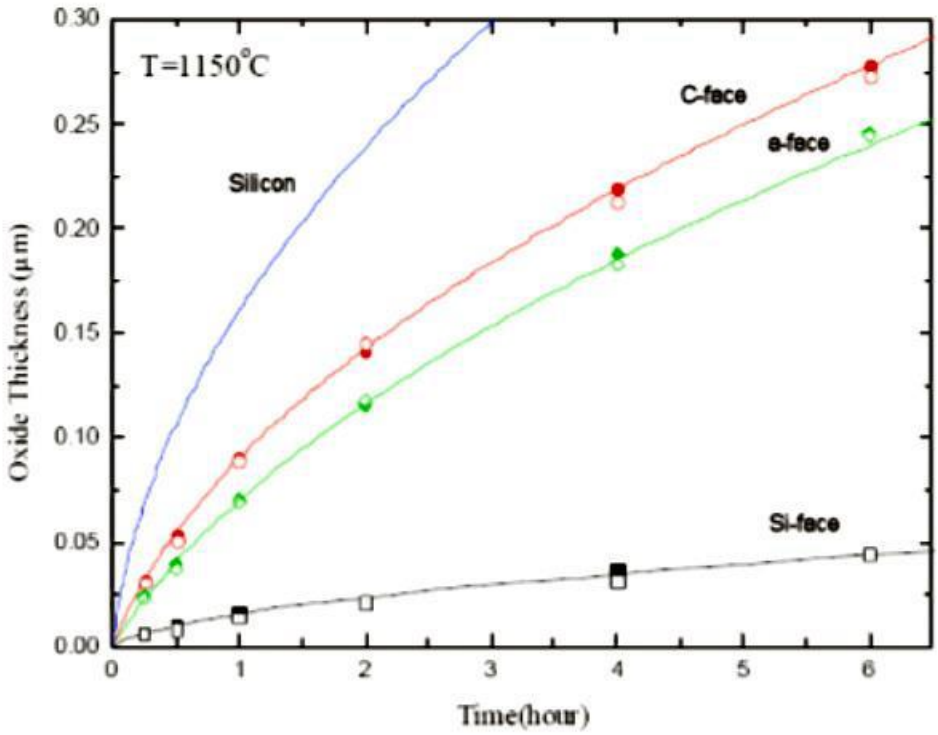

FIGURE 27. DEPENDENCE OF THE RATE OF OXIDATION ON THE ORIENTATION OF THE CRYSTAL [36].

Furthermore, the thermal balance required to form a gate oxide of the required thickness is about ten times higher than that of Si, the Si-C bond being stronger. This means that the oxidation is performed at very high temperatures, usually at 1100°C - 1300°C. Alternatively, to reduce the process time, SiO_2 layers made by Chemical-Vapor-Deposition (*CVD*) can be

used, but a thermally grown oxide is still required to ensure a physical connection with the underlying SiC.

Another way to reduce process time is an oxidation performed at higher oxygen partial pressures [33] [37].

OXIDATION THROUGH DEPOSITION PROCESS - DCS-HTO (DICHLOROSILANE-HIGH TEMPERATURE OXIDATION)

In this oxidation process, the silicon is carried to the oxidation chamber using gaseous or liquid reagents. The deposition is obtained by using the *CVD* technique of the *LPCVD* type (low pressure *CVD*) at a temperature of about 800°C. To optimize the quality of the SiC/SiO_2 interface, precursors that do not contain carbon are used for the deposition, since the presence of the latter has a negative influence on the channel mobility of the MOS, as observed in the case of thermal oxidation. A typical reaction that takes place inside the chamber using dichlorosilane (SiH_2Cl_2) with the dinitrogen (N2O) is:

$$SiH_2Cl_2 + 2N_2O \rightarrow SiO_2 + 2HCl + 2N_2$$

EQUATION 42

Through this reaction SiO_2 is deposited at a temperature of 800°C. After deposition, the oxides undergo to a thermal oxidation process which improves the performance and characteristics of the interface with the semiconductor.

In the previous chapters we have discussed the many useful aspects that made SiC-based device leader in the field of microelectronics. However, the presence of defects gives rise to a serious difficulty in understanding the failure mechanisms, worsening the reliability of the devices [38].

The defects can be observed in as-grown n-type and p-type SiC epitaxial layers and are due to the thermodynamics of the solid state and populate all crystals. *Extrinsic defects* are induced by stoichiometry and impurities. In table 3 it is shown the most important extended defects observed in SiC wafers [12].

Dislocation	Major direction	Typical density (cm^{-2})
Micropipe	<0001>	0–0.1
Threading screw dislocation (TSD)	<0001>	300–600
Threading edge dislocation (TED)	<0001>	2000–5000
(Perfect) Basal plane dislocation (BPD)	in {0001} plane (preferably <11$\bar{2}$0>)	500–3000

TABLE 3. MAJOR EXTENDED DEFECTS OBSERVED IN SIC BOULES AND WAFERS.

The intrinsic defects cannot be removed; hence we try to find strategy to reduce and eliminate (as long as possible) extrinsic defects: those defects that are responsible of device degrading and breakings. In this context, “extrinsic” refers to early failures due to oxide defects. Since the extrinsic failures do not represent the fundamental properties of the oxide, they are eliminated from statistical failure distribution.

Extrinsic defects can be found both on the gate oxide and on the epitaxial layer. Extrinsic defects affect almost all engineering properties, but they are particularly important in semiconducting crystals, where extrinsic defects are used to control electrical properties, and

in structural metals and alloys, where extrinsic defects are added to increase mechanical strength. It is useful to identify the characteristics of this according to their nature (zero-, mono-, bi- or three-dimensional) [29].

Defects in semiconductors also can be classified as: point defects and extended defects. Point defects are localized in a lattice site, involving only a few nearest neighbors and not extended to any spatial dimensions. Extended defects, such as, grain boundaries, dislocations and/or stacking faults, are extended in all dimensions [39] [40].

POINT DEFECTS

During growth, subsequent cooling and device processing, defects will be created intentionally or unintentionally in the SiC lattice.

Point defects exist in small concentrations in all semiconductor materials and formed mainly due to vacancies, interstitials, and substitutions. Aggregation of few point defects which generate a perturbation in a lattice site and its immediate vicinity, such as, divacancies, vacancy–donor complexes, are also considered as point defects [41].

Defects can be intentionally introduced by impurity doping to increase conductivity [42]. A defect is of intrinsic origin, if the defective volume is composed of the same atoms as the undisturbed crystal lattice. If foreign atoms, such as doping impurities, take part in the defect, the defect is said to be of extrinsic character. Small amount of point defects exists in all semiconductor materials, and they are point-like defective volumes, limited roughly to the size of a unit cell of the crystal structure, such as a substitutional impurity, vacancy, interstitial or antisite [43]. Substitutional impurity means that an atom is replaced by another atom not belonging to the crystal lattice. Vacancies occur if one atomic lattice position is left empty in the crystal. Atoms not placed in an ordinary lattice site but in between are called interstitials. If they are of the same kind as the crystal lattice, they are called self-interstitials otherwise impurity interstitials. An interstitial atom together with a vacant lattice site is labeled FRENKEL pair. If in a compound semiconductor, such as SiC, C is taking a Si-lattice site, or Si is sitting on a C-place, the defect is called antisite. Defects including two or slightly more atoms form complexes or complex structures. A vacancy paired with an impurity atom form a vacancy-

impurity complex. A split interstitial is given when two atoms take the lattice place of only one atom [88] and thus disturbing the lattice locally. In case of SiC, if two carbon interstitials are close to a carbon atom and in addition shift the carbon atom from its original position, a dumbbell self-interstitial complex is formed [89]. Increasing the numbers of joining atoms, the defect can be assigned to defect clusters, such as Ci-aggregates [44]. Point defects introduce electronic energy states within the semiconductor bandgap which can act as, 'traps', 'recombination centers', or 'generation centers' and may modify the semiconductor properties and device performances significantly. The introduction of deep levels, which serve as trapping centers, decreases the minority charge carrier lifetime or increases the resistivity by compensation effects [43]. The point defects are desirable for some devices and introduced intentionally. As for example, in switching devices, energy levels introduced by point defects can be used as recombination centers which help to remove minority carriers quickly during turning off and enhance the device's switching speed thereby increasing efficiency [45] [46]. However, for many cases point defects are detrimental to the device performances. Energy states created by point defects may act as a recombination center for the generated electron-hole pairs and degrade the performance of the devices.

Extended Defects

Morphological Defects

If whole atomic planes are shifted, the defect is no longer a point defect but belongs to the class of extended defects; most of SiC devices are fabricated in such a way that their electrically active regions reside entirely within the epilayer grown on bulk crystal substrate [41]. The electrical characteristics of these devices critically depend on the quality and smoothness of the semiconductor surface. So, the defects contained in the epilayer are of great interest to any opto-electronic devices [41]. The defects in SiC epilayer that impact electronic devices performances are threading screw dislocation (TSD), threading edge dislocation (TED), basal plane dislocation (BPD), small growth pits, triangular inclusions, carrots, and comet tail defects [47] [48] [49]. For this kind of defects, it is possible to define a length along the off-direction, L, close to the length of a basal plane in the epilayer when projected onto the surface, taking into account the substrate off-angle, ϑ:

$$L \approx {}^{d_{epi}}/_{tan\vartheta}$$

EQUATION 43

where d_{epi} is the epilayer thickness. The presence of this defects has a very important implication: these defects are nucleated at the very initial stage of epitaxial growth. If these defects are observed (though they are not desirable), the epilayer thickness can be estimated from the defect length [29].

Lots of defects originated in bulk cannot propagate to the epilayer, so the epitaxial layer contains significantly fewer defects than bulk wafers.

THREADING SCREW DISLOCATION AND MICROPIPES

The TSD can penetrate along the crystallographic c-axis through the entire length of the crystal [41]. Screw dislocations terminate only in the crystal surface and are present in all wafers cut from the grown crystal. This screw dislocation can propagate throughout the whole thickness of epitaxial layer grown by CVD technique. Additional screw dislocation may also form during the epitaxial [50] [51]. Extended screw dislocation is usually measured by the length of the Burgers vector (b). For pure screw dislocation the Burgers vector is parallel to the crystallographic c-axis and the Burger vector length is related to the step height of the screw dislocation. Screw dislocation with large Burger vector forms hollow cores and is widely known as micropipes [52].

As discussed before, a screw dislocation is a common dislocation that transforms successive atomic planes within a crystal lattice into the shape of a helix. Once a screw dislocation propagates through the bulk of a sample during the wafer growth process, a *micropipe* is formed. Micropipes are hollow tubular defects penetrating the SiC single crystals and their radius ranges from a few tens of nanometers to several tens of micrometers. The performance of SiC based power devices and radiation detectors is severely degraded by these micropipes [48] [53] [54]. The presence of a high density of micropipes within a wafer will result in a loss of yield in the device manufacturing process. Substrate micropipe defects with an area of 1 mm^2 or larger may cause pre-avalanche reverse-bias point failure in epitaxially grown p-n junction devices. Studying the evolution of this dislocation during CVD

growth, it has been shown that micropipes can be dissociated into several elementary closed-core screw dislocations, leading to "*micropipe closing*". On the growing surface, competition exists between spiral growth around a micropipe and step-flow growth as a result of the off-axis substrate. With the steady development of the material growth process, the micropipe densities have been reduced drastically (from 104 cm^{-2} to less than 1 cm^{-2}) and recently vendors have grown micropipe-free epitaxial layers [55] [41]. The SiC screw dislocation with small Burgers vector forms close core and sometimes termed as elementary screw dislocations which exist at densities on the order 29 of thousands per cm^2 in 4H- and 6H-SiC wafers and epilayers [56] [57].

Close core dislocation is not as detrimental as micropipes, however, experimentally it is proven that theses defects have negative impact on device performances [53]. It is found that soft breakdown (at voltage <250 V) in 4H-SiC p-n junction diodes may happen due to this close core dislocation. Wahab et al. showed that increasing density of close core dislocations in the active region can cause the degradation of the breakdown voltages [58].

It is believed that micropipe closing takes place when step-flow growth is dominant, even near the core of a micropipe, and the core is directly swept by steps proceeding in the lateral direction. Although micropipes are now almost eliminated in the substrates (wafers), micropipe closing during epitaxial growth is an interesting phenomenon from the viewpoint of defect engineering [29].

Basal Plane Dislocation (BPD)

Basal plane dislocations (BPDs) probably have the highest density of all the dislocations. BPDs easily slip under stress because the critical resolved shear stress is relatively low in SiC, especially at high temperature. The glide motion of BPDs during epitaxial growth has in fact been observed by X-ray topography. BPDs form to relaxation of the thermal stress which mainly occurred during cooling down from high growth temperature to room temperature. A large temperature inhomogeneity can induce significant thermal stress, and when this stress is added to the misfit stress (i.e., acts in the same direction) pre-existing BPDs glide for lattice relaxation. The direction of glide motion depends on the Burgers of the BPD and the stress direction.

BPDs in p-n diodes may dissociate into two Shockley partials, that is a pair of a dislocations which can lead to the presence of stacking faults, and cause an increase of forward voltage drop [41] [59]. Basal plane tilt low angle grain boundaries due to the pile-up of BPDs [67]. BPDs often lies near the interface between a lightly doped epitaxial layer and a heavily-doped substrate; thus, a BPD lying at the epitaxial layer/substrate interface is called an “interface dislocation”. Note that this is not a pure misfit dislocation resulting from lattice relaxation caused by doping-induced misfit strain, because such interface dislocations are not observed, even for more than 100 µm-thick n^--type SiC epitaxial layers, when they are grown under appropriate conditions.

THREADING EDGE DISLOCATION (TED)

Threading edge dislocation (TED) is an edge type dislocation which has Burgers vectors perpendicular to along the c-axis of the crystal. TEDs are mostly inherited from the substrate. Basal plane dislocations (BPDs) propagate from the off-axis 4H-SiC substrate into the homoepitaxial layer and convert into threading edge dislocations in the epitaxial layer. The conversion from BPDs to TEDs happens due to the image force in the epilayers. The converted dislocations are inclined from the c-axis toward the down-step direction by about 15° [60]. Ha et al. [61] suggest that TEDs may also form due to prismatic plane slip.

STAKING FAULTS

Staking faults (SFs) are kind of planar defects and exist mostly in the primary slip plane {0001} of SiC. SFs occur due to the deviation of Si–C bilayers from the perfect stacking sequence along the c-axis of the crystal. Stacking faults are common defects because of the low stacking fault energy (14 mJ m^{-2} for 4H-SiC and 2.9 mJ m^{-2} for 6H-SiC) and the occurrence of many polytypes in SiC. SFs reduce the barrier height and the breakdown voltage of a Schottky diode. An electrostatic potential may appear in SiC p-n diodes due to the charge accumulation in the stacking faults and can increase the forward voltage drop in the diode [60]. Through the recent progress in polytype control, inclusions of foreign polytypes and stacking faults have been greatly reduced. The typical stacking fault density along the c-axis is well below 1 cm^{-1}. Generation of stacking faults during SiC epitaxial growth is one of the remaining issues [29].

MORPHOLOGICAL DEFECTS DELINEATION BY ETCHING

Chemical etching of silicon carbide is the most versatile way to characterize silicon carbide crystals and has been effectively used to evaluate the crystal qualities. Most of the chemicals that need in chemical etching process are used in molten state. Since the sublimation temperature of SiC is 2830 ˚C, it is possible to etch SiC at temperature as high as 1200 ˚C. Due to high number of hazards involved in etching SiC at such high temperature, a new method of SiC low temperature etching is necessary. Molten KOH etching is the widely used method of etching to investigate the growth defects in SiC wafers. SiC etching by molten KOH is an isotropic etching which is a non-directional etching with uniform etch rate in all directions of the wafers. Thus, melt KOH removes the SiC surface layers at the same etch rate in all directions regardless of the orientation of the crystal.

ELECTRICALLY ACTIVE INTRINSIC DEFECTS IN SIC

Defects in the band gap can be classified according to their energetic properties in the gap; whether they are shallow - hydrogenic impurities or deep. Deep levels can be further characterized by their interaction strength with the bands, as traps or recombination centers [62].

Defects are often divided into two groups: shallow and deep levels. Depending on the size of the band gap, a level may be regarded by its energetic location as deep in Ge or Si but may be shallow in a wide-band gap semiconductor.

Deep-level traps or deep-level defects are a generally undesirable type of electronic defect in semiconductors. They are "deep" in the sense that the energy required to remove an electron or hole from the trap to the valence or conduction band is much larger than the characteristic thermal energy Deep traps interfere with more useful types of doping by compensating the dominant charge carrier type, annihilating either free electrons or electron holes depending on which is more prevalent. Therefore, Deep levels can further be classified after their primary interaction with the bands. If the electron capture rate, cn, is much larger than the hole capture, cp (cn >> cp), then the defect is called electron trap; vice versa if the hole capture is larger than the electron capture, then the defect is acting as a hole trap (cp >> cn). If both capture rates are almost similar (cn ≈ cp), then the defect interacts with the same

strength with both bands and is regarded as a generation-recombination center (G-R center), shown figure 28.

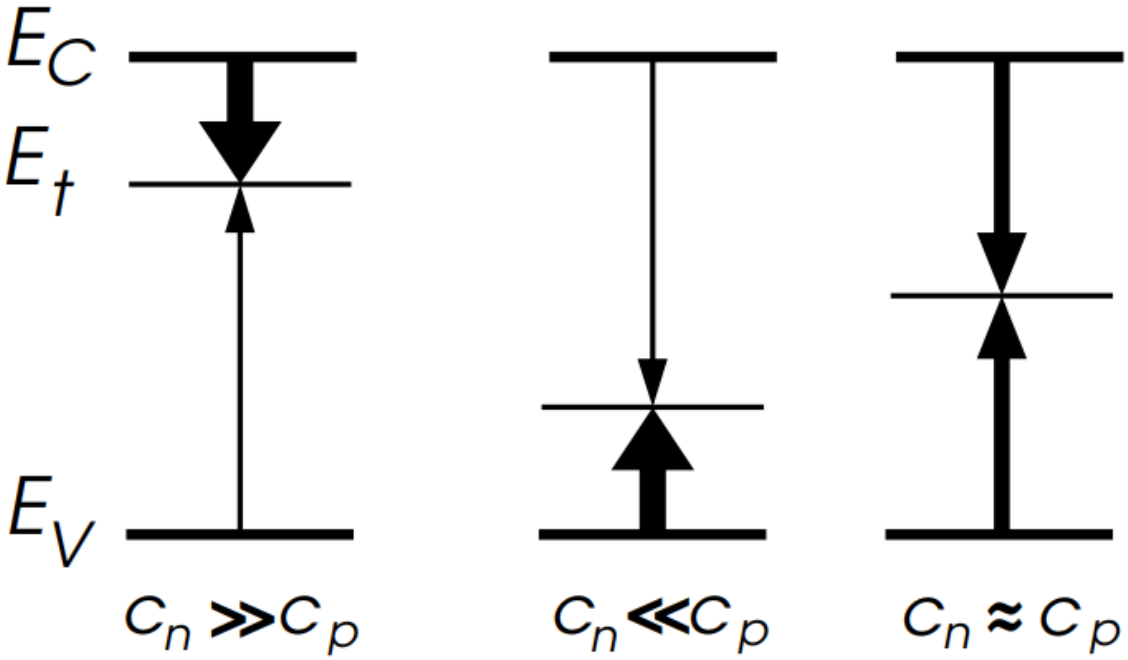

FIGURE 28. CAPTURE AND EMISSION CHARACTERISTICS OF TRAPS AND RECOMINATION CENTERS [62].

Recombination of excess carriers via this state may be responsible for the reduced lifetimes inside the fault region. Trapping of electrons at these states naturally causes the formation of a space-charge region in the vicinity of the stacking fault, which may create a potential barrier to electron transport.

Deep levels acting as recombination centers interact with both the valence and conduction band. As such, the defect levels reduce the minority charge carrier lifetime. Impurities in semiconductors play an important role to adjust their semiconducting properties. Intentional doping can introduce shallow defect levels to increase the conductivity or deep levels for achieving semi-insulating (SI) SiC. Impurities, especially transition metals generate defect levels deep in the band gap of SiC, which trap charge carriers and thus reduce the charge carrier lifetime.

SCREENING AND DETECTION METHODS OF FAILURE (EWS, WLBI & BI)

ELECTRICAL WAFER SORT - EWS

EWS is the set of tools, hardware and software, which allow the test electric of each die made on the wafers coming out of a line of production. The result of the test is the compliance of the die tested with certain requirements of functionality, in particular with respect to product specifications. The test provides a significant amount of information that allows for analysis details of the possible causes of rejection. The EWS represents one of the main activities for the improvement of production process and to increase the economic return of a certain product.

There are some anomalous events that do not make the processing of the wafers compliant with departmental standard. These events may concern:

- machine parameters and related control charts
- drifts of the process of a given equipment
- criticalities highlighted on large volumes
- use of non-compliant materials
- operation not carried out perfectly
- excessive release of particles (attachment equipment, washing etc ...)

In order to prevent - or minimize their impact - in the process flow they are systematic checks have been introduced such as:

- inspections under the microscope
- control charts of machine and measurement parameters
- automatic visual inspection (KLA, Tencor, AIT)

Prog. EWS: test sequence that allows the verification of the functioning of the parts constituents the device.

At each test (measurement software routine) the die tested is subjected to a determined electrical stress (reading, programming etc ...). Tested devices that fail a certain test are assigned a rejection class, called binning. that are arranged in a map representing the wafer.

WLBI

Wafer level Burn-in refers to the electrical and thermal stress test performed on the wafer and able to detect and cut out the potentially early life failures. The WLBI procedure follows the same principles of Burn-in (see below) but performed directly on the wafer before the packaging and testing a large number of devices simultaneously. The procedure requires the use of a costly probe station but reduces the test time, and the overall costs [63].

HTGB

The high-temperature gate bias (HTGB) stress test for the power MOSFET tests its gate-oxide integrity and ionic-contamination level. It is done by applying the maximum gate voltage allowed by the data sheet while stressing the device at high temperatures and for a long time [63].

HTRB

In the high-temperature reverse bias (HTRB) stress test, typically applied on power devices, a percentage of the BVDSS (drain-source Breakdown Voltage, with VGS=0) allowed by the data sheet is applied to the body diode with the gate grounded to the source while stressing the device keeping it at a high temperature. The stress time depends on the mission profile. The combined electrical and thermal stress can test the junction integrity of the body diode, crystal defects and ionic-contamination level [63].

BI

Burn-in (something like running-in for mechanical parts) is the process to which the components of a system are subjected before being put into service (and, often, before the system has been completely assembled with those components).

The target is to identify those particular components that would fail as a result of the so-called infant mortality, or, during the initial part, at a high rate of failure, of the *"bathtub"* curve of components reliability. If the burn-in period is long enough, and the working condition are

enough to stress the devices, at the end of the test, we can assume that all the infant mortality has been identified.

The stress conditions applied (generally) are temperature and voltage, for a time sufficient to guarantee the screening of infant mortality (extrinsic defects) without affecting the intrinsic lifetime of the device. More generally, the conditions in the field are the set of very complex factors [64].

The most important condition for Burn-in to be effective is that the failure rate follows a bathtub curve, i.e. there is a significant number of initial failures, with a failure rate decreasing after the initial period itself. Stressing all devices for a certain amount of time, devices with the highest failure rate will be the first to fail and can be eliminated by the population. Devices that survive the applied stress will have a more advanced position in the bathtub curve (they will have a lower failure rate). When the equivalent lifetime of the stress is extended into the increasing part of the bathtub-like failure-rate curve, the effect of the burn-in is a reduction of product lifetime. In a mature production it is not easy to determine whether there is a decreasing failure rate. To determine the failure time distribution for a very low percentage of the production, one would have to destroy a very large number of devices. Thus, by applying a burn-in, the infant failures can be avoided at the expense (trade-off) of a reduced yield caused by the burn-in itself. When possible, it is better to eliminate the root cause of early failures than doing a burn-in. Because of this, the burn-in test may eventually phased out as the various root causes for failures are identified and eliminated.

For electronic components, burn-in is frequently performed at high temperature and perhaps high voltage. The components may be under continuous test or simply tested at the end of the burn-in period.

Historically, the manufacturing of semiconductors has been a very elaborate and expensive multi-step process. Here we need to underline that solid-state semiconductor devices, today play a key role in almost all human day life, hence, test their reliability is a fundamental task. Component burn-in generally refers to the process of thermally and/or electrically testing of newly fabricated semiconductor components. Burn-in allows for the individual identification of faulty components that may develop within a lot or batch of semiconductor devices. Currently, components are burned-in at the “package level”, which means that the individually packaged devices are typically tested after being derived from a wafer. Each component is tested and placed in sockets to be burned-in either as a packaged unit or to be

tested as bare die (before packaging). Both die or package level burn-in can be expensive for manufacturers because they require a lot of labour: each component has to be tested, requiring the human action.

The reliability of the overall package will be shown to be highly dependent upon the reliability of each of the bare die. The usual method for achieving highly reliable parts is through burn-in to sort out extrinsic defects. However, there are very few alternatives for burning-in unpackaged (bare) die. These few alternatives are compared in terms of the cost per burned-in die versus wafer volume. Recently a number of improvements have been e introduced, significantly reducing the cost per die [63].

The problems related to burn-in are mainly related to:

- an increase in cycle time and chip management
- a lot of additional direct work (cost)
- limit production growth

In many cases, customers are insensitive to additional costs, they just want "better reliability"!

RAMAN SPECTROSCOPY

INTRODUCTION

The light interacting with molecules and matter can be absorbed, scattered, diffracted, or reflected or may not interact with the material and may pass straight through it. It is well known that a perfectly homogenous medium does not scatter light; the elementary beams re-emitted from different points of such a media interfere destructively and cancel each other in all directions, except for the forward direction [65]. However, scattering does occur due to thermal fluctuations of the atoms in the media, leading to density fluctuations, so the media cannot be considered as perfectly homogeneous anymore. If the inhomogeneities are of the size of the light wavelength, scattering will occur into arbitrary of well-defined direction. The process of absorption is used in a wide range of spectroscopic techniques. For example, it is used in acoustic spectroscopy where there is a very small energy difference between the ground and excited states and in X-ray absorption spectroscopy where there is a very large difference. In between these extremes are many of the common techniques such as NMR, EPR, infrared absorption, electronic absorption and fluorescence emission, and vacuum ultraviolet (UV) spectroscopy. Figure 29 indicates the wavelength ranges of some commonly used types of radiation.

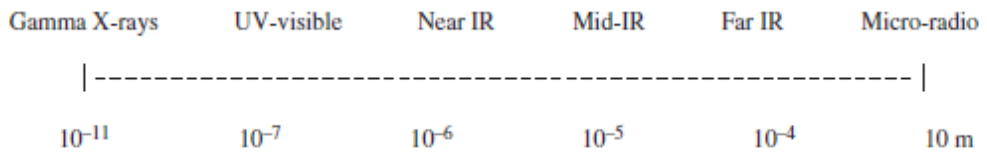

FIGURE 29. THE WAVELENGTH RANGES OF SOME COMMONLY USED TYPES OF RADIATION [55].

Scattering is a commonly used technique. For example, it is widely used for measuring particle size and size distribution down to sizes less than 1 mm. One everyday illustration of this is that the sky is blue because the higher energy blue light is scattered from molecules and

particles in the atmosphere more efficiently than the lower energy red light. However, the main scattering technique used for molecular identification is Raman scattering.

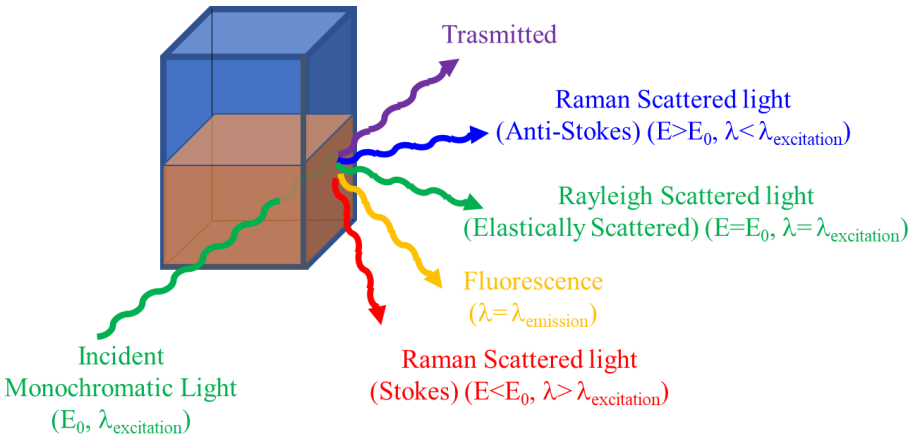

FIGURE 30. LIGHT INTERACTION WITH MATTER.

Raman scattering spectroscopy is a vibrational spectroscopic technique that enables a wide range of information about a material to be acquired. This technique is of particular importance in materials science because it allows to obtain in a simple, non-invasive, fast and efficient way, information on the structural, chemical and electronic properties of a large number of materials. From the experimental point of view, a Raman spectroscopy experiment requires the use of a monochromatic source (usually a laser), a sample holder capable of providing an adequate geometry to the process of scattering the light on the sample, a monochromator and a detector. Unfortunately, the efficiency of the Raman process is rather low, so it is necessary to create very sensitive devices capable of preventing the light from reaching the photodetector without having been dispersed (stray light). Furthermore, the spectral resolution must be high to ensure the analysis of low-frequency Raman signals which are often very interesting [66] [67] [68].

Today many commercial apparatuses (an example in figure 32) are equipped with an optical microscope, and this allows the light coming from a small part of the sample to be sent to the monochromator and therefore to make a real spatial map of the Raman signal. This technique, known as micro-Raman, allows to study the Raman response on a micrometric

scale and therefore to map the presence of chemical species or impurities that otherwise could hardly be detected in a non-invasive way.

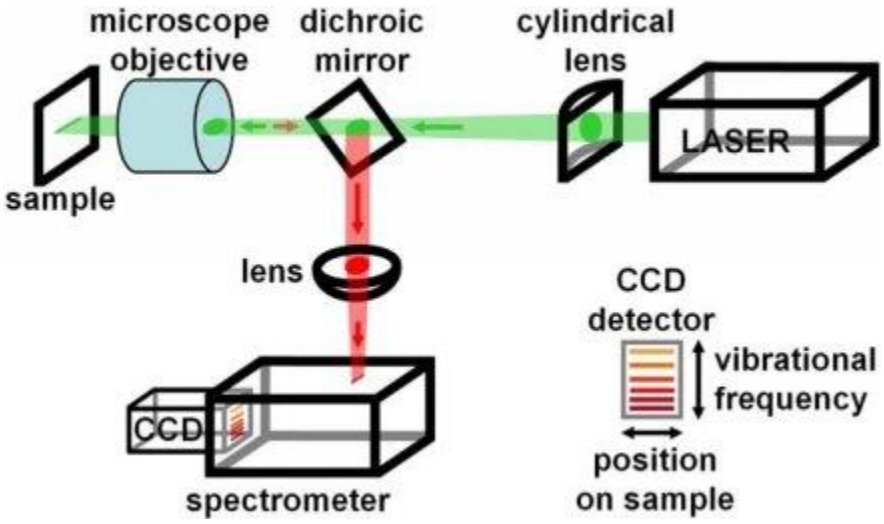

FIGURE 31. SCHEMATIC OF RAMAN SPECTROMETER

The Raman shift is closely related to the vibrational properties of the sample and can be accurately described by treating the system and the electromagnetic field classically. When a molecule interacts with the electromagnetic field **E**, an electric dipole moment **P** is induced which vibrates at three different frequencies.

$$P = a \cdot E + \beta : EE + \gamma : EEE$$

EQUATION 44

Each of these terms depends on the position of the nuclei and therefore on the vibrational state of the molecule.

The energy changes we detect in vibrational spectroscopy are those required to cause nuclear motion [41]. If only electron cloud distortion is involved in scattering, the photons will be scattered with very small frequency changes, as the electrons are comparatively light. This scattering process is regarded as elastic scattering and is the dominant process at the oscillation frequency of the electromagnetic field Eq. 44. For molecules it is called Rayleigh scattering. However, if nuclear motion is induced during the scattering process, energy will be transferred either from the incident photon to the molecule or from the molecule to the

scattered photon. In these cases, the process is inelastic, and the energy of the scattered photon is different from that of the incident photon by one vibrational unit. The photon scattered in this process has energy shift and we call this energy shift Raman shift and the photon scattered by this process Raman scattered photon, see figure 31.

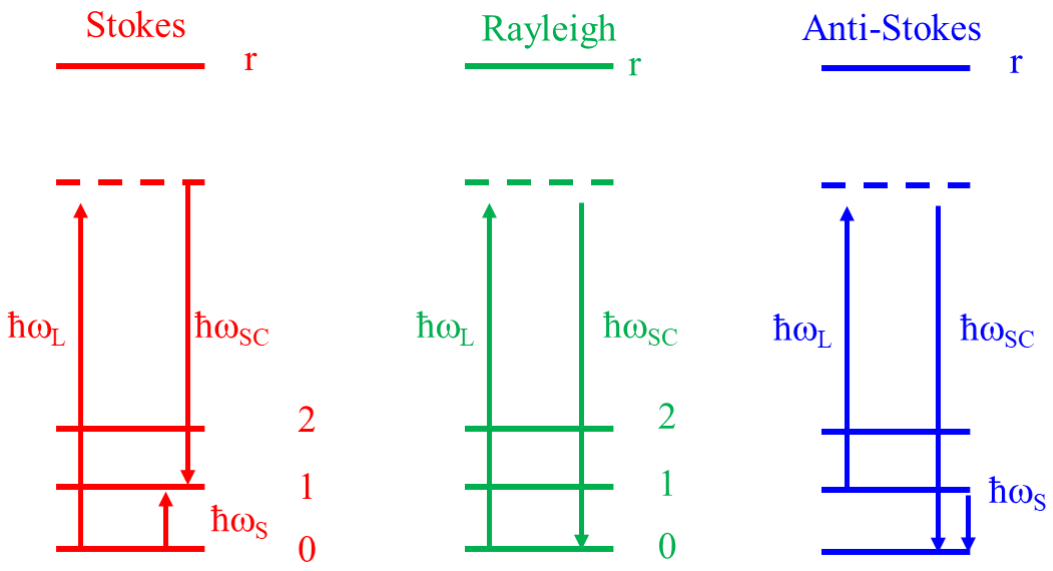

FIGURE 32. INCIDENT PHOTON SCATTERED IN THREE WAYS, (A) RAYLEIGH SCATTERING, (B) FIRST-ORDER STOKES SCATTERING, (C) FIRST ORDER ANTI-STOKES SCATTERING [55].

The other terms of the Eq. 44 obtained for polarization describe two dipoles that oscillate at two different frequencies and therefore radiate energy at these frequencies. These two components of the radiated electromagnetic field correspond to the Raman lines called anti-Stokes (the one with higher frequency) and Stokes (the one with lower frequency). However, the classical theory used to explain the Raman spectra is inadequate and cannot explain the difference in intensity of the Stokes and anti-Stokes peaks.

D. Long [69] using a semi-classical model, gave a convincing explanation of the phenomenon. The proposed model deals with the electromagnetic field in a classical way and the system using quantum mechanics.

$$P_{fi}^{1} = \langle \Psi_f^0 | \hat{P} | \Psi_i^1 \rangle + \langle \Psi_f^1 | \hat{P} | \Psi_i^0 \rangle$$

EQUATION 45

With some hypotheses it is possible to find an expression for the relationship between the intensities of the stokes and anti-stokes lines:

$$\frac{I_S}{I_{AS}} = \frac{(\omega_L - \omega_k)^4}{(\omega_L + \omega_k)^4} e^{-\left(\frac{\hbar\omega_k}{k_B T}\right)}$$

EQUATION 46

Furthermore, the anti-Stokes process is usually weaker than the Stokes process because the probability of phonons being in the higher populated state is lower than in the ground level. However, at room temperature, there is still small probability of finding these phonons in excited states. In the Stokes process, the emitted photon has lower Raman shift than the one emitted in anti-Stokes process i.e. the final energy of the photon is lower in the Stokes process than in anti-Stokes process (figure 32).

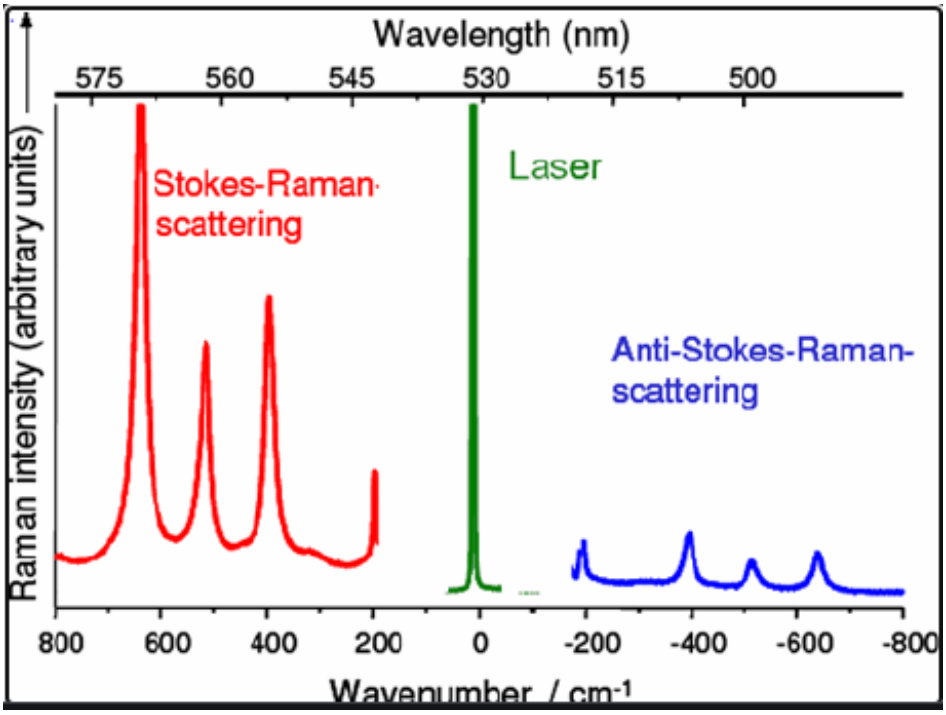

FIGURE 33. STOKES AND ANTI-STOKES RAMAN SPECTRUM (SCHEMATIC). THE STRONG LINE AT ΩL IS DUE TO RAYLEIGH SCATTERING [55].

The way in which radiation is employed in infrared and Raman spectroscopies is different. In infrared spectroscopy, infrared energy covering a range of frequencies is directed onto the sample. Absorption occurs where the frequency of the incident radiation matches that of a vibration so that the molecule is promoted to a vibrational excited state [55]. The loss of this frequency of radiation from the beam after it passes through the sample is then detected. If the energy of an incident photon corresponds to the energy gap between the ground state of a molecule and an excited state, the photon may be absorbed, and the molecule promoted to the higher energy excited state [55]. It is this change which is measured in absorption spectroscopy by the detection of the loss of that energy of radiation from the light.

Unlike infrared absorption, Raman scattering does not require matching of the incident radiation to the energy difference between the ground and excited states. Raman diffusion is closely related to the vibration modes of a substance; since these depend on the mass of the atoms, the bonding forces and symmetries, it results that the Raman spectrum of a substance corresponds to its real fingerprint which allows its unique identification. For the discovery of

this diffusion, which took place in 1928, Sir C.V. Raman was awarded the Nobel Prize in Physics in 1930.

An extraordinary aspect of Raman shift, is that it is not only unique and distinct for each matter, but it remains constant regardless of the wavelength of the source used. This aspect is far from secondary if we think that in gemology, as in many other fields, we are dealing with a multitude of different materials, which often react very differently depending on the energy of the emission used to identify them. Some samples will in fact be easier to identify using a source in the visible spectrum while for others, which may exhibit luminescence when excited at these wavelengths, it may be necessary to use infrared sources.

As mentioned, Raman spectroscopy is a non-destructive, non-contact material characterization method [70]. With the advent of charge coupled device (CCD) cameras, Fourier-transform methods, high quality diffraction gratings, and computer analysis, this technique has become a simple-to-use method for materials characterization. For example, it can be used to measure the stresses in the crystal lattices of certain materials. To do so, a laser is focused on a sample and the incident radiation is scattered by the vibrations of the crystal lattice (phonons). Residual stress in the crystal lattice will cause the phonons to vary proportionally to the strain in the lattice [71]. Thus, a slight shift in the frequency of the scattered spectrum is also observed. This makes Raman spectroscopy an effective way to monitor localized stress in MEMS devices.

Raman spectroscopy can also be used to identify the presence of different atomic bonds and crystalline arrangements. For example, the spectrum for silicon, 6H-SiC, 15RSiC, and 4H-SiC all look different from one another. In this way, a sample can be “mapped” according to what type of material exists at a specific location within the sample. This mapping can be further localized with the use of a microscope and other optics to focus the laser beam excitation source. This is called micro-Raman spectroscopy, where in the beam is focused to a spot size of around 1-3 µm on the sample’s surface.

TEST SETUP AND RESULTS

INTRODUCTION

As already mentioned, Silicon carbide is a wide-band gap semiconductor material which became the most desirable candidate for automotive applications making power transistors with high power density module featuring high blocking voltage and ultra-low conduction resistance due to its better physical properties than silicon such as a wider band-gap of around 3eV, an about ten times higher critical electric field and an about three times higher thermal conductivity.

These features allow higher operation temperature, better efficiency in power conversion, power rate and switching frequency which, combined with very fast process improvement, contributed to make it technologically mature as commercial products.

Unfortunately, the gate oxide weakness, the presence of carbon atoms in the crystal which results in a slow oxide growth rate and the high amount of crystal defects in SiC wafers are currently cutting back the total exploitation of all these performances. As deepen explained on chapters related to defectivity cap. 5, for the next generation of SiC based power devices improvement of quality and technical parameters of devices requires better control of material during the epitaxial growth.

On that phase, crystallographic defects and contaminations may extend into epitaxial layer and wafer surface to form various surface defects, including carrot defects, polytype inclusions, scratches, micropipes, dislocations and grain boundaries, or even convert to produce other defects, leading to detrimental effects on the final SiC device such as critical breakdown electric field reduction, higher leakage currents, and degrade the on-state performance of devices.

Defects such that are then considered to be device-killer since they kill or severely damage the electrical properties of the devices, hence they need to be appropriately characterized and deepen studies on their effect on reliability are needed.

Other non-killer defects such as basal plane dislocations and threading edge dislocations might not kill the electrical properties of the devices but can cause performance degradation and excessive defect induced leakage current.

Usually, they could be activated under transistor on conditions which are related to positive bias on gate electrode.

Moreover, efforts have recently been intensified to characterize the gate oxides also in a condition of negative polarization due to the negative electric field induced, as shown in several simulations, on the gate oxide in a condition of high drain polarization.

On the other hand, in the field of batteries application, negative bias characterization has been required to characterize the accidental case of reversing electrodes polarity.

These are the reasons why, during the past decades, extensive studies have been conducted to understand the impact of major SiC defects, to reduce their amount and to address correctly and efficiently failure analysis related to them.

The starting point obviously, requires a fully and accurate characterization of the most reliability test implemented on standard and defect free devices in order to understand the normal aging of the transistor under accelerated test.

In this context, the 4H-SiC MOSFETs bias temperature instability during long term interdiction including high temperature reverse bias and high temperature gate bias are the routinely performed. Which is done to ensure the reliability aspect of the devices operating in high temperature and voltage to accelerate degradation induced by latent extended or point defectivity, which are not detected at parametric and functionality test. The purpose of each test is, for the former to check the integrity of the junction, the weakness due to crystal defectivity in the field depletion structure, known as JFET area, or at the edge termination and for the latter the drift of electrical parameters related to charge trapping at SiC/SiO_2 interface, bulk oxide traps in the gate oxide [72]. The main issue in failure analysis is often the addressing after an irreparable damage to the structure which is the usual output of a standard reliability test such as HTRB and HTGB. The results will confirm how defectivity is detrimental to device reliability under HTRB test inducing sudden breakdown which, according to the simulation are located at device edge although In-depth studies are still

underway to understand whether some types of extended defects are sensitive to charge trapping and therefore induce parametric drift during stress before hard failure [73].

Therefore, the main topics of this chapter are:

1. Perform the numerical simulation to obtain information about the equivalence, in terms of electric field, between a negative HTGB and a HTRB stress
2. Provide a graphical distribution of the electric field and the most critical points into the device cross section suggesting the worst-case stress under different polarities
3. Test and measurement's purpose is to confirm, on several "defect-free" devices, the hypothesis deduced from simulation that showed the real aging and the parameter drifting under stress
4. Test several defected devices to understand if the extended defects are electrically active and/or also if they include contamination and energy levels in the band gap being subjected to progressive degradation or, otherwise, being not related to point defects, to a sudden breakdown
5. Carry out a Raman Spectroscopy electrical characterization on the most common defects of 4H-SiC epitaxy

PRELIMINARY ELECTRICAL CHARACTERIZATION

In order to provide the correct information to extrapolate TCAD simulation of a real 4H-SiC PowerMOSFET which operates in the Drain Voltage regime of 650V, a preliminary characterization at bench level has been performed to calculate the correspondent gate oxide field related to a high drain voltage condition: firstly I-V measurement have been performed on vertical MOSFETs operating in gate-controlled-diode (GCD) configuration. In this operation mode, the source, drain and body electrodes of the MOSFETs are grounded, while the gate electrode becomes the anode of the GCD. In this way the majority carriers (electrons) are supplied under positive bias from the n-type region (source and drain) and on the other hand, under negative bias, the holes are injected from the p-body. Secondary, a BVdss characterization has been performed sweeping drain electrode grounding source and gate, setting the transistor in off condition until the D-S junction breakdown to define the HTRB and HTGB stress conditions.

By the Ig-Vg characteristics, obtained sweeping gate electrode from -50V to 50V (see figure 34) it is possible also to extrapolate the potential barrier (mandatory data for TCAD simulations) on both interfaces to SiC and Polysilicon to gate oxide, by a Fowler-Nordheim plot using the well-known equations:

$$J = A(E_{ox})^2 e^{-\frac{B}{E_{ox}}}$$

EQUATION 47

With:

$$A = \frac{q^3}{8\pi h}\frac{m_0}{m_{ox}(\Phi_B)} = 2.46 * 10^{-25}\frac{m_0}{m_{ox}\Phi_B}(A * V^{-2})$$

EQUATION 48

And:

$$B = \frac{8\pi\sqrt{2m_{ox}}}{3hq}(\Phi_B)^{\frac{3}{2}} = 1.05 * 10^{38}\left(\frac{m_{0x}}{m_o}\right)^{\frac{1}{2}}(\Phi_B)^{\frac{3}{2}}(V * cm^{-1})$$

EQUATION 49

Where q is the electronic charge, h Planck constant, Φ_B sis the barrier height at electrode/oxide interface, m electron mass at vacuum and m_{ox} electrons mass average.

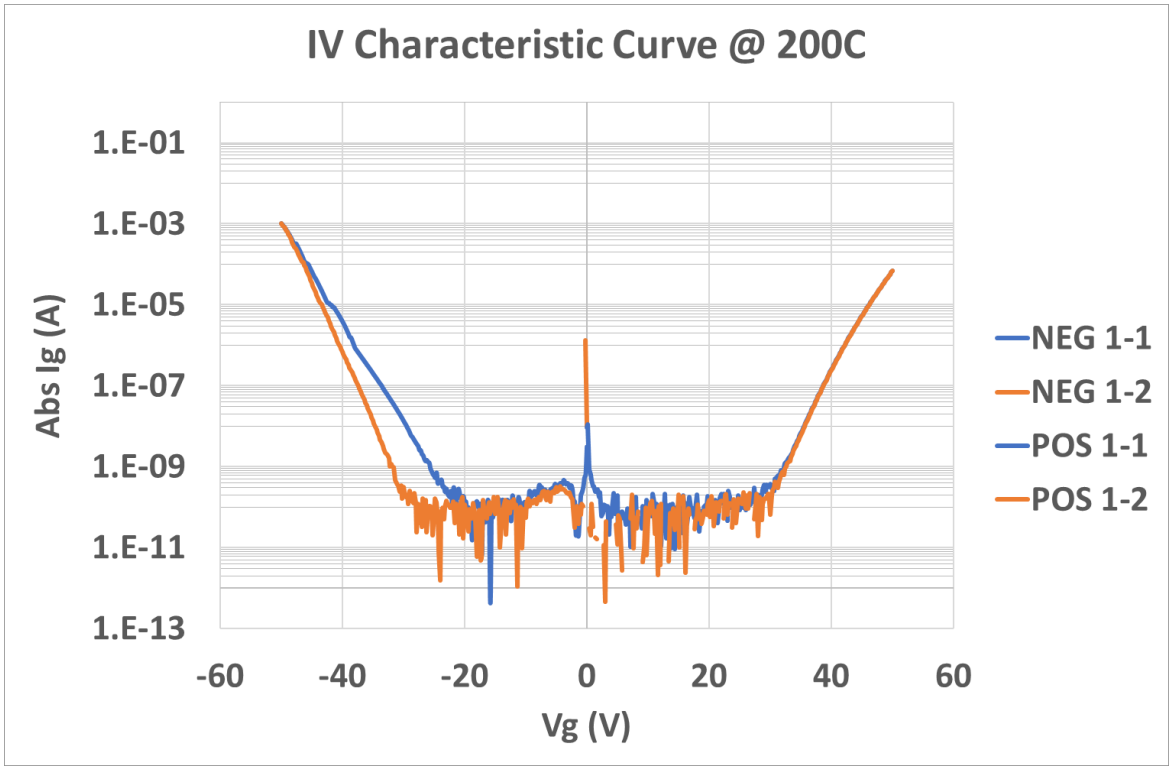

FIGURE 34. IV CHARACTERISTIC CURVE @ 200C.

In the same picture it is possible to extrapolate the F-N Voltage onset under positive and negative bias which is around 36V and -18.5V. The test has been repeated two times under negative and positive voltage in order to exclude trapping effect at SiC/SiO_2 interface especially under negative bias.

The second characterization, showed in figure 35, is a BVdss under off conditions sweeping drain from 0 to 930V, in off conditions (Vg=0) with a maximum allowed current of around 40mA.

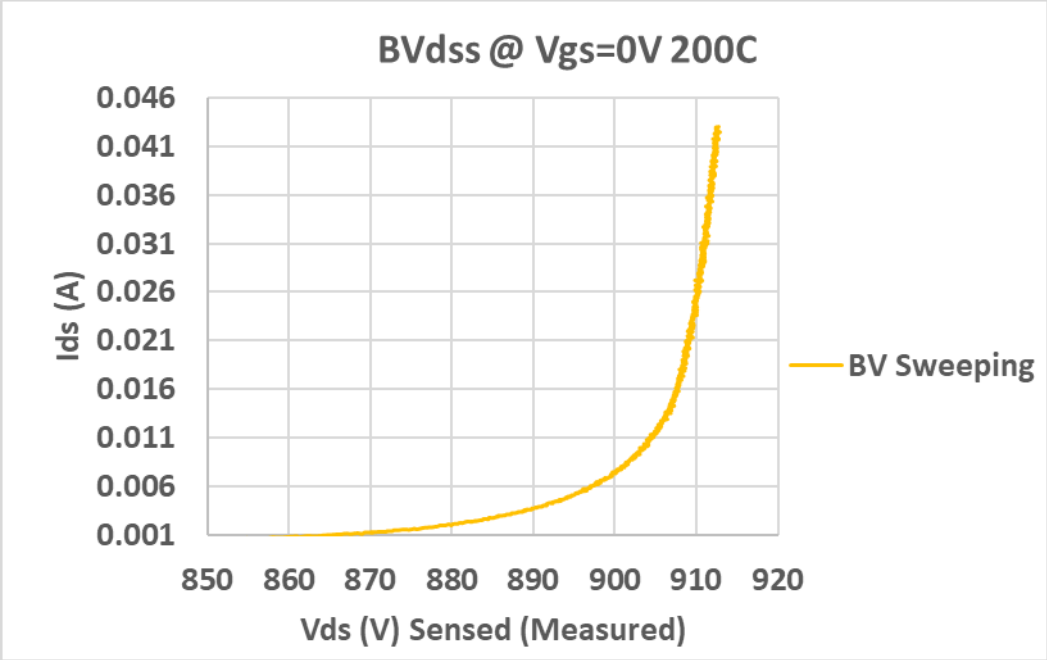

FIGURE 35. BDDSS @ 200C.

NUMERICAL TCAD SIMULATION

According to the second point of the introduction, we needed to understand the physical impact of a reliability test on the transistor robustness and the role of the point of the application of the gate oxide field rather than its absolute value. For this purpose, we performed a numerical TCAD simulations in terms of electric field and minority carrier distribution, to calculate the equivalent negative field induced by HTRB test on PowerMOSFET gate oxide. The half-cell structure of SiC vertical MOSFET is presented in figure 36. Static 2D TCAD physical simulations were carried out to show the electric field (E) distribution near the SiC-SiO_2 under HTRB and HTGB conditions. Although the absolute value of the electric field induced on the gate oxide is the same, under HTGB negative bias, the field lines behavior at source/body interface (where the channel is created) highlights the electrical field is much higher than in the drift region (which is the large n-type area where electrons flow in on conditions). The above may be attributed to the mismatch in the dielectric constant of the oxide and the semiconductor. An opposite behavior was found in the case of the HTRB test where the maximum electric field occurs in the drift region, and it is almost zero in the source/body region.

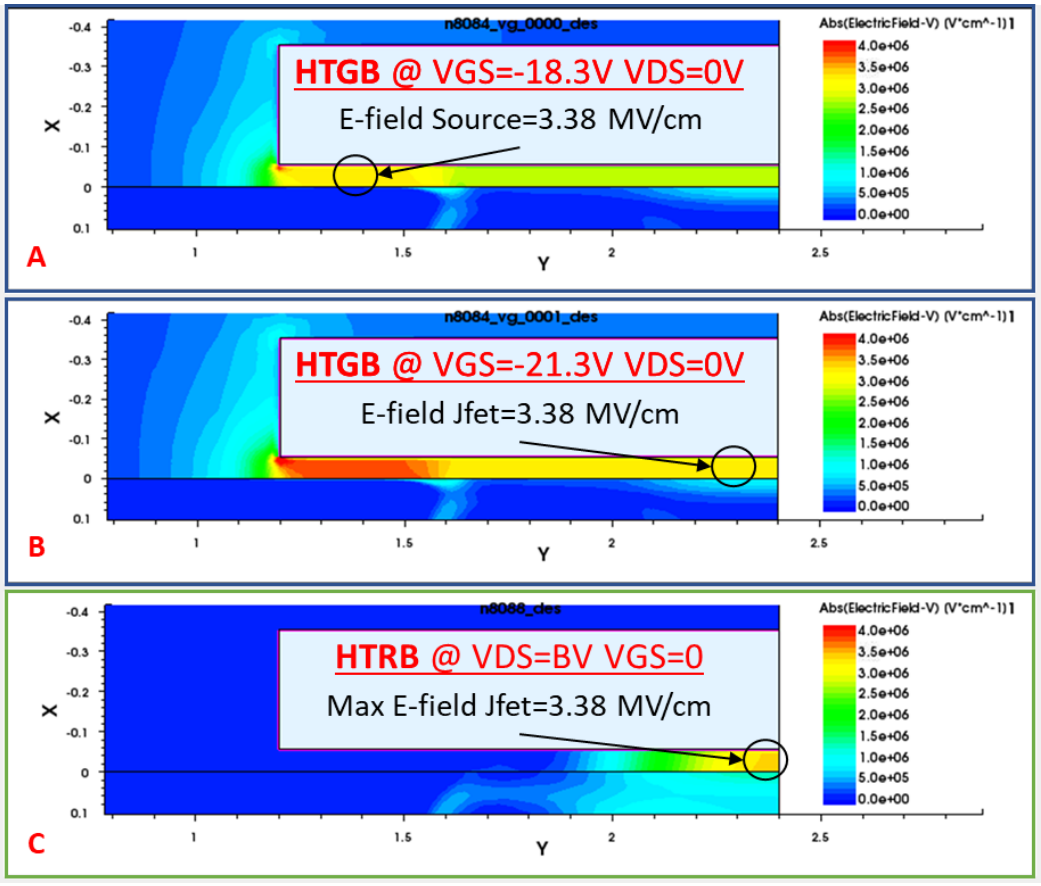

FIGURE 36. SIMULATION OF THE GATE OXIDE FIELD UNDER HTGB (A-B)AND HTRB (C) CONDITIONS.

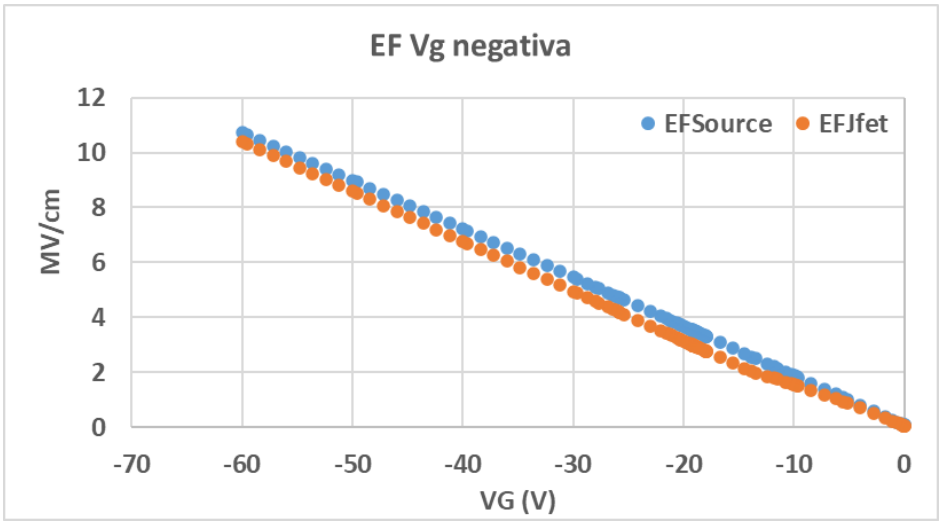

FIGURE 37. ELECTRIC FIELD IN FUNCTION OF VG NEG FOR SOURCE E JFET REGIONS.

This result allows to understand the real effect of these two different stresses in the above polarization conditions. Also, as listed in the first point of the introduction, to find the equivalence between a negative HTGB and a HTRB stress in terms of electric field. Then, as anticipated on point 3 of the introduction, an experimental validation of the simulation is required, searching for the most sensitive parameter to drift under stress conditions. Hence, particular focus was placed on the drift of some key parameters of the transistor such as leakage (Igss and Idss), conduction in the oxide (Vfn+ and Vfn- Fowler-Nordheim Voltage onset by electrons and holes current) the Drain-Source Breakdown (BVdss) the transistor threshold, the Vdson and the Vfec (direct bias of the Body-Drain diode).

ROUTINE DEVELOPMENT

In order to induce significant drift in the selected parameters during stress, a measure/stress cycling routine has been developed under Keysight Easy Expert, which allowed to control the Keysight B1505 device analyzer and the HV MPI-TS2000DP semiautomatic probe-station to perform wafer level measurements at temperature of 200C.

Hence under highly accelerated pulsed HTRB conditions, very close to the drain-source breakdown voltage, it is possible to sense, every 30 minutes until 40 hours of stress, several electrical parameters in order to find the worst case and/or the most sensitive parameter to be drifted [74] [75].

Besides, the equivalent pulsed negative High Temperature Gate Bias has been carried out on other samples and the drift induced by both stress on threshold and Fowler-Nordheim instability, compared, investigated and illustrated, providing the net charge injected during stress and the centroid position of the maximum trapped charge inside the gate oxide bulk.

The advantage of this routine is to combine different measure and stress conditions and a schematic of the test and sequence procedures have been reported in figure 41.

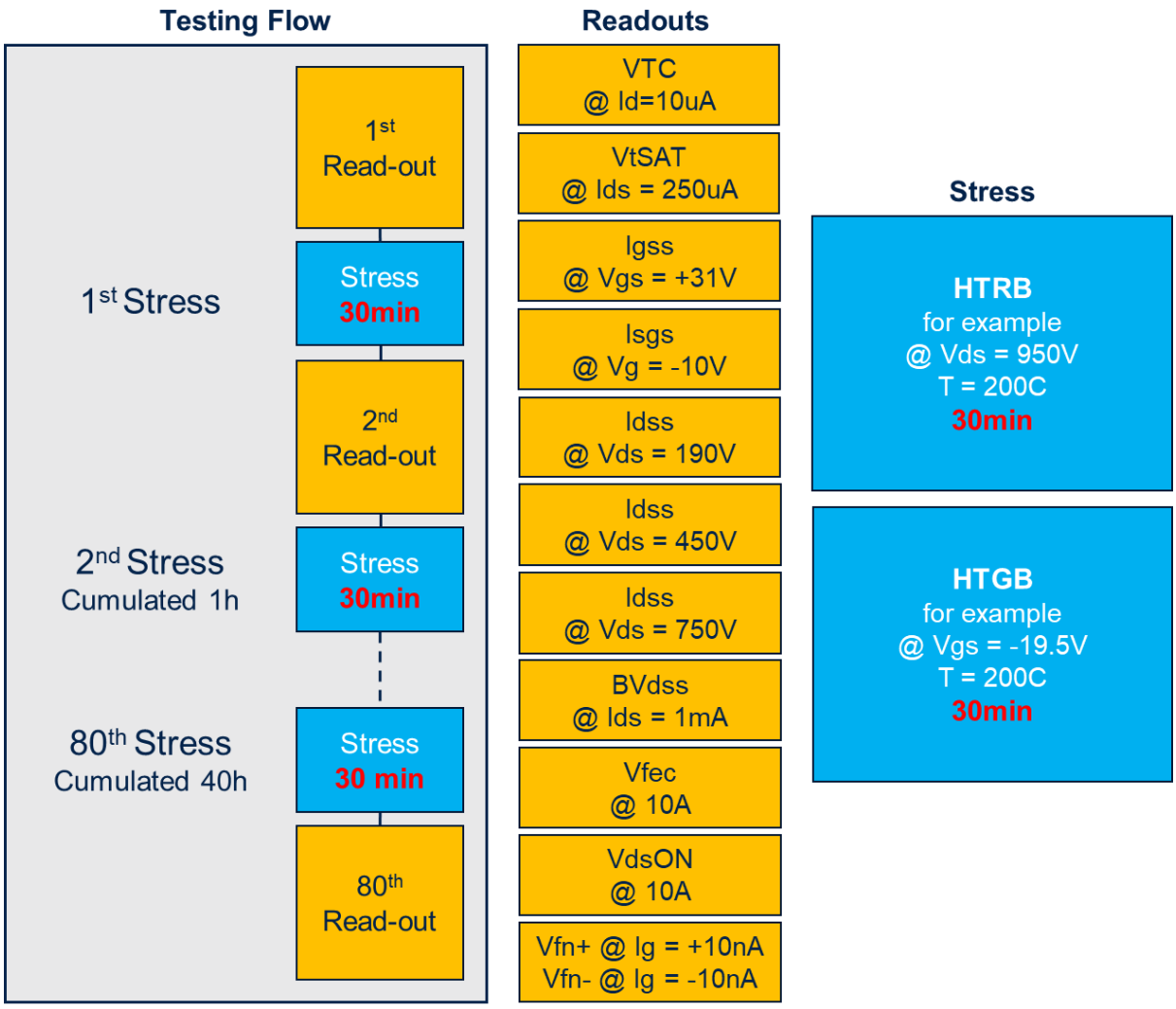

FIGURE 38. STRESS CYCLING PROCEDURE. WITH OUR ROUTINE IT IS POSSIBLE TO SELECT OR DESELECT EACH READOUT MODULE AND TO CHANGE THE STRESS TYPE OR CONDITION FROM HTRB TO HTGS OR WITH A COMBINATION OF BOTH.

TEST SETUP AND STRESS PULSE CHARACTERIZATION

In order to easily switch from High Voltage to High Current test a module Selector Keysight N1258A has been put between the inputs (B1505 sources) and the outputs (TS2000-DP probe-heads and then transistor connectors).

The introduction of the module N1266A, which allowed to stress under HTRB conditions at the voltage of 960V and leakage current of 33mA in pulsed mode, solved another issue brought by the need to accelerate the parameter drifting within 40 hours of stress and, consequently, to overcome the 8mA limitations of the Keysight HV module at about 1kV. Figure 39 reports the used configuration.

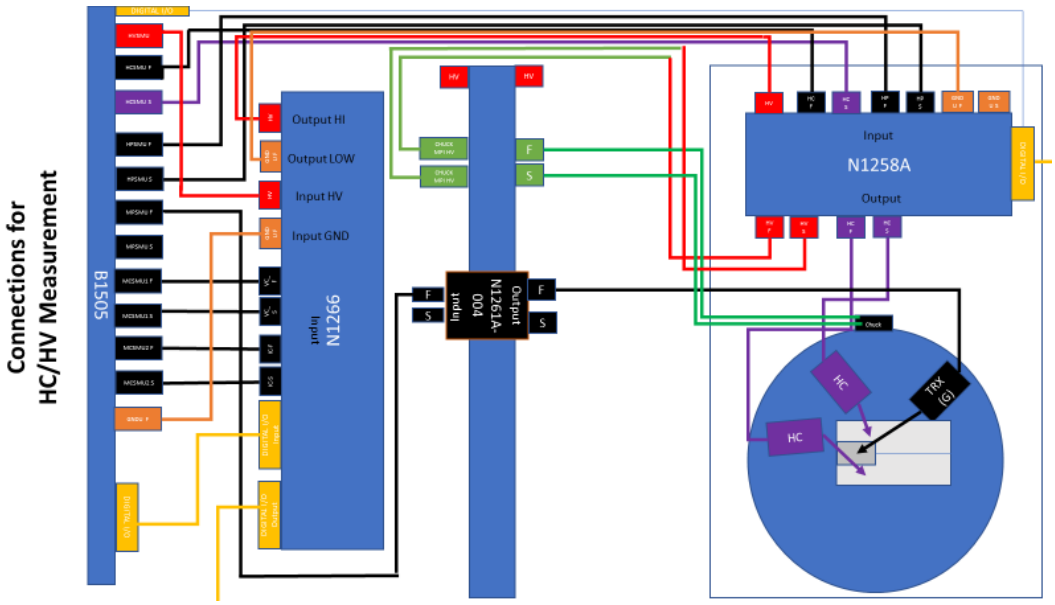

FIGURE 39. TEST SETUP AND SYSTEM CONFIGURATION SCHEMATIC.

The pulse characterization was achieved by connecting an oscilloscope with an HV probe in series with the output of the resources. Although the N1266 module provides for a maximum impulse of 1ms, the wiring system's impedance and the resulting misalignment between the forced voltage and the actual applied voltage have caused the impulse to be reduced to 500us. As shown in figure 40, the overall testing period consists of 5ms (4.5ms signal shutdown and 0.5ms pulse).

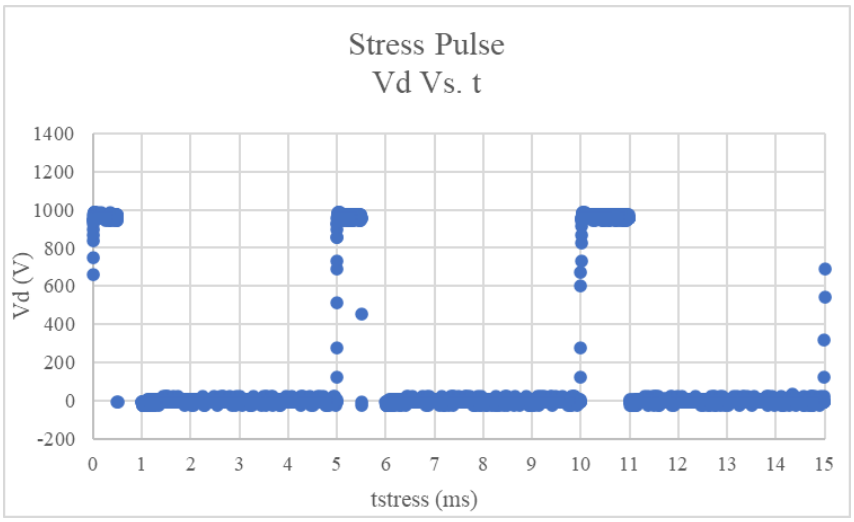

FIGURE 40. STRESS PULSE CHARACTERIZATION.

Each stress consists of 1000 pulses with a 5ms period, repeated 360 times for a total stress time of 1800s as shown in the blue boxes in figure 38.

SAMPLES UNDER TEST SELECTION

The Power MOSFET transistors that we characterized in this work are built on 6" wafers on n-type (0001) 4H-SiC 180µm thick substrate doped 4-5E18 cm^{-3} and resistivity of 0.012 - 0.025Ω*cm. The n-epitaxy layer is 12µm thick and doped 8E15 cm^{-3} and is grown in a warm wall multi-wafer CVD reactor. Over the Epi Layer a 50-nm-thick oxide has been deposited, through a Low-Pressure Chemical Vapor Deposition (LPCVD DCS) in High Temperature Oxidation (HTO) furnace under dichlorosilane (SiH_2Cl_2) ambient and a Post Oxidation Annealing (POA) using NO as gaseous precursor.

For this study anomalous wafers due to a high defectivity have been selected and scrapped from the production (see figure 41). These samples allow an accurate selection of good and defect free devices by superimposing defectivity maps at epitaxial layer to the final EWS map (Electrical Wafer Testing). They could be normally intended for sale, but at the same time immersed in an anomalously defective substrate that makes the devices themselves doubtful from a reliability point of view.

First, the materials have been inspected at the start of the process in order to choose devices that, at this stage of analysis, don't have epitaxial defectivities, which are known to be killer.

For this purpose, we perform an inspection at epitaxy level with Candela 8520 by KLA-Tencor scan which allowed to detect surface defects such as droplet, carrots, triangles, micropits, etc.). Another inspection has been performed in next level, by KLA Altair inspection microscope, after an appropriate mask level which define the final devices dimension. In order to detect the exact position of the defect within the device which, at the end of the process, superposing defectivity and EWS (Electrical Wafer Sorting) map look electrically aligned to the product specification.

The overlay of the defects and EWS maps allow to detect the position of defects free devices, i.e. the ones aligned with the commercial product specifications.

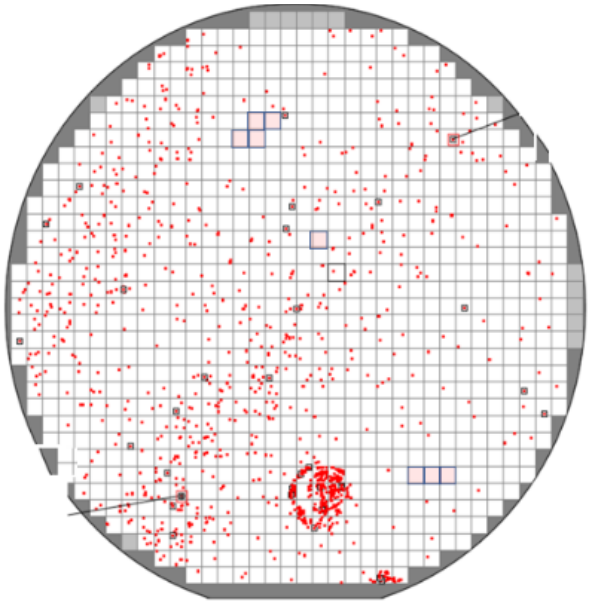

FIGURE 41. DEFECTIVITY MAP AT EPITAXIAL INSPECTION LEVEL. IN PINK THE TESTED DEVICES DEFECT FREE AND GOOD AT FINAL TEST.

HTRB Test On Defect Free Devices

The findings of a preliminary characterization of the devices intended to be stressed in the HTRB test are shown in tables 4 and 5, which are organized separately for leakage values and other parameters.

In particular we can see from the table 4 the characteristics Igss and Idss leakage of the defect free devices before stress and in in the table 5 is shown the parametric values (Vth, Vfn, BVdss…) for the same devices in the same conditions.

	Leakage Data before 40hours HTRB stress @ 200C, Vds = +890V						
	Num. Def @ Epitaxial Inspection	Subthreshold Leakage (A) @ Vgs = 0V Vds = 0.1V	Igss (A) @ Vgs = +32V	Isgs (A) @ Vgs = -10V	Idss (A) @ Vds = +190V Vgs = 0V	Idss (A) @ Vds = +450V Vgs = 0V	Idss (A) @ Vds = +750V Vgs = 0V
DEV34-Wf 01	0	1.80E-07	1.36E-09	-7.56E-11	2.35E-06	8.91E-06	6.70E-05
DEV37-Wf 01	0	1.93E-07	9.78E-10	-2.01E-11	2.50E-06	9.04E-06	6.37E-05
DEV19-Wf 02	0	2.95E-08	1.70E-10	-3.53E-10	1.27E-07	4.72E-07	3.53E-05
DEV20-Wf 02	0	2.29E-08	2.59E-10	-4.41E-10	1.31E-07	4.61E-07	3.43E-05

TABLE 4. GATE AND DRAIN LEAKAGE IN OFF CONDITIONS BEFORE HTRB TEST.

	Parametric Data before 40hours HTRB stress @ 200C, Vgs = +890V									
	Num. Def @ Epitaxial Inspection	GmMax (S)	Vth (V) @ GmMax (Vds = 0.1)	Vth (V) @ Ids = 5uA (Vds = 0.1V)	Vfn+ (V) @ Ig = +10nA	Vfn- (V) @ Ig = -10nA	Vth (V) @ Ids = 250uA (G & D Shorted)	BVdss (V) @ Ids = 1mA (G & S Grounded)	Vfec (V) @ Ids = -10A (Forward Body/Drain Diode)	VdsOn (V) @ Ids = +10A, Vds = +18V
DEV34-Wf 01	0	1.54E-03	3.406	0.523	33.42	-17.30	1.10	879.11	-1.56	0.131
DEV37-Wf 01	0	1.55E-03	3.544	0.510	33.58	-17.78	1.10	881.43	-1.56	0.143
DEV19-Wf 02	0	1.45E-03	3.740	0.814	36.00	-18.59	1.40	853.08	-1.68	0.132
DEV20-Wf 02	0	1.42E-03	3.599	0.842	35.82	-18.14	1.40	853.34	-1.70	0.135

TABLE 5. VARIOUS PARAMETER RELATED TO CHANNEL AND GATE OXIDE BEFORE HTRB TEST.

In order to find the parameter more sensitive to HTRB test, a drift analysis of each parameter has been carried out as shown on tables 6 and 7. Table 6 reports the ratio between the values of the parameters at time *t=40h* and at *t=0h* (without stress), while table 7 shows the shift of the parameters divided by the value of the parameter at *t=0h*.

	Drift Analysis after 40hours HTRB stress @ 200C, Vds = +890V ((Value (t)/(Value(0))						
	Num. Def @ Epitaxial Inspection	Subthreshold Leakage (A) @ Vgs = 0V Vds = 0.1V	Igss (A) @ Vgs = +32V	Isgs (A) @ Vgs = -10V	Idss (A) @ Vds = +190V Vgs = 0V	Idss (A) @ Vds = +450V Vgs = 0V	Idss (A) @ Vds = +750V Vgs = 0V
DEV34-Wf 01	0	1.16E+00	2.95E-01	3.88E+00	1.00E+00	1.01E+00	1.00E+00
DEV37-Wf 01	0	1.23E+00	6.22E-01	1.96E+00	1.08E+00	1.07E+00	1.04E+00
DEV19-Wf 02	0	1.32E+00	-4.05E-01	1.18E+00	1.54E+00	1.27E+00	9.82E-01
DEV20-Wf 02	0	1.02E+00	3.12E-01	5.84E-01	1.03E+00	1.00E+00	9.85E-01

TABLE 6. LEAKAGE DRIFT (I(T)/I(0)) AFTER 40H HTRB STRESS.

	Drift Analysis after 40hours HTRB stress @ 200C, Vds = +890V ((Value (t)/(Value(0))									
	Num. Def @ Epitaxial Inspection	GmMax (S)	Vth (V) @ GmMax (Vds = 0.1)	Vth (V) @ Ids = 5uA (Vds = 0.1V)	Vfn+ (V) @ Ig = +10nA	Vfn- (V) @ Ig = -10nA	Vth (V) @ Ids = 250uA (G & D Shorted)	BVdss (V) @ Ids = 1mA (G & S Grounded)	Vfec (V) @ Ids = -10A (Forward Body/Drain Diode)	VdsOn (V) @ Ids = +10A, Vds = +18V
DEV34-Wf 01	0	9.72E-01	0.990	0.989	1.01	1.07	1.00	1.00	1.00	0.977
DEV37-Wf 01	0	9.74E-01	1.031	0.950	1.01	1.05	1.00	1.00	1.00	1.019
DEV19-Wf 02	0	9.52E-01	1.180	1.014	1.01	1.06	1.00	1.00	1.00	0.968
DEV20-Wf 02	0	9.84E-01	1.173	1.010	1.01	1.07	1.07	1.00	1.01	0.967

TABLE 7. PARAMETER DRIFT (VALUE(T=40HRS)/VALUE(0))/VALUE(0)).

It is evident that Threshold voltage and Fowler-Nordheim voltage under negative bias (holes injection from p-body) are more sensitive to the stress while the drift of the other parameters is almost negligible.

HTGB Test On Defect Free Devices

The same preliminary characterization, performed before HTRB stress, have been implemented to devices dedicated to HTGB stress. Results are collected on Tables 8 and 9.

	Leakage Data before 40hours HTGB stress @ 200C, Vgs = -19.5V						
	Num. Def @ Epitaxial Inspection	Subthreshold Leakage (A) @ Vgs = 0V Vds = 0.1V	Igss (A) @ Vgs = +32V	Isgs (A) @ Vgs = -10V	Idss (A) @ Vds = +190V Vgs = 0V	Idss (A) @ Vds = +450V Vgs = 0V	Idss (A) @ Vds = +750V Vgs = 0V
DEV34-Wf 01	0	2.86E-07	9.03E-10	9.40E-11	3.75E-06	1.39E-05	8.98E-05
DEV37-Wf 01	0	1.93E-07	2.47E-09	-1.66E-10	2.20E-06	7.92E-06	6.08E-05
DEV21-Wf 02	0	1.66E-08	3.50E-10	1.45E-10	7.84E-08	3.37E-07	4.70E-05
DEV22-Wf 02	0	3.50E-08	5.47E-10	1.57E-10	1.91E-07	7.08E-07	4.10E-05

TABLE 8. GATE AND DRAIN LEAKAGE IN OFF CONDITIONS BEFORE HTGB TEST.

	Parametric Data before 40hours HTGB stress @ 200C, Vgs = -19.5V									
	Num. Def @ Epitaxial Inspection	GmMax (S)	Vth (V) @ GmMax (Vds = 0.1)	Vth (V) @ Ids = 5uA (Vds = 0.1V)	Vfn+ (V) @ Ig = +10nA	Vfn- (V) @ Ig = -10nA	Vth (V) @ Ids = 250uA (G & D Shorted)	BVdss (V) @ Ids = 1mA (G & S Grounded)	Vfec (V) @ Ids = -10A (Forward Body/Drain Diode)	VdsOn (V) @ Ids = +10A, Vds = +18V
DEV34-Wf 01	0	1.55E-03	3.165	0.446	33.68	-17.59	1.00	879.82	-1.52	0.130
DEV37-Wf 01	0	1.54E-03	3.456	0.510	32.98	-17.38	1.10	878.16	-1.56	0.133
DEV21-Wf 02	0	1.48E-03	4.033	0.891	36.21	-18.41	1.50	840.66	-1.70	0.130
DEV22-Wf 02	0	1.42E-03	3.728	0.820	35.46	-18.55	1.40	844.32	-1.70	0.128

TABLE 9. VARIOUS PARAMETER RELATED TO CHANNEL AND GATE OXIDE BEFORE HTGB TEST.

Tables 10 and 11 shows a drift analysis before HTGB stress.

	Drift Analysis after 40hours HTGB Stress @ 200C, Vgs = -19.5V						
	Num. Def @ Epitaxial Inspection	Subthreshold Leakage (A) @ Vgs = 0V Vds = 0.1V	Igss (A) @ Vgs = +32V	Isgs (A) @ Vgs = -10V	Idss (A) @ Vds = +190V Vgs = 0V	Idss (A) @ Vds = +450V Vgs = 0V	Idss (A) @ Vds = +750V Vgs = 0V
DEV34-Wf 01	0	1.49E+00	4.86E-01	-4.03E-01	7.83E-01	7.80E-01	8.36E-01
DEV37-Wf 01	0	1.72E+00	2.02E-01	2.16E+00	9.46E-01	9.55E-01	9.61E-01
DEV21-Wf 02	0	2.40E+00	5.46E-01	-1.06E-01	5.71E-01	7.78E-01	9.95E-01
DEV22-Wf 02	0	1.31E+00	8.10E-01	-1.79E+00	7.63E-01	8.18E-01	9.82E-01

TABLE 10. LEAKAGE DRIFT (I(T)/I(0)) AFTER 40H HTGB STRESS.

	Drift Analysis after 40hours HTGB stress @ 200C, Vgs = -19.5V									
	Num. Def @ Epitaxial Inspection	GmMax (S)	Vth (V) @ GmMax (Vds = 0.1)	Vth (V) @ Ids = 5uA (Vds = 0.1V)	Vfn+ (V) @ Ig = +10nA	Vfn- (V) @ Ig = -10nA	Vth (V) @ Ids = 250uA (G & D Shorted)	BVdss (V) @ Ids = 1mA (G & S Grounded)	Vfec (V) @ Ids = -10A (Forward Body/Drain Diode)	VdsOn (V) @ Ids = +10A, Vds = +18V
DEV34-Wf 01	0	9.05E-01	1.177	0.955	1.01	1.16	1.10	1.00	1.03	1.014
DEV37-Wf 01	0	8.93E-01	1.016	0.906	1.03	1.15	1.09	1.00	1.02	0.990
DEV21-Wf 02	0	9.14E-01	1.105	0.994	1.01	1.11	1.07	1.00	1.02	1.017
DEV22-Wf 02	0	9.32E-01	1.101	1.000	1.02	1.10	1.07	1.00	1.01	0.988

TABLE 11. PARAMETER DRIFT (VALUE(T=40HRS)/VALUE(0))/VALUE(0)).

At the end a comparison of the threshold voltage drift of HTRB stressed devices and negative equivalent bias under HTGB stress has been carried out (figure 42) [76].

The notation used in the next representation and figures are the following:

- In blue the HTGB (or HTGS) stress
- In red the HTRB stress
- Solid line for the first wafer under test
- Dashed line for the second wafer under test

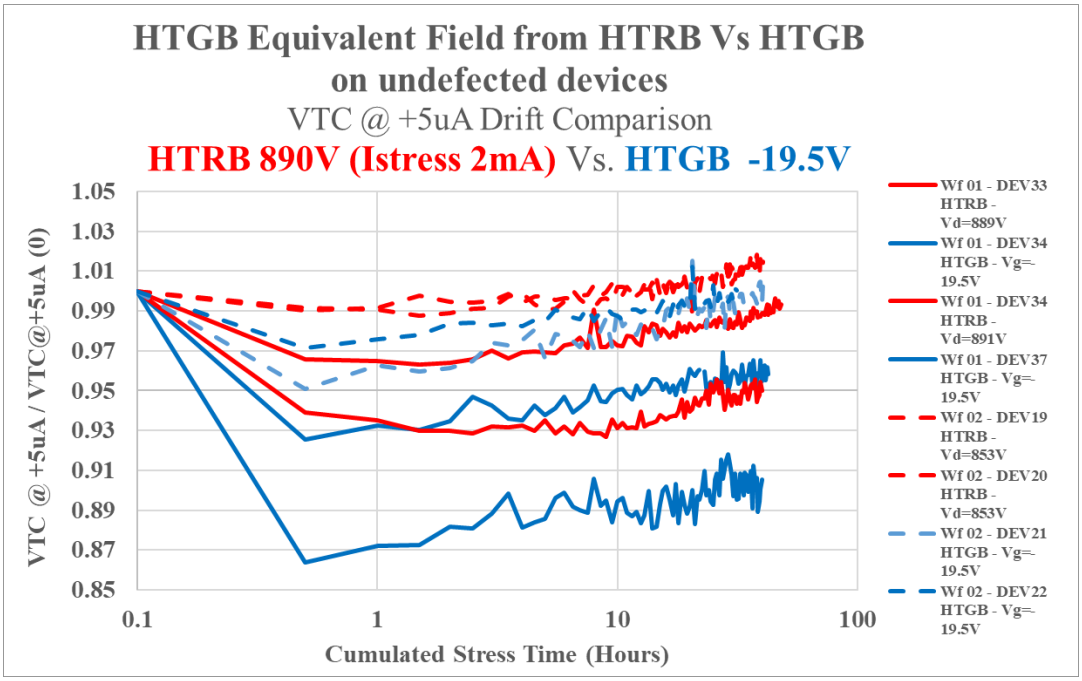

FIGURE 42. THRESHOLD VOLTAGE DRIFT UNDER HTRB (RED) AND HTGB (BLUE) STRESS.

On both wafers the threshold decreasing on the two blue samples (stressed under HTGB conditions) seem to be higher than the red ones (stressed under HTRB conditions). This is usually related to negative charges or holes trapping in the gate oxide. In order to confirm this result, the drift analysis on negative F-N voltage onset has been shown on figure 43. Here the result is more evident, and the F-N voltage shift is higher on the HTGB stressed samples.

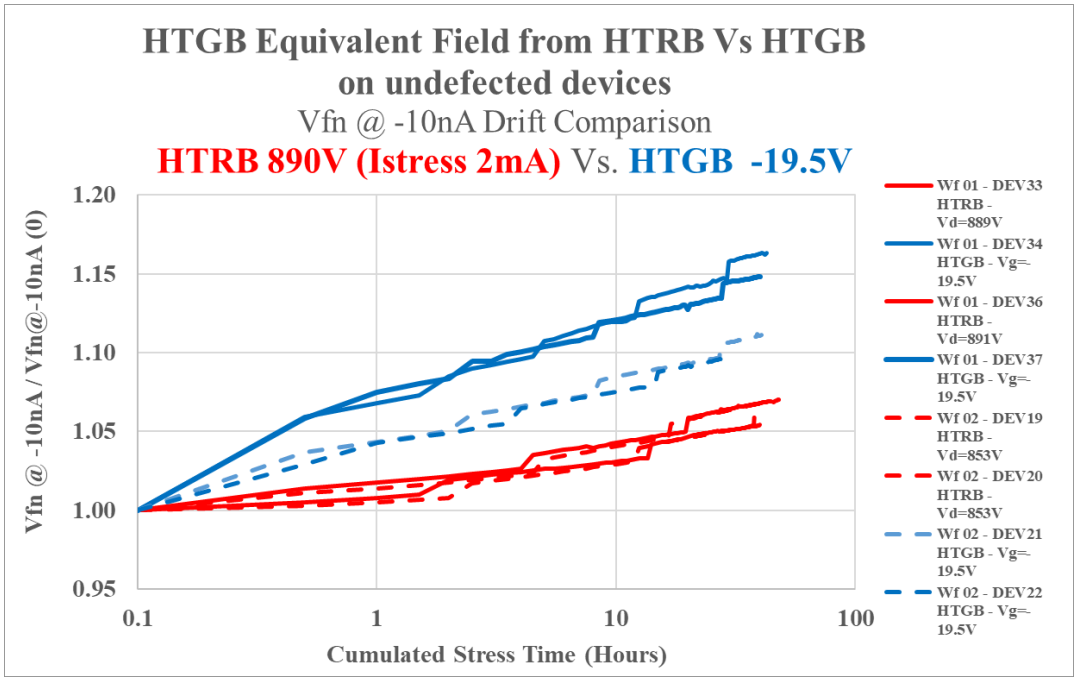

FIGURE 43. NEGATIVE F-N VOLTAGE DRIFT UNDER HTGS (BLUE) AND HTRB (RED) STRESS.

In order to support and confirm this result, the calculation by the charge sensing techniques, based on F-N voltage shift under negative and positive bias, has been performed.

The F-N voltages shift is commonly used to track and spatially locate the trapped charges (both positive and negative) in the gate oxide bulk and is able to also track the trapped charge as a function of the injected electron fluence at SiC/SiO_2 interface.

The estimated trapped charge and the position of the charge centroids, as function of the cumulated current stress time following the method shown by DiMaria and Stasiak [77] is shown in figure 44. Here, the charge sensing method probes the charge centroid for the samples stressed under HTGS and HTRB near the interface. The figure 44 represents an ideal gate oxide cross section between SiC and the poly-silicon contact. In the figure 45 we have a confirmation of the higher trapped charge in gate oxide under HTGB negative bias.

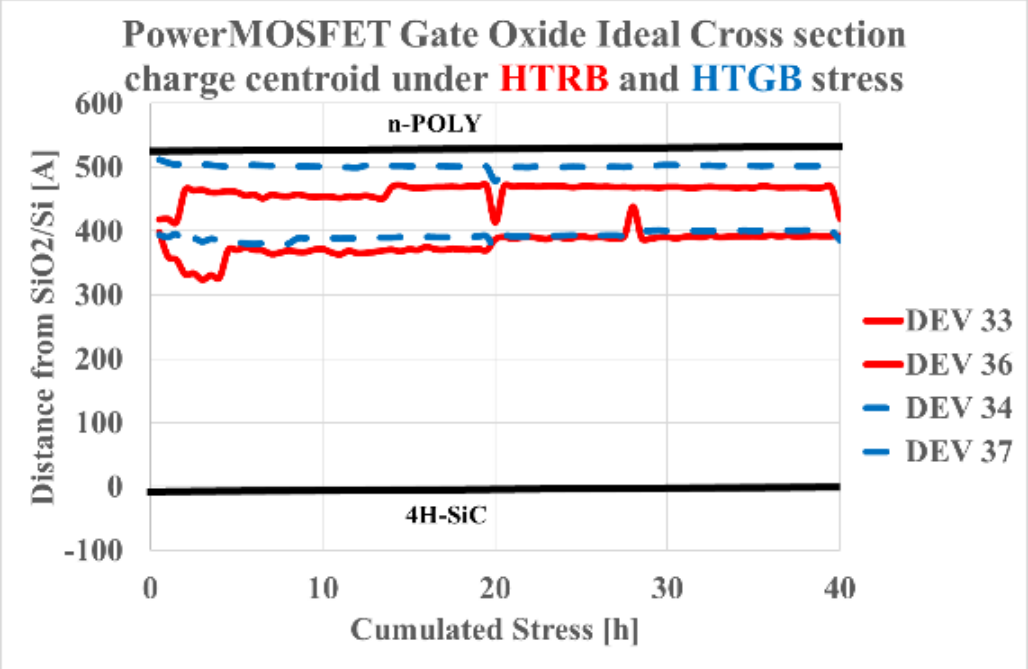

FIGURE 44. CHARGE CENTROID ON THE IDEAL 4H-SIC GATE OXIDE CROSS SECTION.

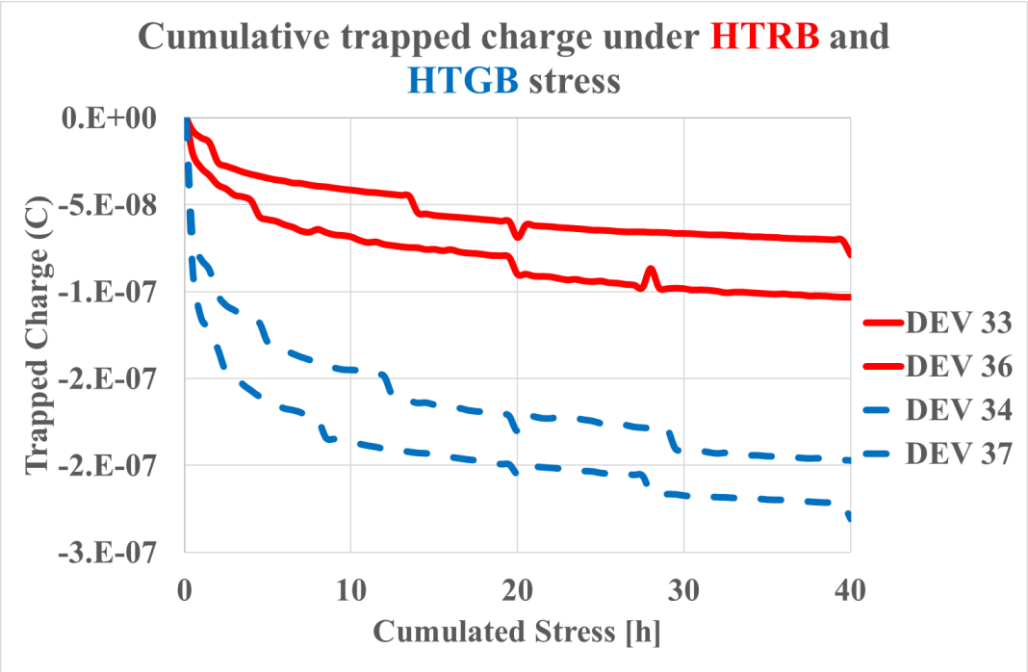

FIGURE 45. CUMULATIVE TRAPPED CHARGE UNDER HTRB AND HTGB STRESS.

DATA/RESULTS AND DISCUSSION: ADDITIONAL ANALYSIS

HTRB TEST ON DEFECT FREE DEVICES

As the wafer under test was particularly defected and anomalous for the standard production the aim of this analysis was to characterize with more details defect free devices in order to catch weak signals coming from the drift analysis of the parameters indicated above.

For this reason, several defects free devices have been stressed under HTRB worst case conditions (930V, 200C vs. previous characterization 890V, 200C).

The highly accelerated tests show a different behavior on these samples (see figures 46 and 47) which, as suggested by some works [73] [78] , could be related to trapping at SiC/SiO_2 interface, energy levels in SiC bandgap or points defect not detected at inspection level. They are small variations which don't affect reliability but highlight what we expected on an anomalous device trapping properties and characterization.

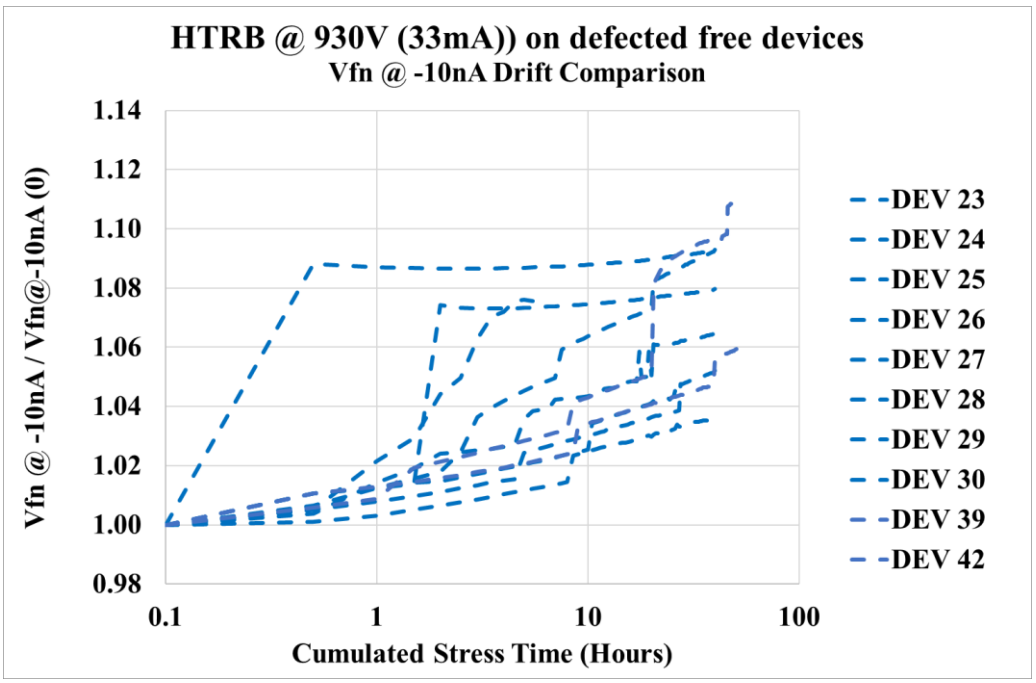

FIGURE 46. NEGATIVE F-N VOLTAGE DRIFT UNDER HTRB STRESS.

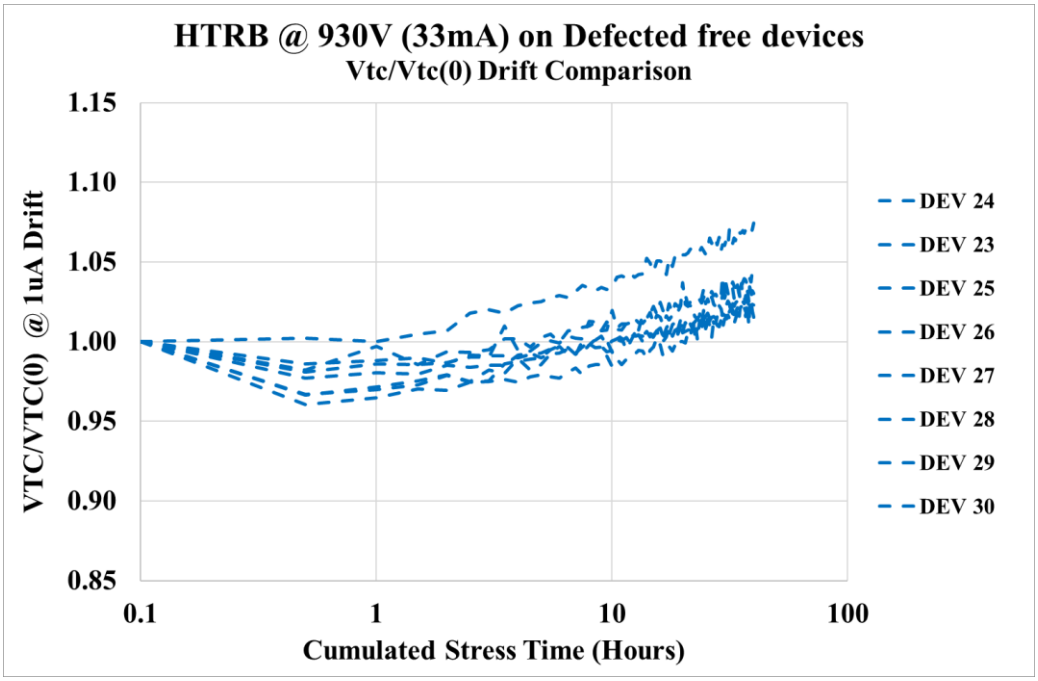

FIGURE 47. VTC DRIFT UNDER HTRB STRESS.

HTRB And Effect On Defected Devices

The fourth point of the thesis outline introduces the same characterization and HTRB stress performed on devices on which defectivity have been detected at epitaxial inspection level.

Figures 48 and 49 demonstrate that there is no relationship between the threshold voltage of defective and defect-free devices and their Negative Fowler-Nordheim onset.

In other words, the defected DUTs don't seem to show any electrical activation induced by the stress. This result has been confirmed on a higher sample population.

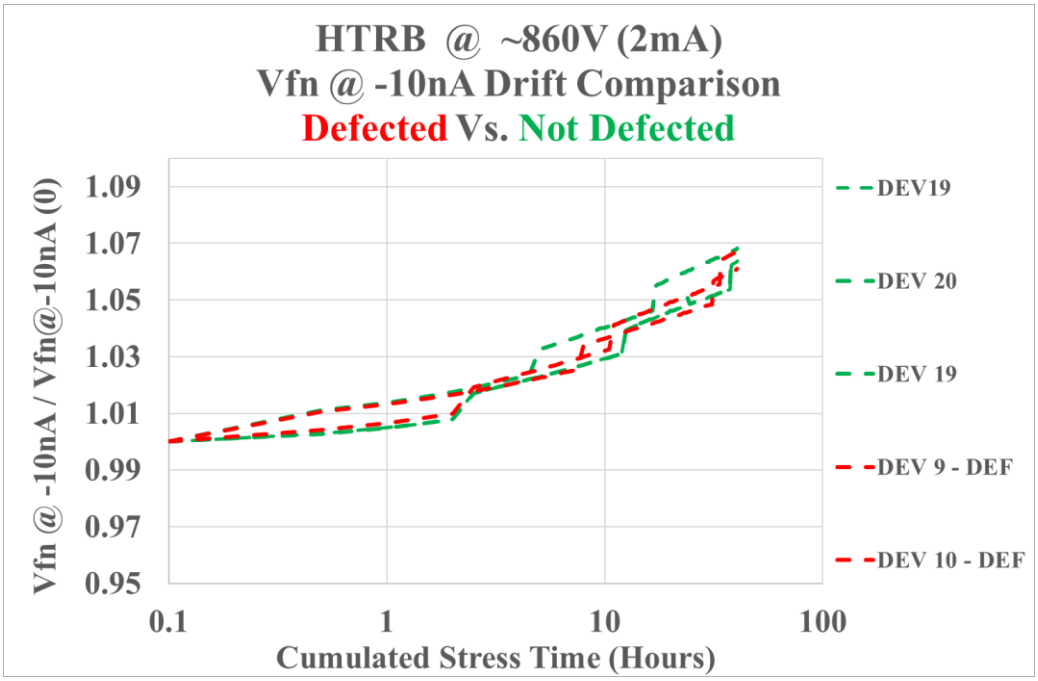

FIGURE 48. NEGATIVE FOWLER NORDHEIM ONSET DRIFT UNDER HTRB STRESS.

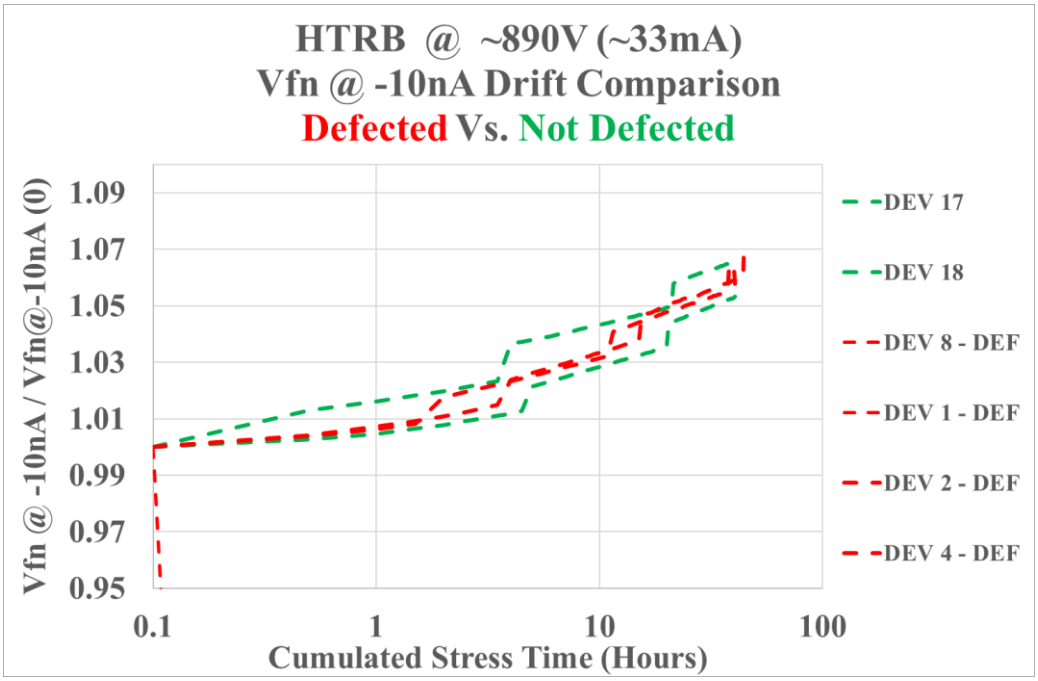

FIGURE 49. NEGATIVE FOWLER NORDHEIM ONSET DRIFT UNDER HTRB STRESS.

Moreover, under the same stress conditions some devices got burnt before completing the entire stress procedure. The defectivity map detected at epitaxial inspection level which locates the defect inside the powerMOSFET, doesn't fit the same failed spot which has been detected at the edge of the transistor has shown on figure 50. This is supposed to be related to the higher field at the edge termination of the device. Another TCAD simulation is running to confirm this hypothesis.

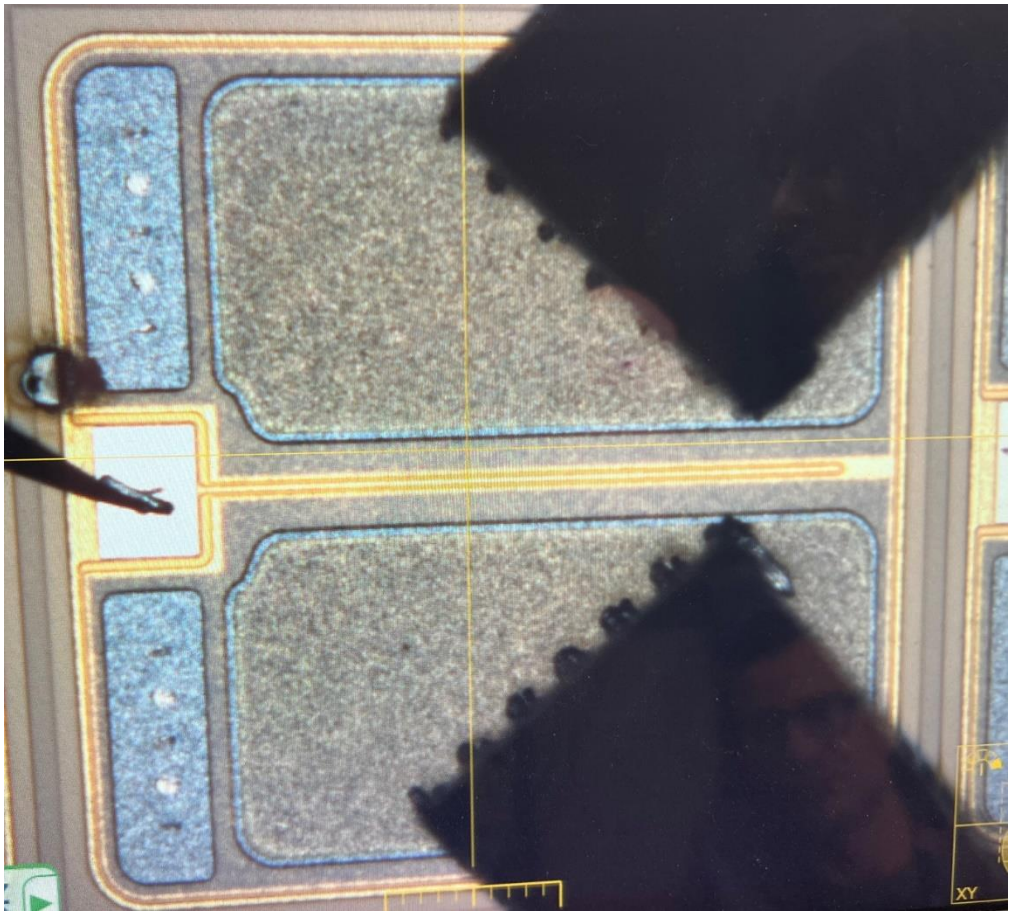

FIGURE 50. BURNT DETECTED AT THE EDGE OF THE TRANSISTOR.

In order to characterize the effect of extended defects on gate oxide conduction, I-V sweeps have been carried out (see figure 51) on both defected and defect free devices. Based on equation 49 it is possible to extrapolate the Fowler-Nordheim barrier height on both type of samples under negative and positive voltage or in other words under holes or electrons

injection. The I-V characteristics don't show any significant difference which leads to evaluate the potential difference [79].

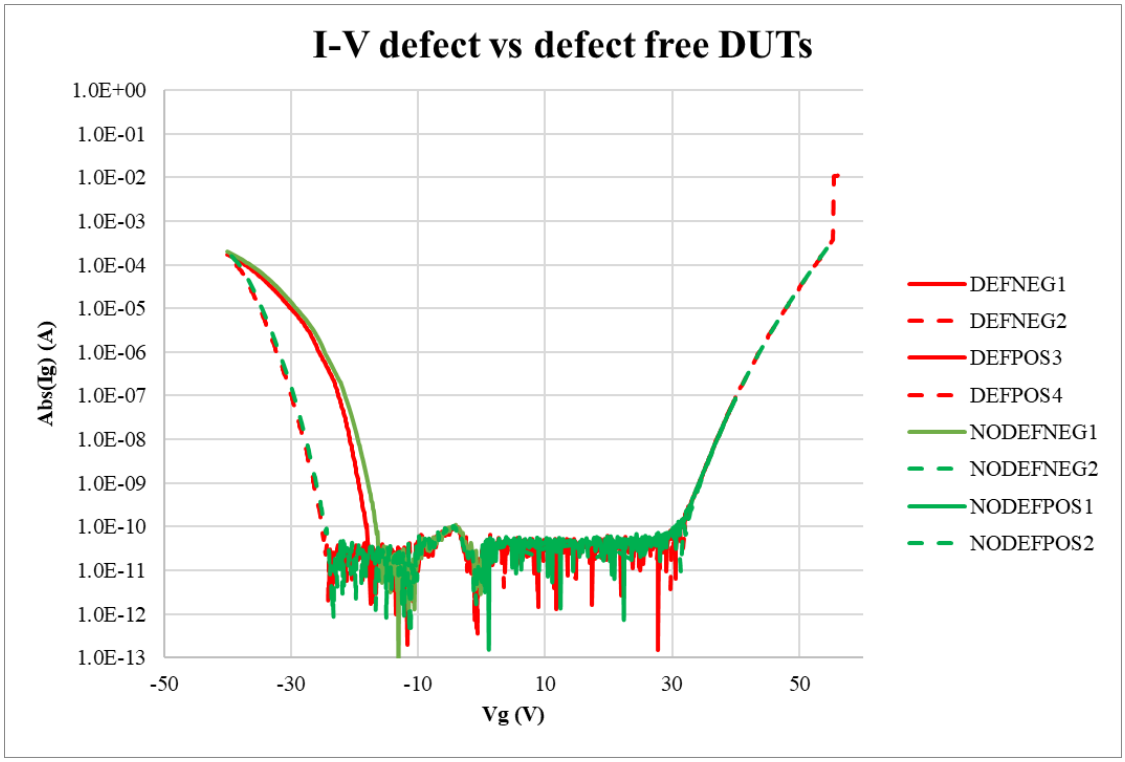

FIGURE 51. I-V UNDER HOLES AND ELECTRON INJECTION ON DEFECTED AND DEFECT FREE DEVICE.

INTRODUCTION ON RAMAN ANALYSIS

In order to better understand the origin and microstructure of the most common type of defects which seem not be electrically activated by the electrical characterization, a physical analysis by Raman spectroscopy has been carried out.

EXPERIMENTAL SETUP

The experimental setup used to collect the Raman data is based on a commercial system (NTegra NTMDT) which consists of two parts. One part is basically an AFM microscope equipped with a linearized tripod scanner on which the sample holder is installed. Above the latter is the optical part consisting of a 100X long working distance objective (Mitutoyo SLWD

100X 0.75NA) and a system of mirrors that project the signal collected from the sample through the objective onto the confocal optical path that precedes the high-resolution spectrometer (350mm flat field spectrometer MS3504i). The laser signal elastically reflected by the sample is rejected by system of filters installed along the optical path. A temperature stabilized 532nm solid state laser emitting a TEM00 single mode line was used as the source. The Raman signal dispersed by the monochromator is detected by a Andor IDUS camera equipped with a triple peltier stage and able to work down to -60 °C. The experiment was carried out by keeping the laser power as low as possible. In fact, it is known that excessive power can locally increase the temperature which would inevitably affect the raman response of the sample. Obviously, lower power means longer integration times. This observation may seem trivial, but it becomes clear when we keep in mind that if we want to acquire the Raman map of the sample, it will be necessary to record a spectrum for each point of the image. The above also limits the number of pixels in the map, in fact the overall acquisition time scales with the square of the number of lines of the image. In our case, the power has been reduced to less than 200 mW which makes it possible to acquire a single spectrum in 0.5s and 128X128points images in a total time of approximately 140 minutes. Another aspect related to the measurement time concerns the lateral resolution obtainable in the image. It is limited by diffraction and therefore by the numerical aperture of the objective and by the wavelength of the source used. In our case, a simple calculation allows us to evaluate the lateral resolution obtainable in 360 nm. The above means that 128X128 points is the highest number of points for images of about 50mm. Increasing the number of points simply increase dramatically the acquisition time adding no more information to the collected data.

RAMAN SPECTROSCOPY AND DEFECT CHARACTERIZATION

A defective device was inspected at the NBL level and selected for physical analysis, in particular Raman spectroscopy, in order to characterize the type of defects. The selected device contained a triangular defect, of particular interest for the purposes of this study, as this type of defect can have a major impact on the reliability and durability of the devices. Triangular defects are frequently observed in 4H-SiC homoepitaxial layers and their existence is reported to greatly degrade the performance. From the measurements carried out it is

possible to appreciate a notable change in the characteristic spectrum of 4H-SiC in the defective area.

Hereafter we analyse the Raman shifts of two different triangular defects. The Raman map described below (figure 52A) represents the intensity variations of the peak at 798 cm^{-1} which is characteristic of the material and therefore allows to highlight the presence of the crystalline defects.

Figures 52 B, C, D, E, F, G show the spectrum obtained at the points highlighted by the arrows on the map. The Raman shift collected outside the defect (figure 52C) shows two main peaks, the first with a greater intensity which is the transverse optical phonon (TO) at 777 cm^{-1}. The second, longitudinal optical phonon A1 (LO), is located at 970 cm^{-1}. These two peaks are well known, and match very well with the Raman peak positions of 4H-SiC polytype [80].

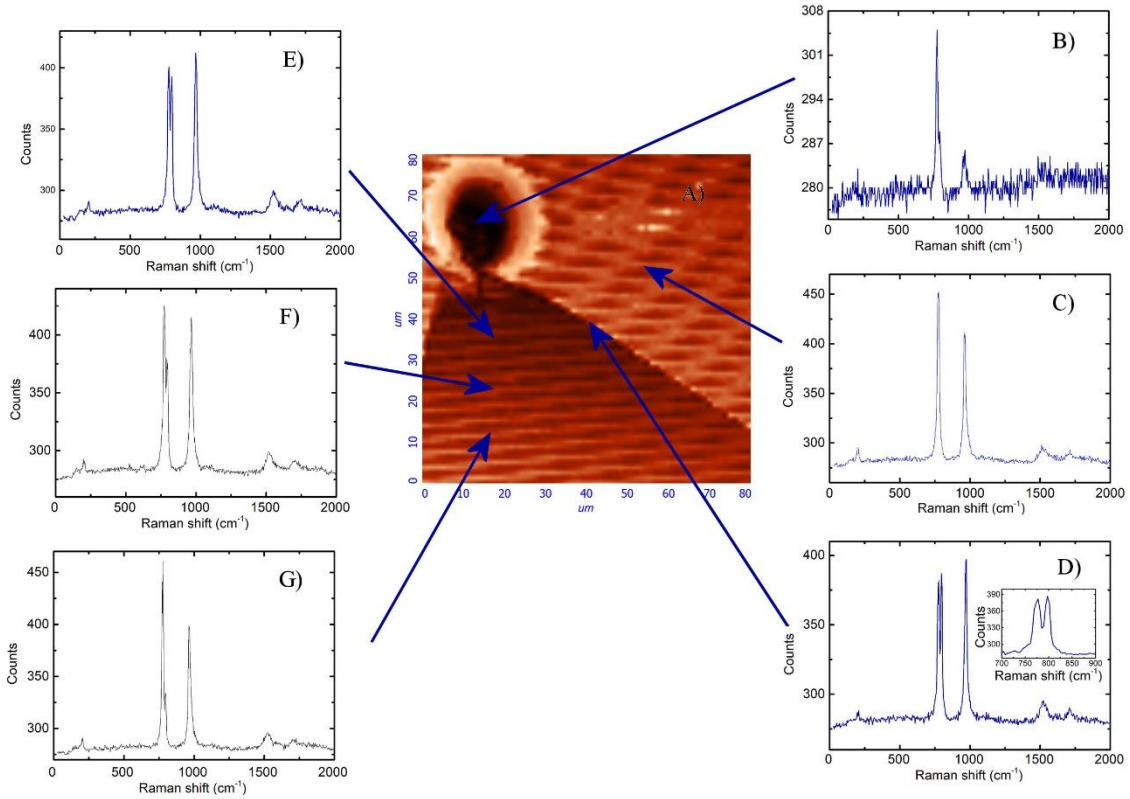

FIGURE 52. RAMAN SPECTRA COLLECTED AT DIFFERENT POSITIONS ON THE SAMPLE SURFACE.

Figure 52D shows the spectrum acquired at the interface between the defect free region and the triangular defect. The resulting Raman spectrum of this region, compared to the characteristic spectrum in figure 52C, shows the appearance of a new peak (see the inset in

figure 52D). In particular, the characteristic 4H-SiC peak at 777 cm^{-1} is still present but has a 12.4% lower intensity than the defect-free area. Furthermore, the spectrum is characterized by the presence of a new intense peak at 798 cm^{-1}. The latter is the characteristic peak of the 3C-SiC polytype, therefore, this analysis suggests that the triangular defect has a 3C nature as reported in the literature [61] [62] [63] [64]. The presence of both Raman spectrums in the triangular region, with 3C in higher intensity, can mean that the 3C layer is fully embedded under an overgrown 4H layer.

One of the most striking features is the large size spherical particulate located at the apex of the triangular region, which is most likely a downfall particle. Therefore, a further inspection is carried out in this region; the Raman spectrum collected at the center of the structure is characterized by a peak at 798cm^{-1} (figure 52B), indicating the 3C-SiC nature of the particle, likely dropped from the inner wall of the growth chamber during CVD epitaxy.

Figures 52 E, F, G are the Raman spectra collected to three roughly equidistant points arranged on a vertical line. As can be observed moving away from the defect located on the upper vertex of the triangular structure, the amplitude of the characteristic peak of the crystal configuration 3C decreases. This circumstance highlights that the triangular defect originating from the presence of a particle with a 3C crystalline structure propagates during epitaxial growth, and then tends to disappear as one moves away and the crystalline structure returns to the 4C form.

CONCLUSIONS

Despite the rapid development of technology, several problems remain that limit the reliability performance of SiC devices. One of the most important problems concerns the presence of crystalline defects that can propagate due to the thermomechanical stresses that the device undergoes during its operation. By propagating these defects can reach the active area of the device and destroy it, for this reason they are also named “killer defects” for 4H-SiC power devices. An appropriate reliability screening needs to be implemented to reject the weak devices, often “awaking” latent defectivity before the commercial distribution.
On this scenario pulsed HTGB and HTRB stress characterization have been carried out on 4H-SiC PowerMOSFETs defect free defected and at epitaxial defectivity inspection, and good after electrical wafer sorting, to characterize the most sensitive electrical test parameter drift under stress. Threshold voltage and Fowler-Nordheim voltage under negative bias show a higher instability and degradation than the other electrical parameters, i.e, these two parameters are much more sensitive than others. Moreover, supported by a TCAD simulation and a numerical quantification of the trapped charge inside the gate oxide, we demonstrated how the dominant process on the device degradation is related to the gate oxide field line distribution induced by stress on the device section rather than its absolute value. The above makes it clear that the device topology plays a key role in its reliability. Finally, we calculated the position of the trapped charge centroid to quantify, by the charge-sensing method, the trapped charge inside the gate oxide. The results confirm the hypothesis of the worst-case effect on gate oxide degradation of negative bias gate stress than HTRB stress even if the simulated gate field is the same

Increasing the defect free devices sampling under analysis on a high defective wafer, a weak signal of stress induced trapping has been detected by anomalous threshold and Fowler-Nordheim drift.

On the other hand, on extended defective devices, at present, there appears to be no greater accelerated drift on significant parameters and no different height of the hole barrier and electron charge. As a result, we may speculate that the chosen faulty devices do not have

point defects or contaminations that introduce interface states or energy levels in the SiC band gap that contribute to the entrapment charge [81] [79]. Additional tests are running to confirm the above hypothesis.

Beside the electrical characterization a physical analysis based on Raman Spectroscopy has been reported on 4H-SiC homoepitaxial layers which are often populated by a large number of triangular defects; understanding the origin and microstructure of this type of defects is therefore very important to define a strategy able to reduce their density as low as possible to improve the production yield and the reliability of the devices. There are currently two main models that explain the mechanisms of formation of triangular defects. One of these was postulated by Hallin and Konstantinov [61] [62] in 1997; the authors stated that an on-axis triangular region starts to grow during the homoepitaxy due to a substrate defect just below the apex of the triangular region. The formation of the triangular stacking fault (TSF) suppresses the conventional growth and leads to a bi-dimensional nucleation of 3C-SiC that forms large terraces. Si and Dudley [63] postulated another well-established model in the same year; they argued that the origin of the triangular defect is step grouping during epitaxy growth; the transition period is large enough to allow 2-dimensional nuclear 3C crystals on the terrace. The morphology of the triangular defect is the result of the competing expansion/propagation of both the 2-dimensional nucleated 3C-SiC on the 4H substrate and the 4H-SiC.

Our Raman inspection is in good agreement with the latter hypothesis and suggests that the 3C-SiC crystals nucleated two-dimensionally on the large triangular terrace left by the falling particle introduced during growth.

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