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**New Frontiers of Wide-Bandgap
Semiconductors-Based Power Electronics:
Novel Architectures and Reliability**

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Dedication

To the One Above, my deepest gratitude, first and foremost,
For guiding my steps and granting me strength when I needed it most.

To my beloved parents, Ayachi and Rachida,
Your unwavering love, boundless support, and immense sacrifices have been the cornerstone
of my success. Thank you for believing in me, for inspiring me to pursue my dreams, and
standing by me during the most challenging moments of this academic journey.

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General Introduction

The increasing demand for energy-efficient technologies has positioned power electronic devices as indispensable components in modern applications. These devices are integral to a wide range of technologies, from renewable energy systems and industrial automation to consumer electronics and electric vehicles. Their ability to optimize energy use, reduce losses, and improve system performance has made them critical to achieving these demands.

Power electronic devices play a crucial role in critical systems where performance and reliability are essential. For example, in electric vehicles, they have a direct impact on the overall performance of the vehicle. The significance of these devices extends to many other applications, where their reliability is often critical to ensure efficient operation.

However, with the growing reliance on wide-bandgap (WBG) semiconductor-based power devices in essential applications, the question of their long-term reliability becomes increasingly pressing. Failures in these devices can significantly impact the performance of the overall system, making it imperative to understand and mitigate potential reliability challenges. The complexity of reliability challenges is further compounded by the diverse operating conditions these devices encounter, including high thermal, mechanical, and electrical stress.

To address these challenges, a comprehensive reliability assessment of these devices is essential. In this context, this thesis aims to investigate the reliability challenges of Gallium Nitride (GaN) High Electron Mobility Transistors (HEMTs), a leading class of WBG-based power electronic devices. The research is structured to investigate two primary aspects of their reliability that significantly impact both their performance and operational lifetime.

The thesis is structured into several chapters, aiming to explore the various aspects related to our research topic.

Chapter 1 explores the principles and applications of semiconductor materials, emphasizing their critical role in power electronics. It begins with an overview of their fundamental

properties, followed by an introduction to the epitaxial growth techniques used for semiconductor-based electronic devices. The chapter then provides a detailed discussion of wide-bandgap semiconductors, including the key selection criteria for power electronic semiconductors, with a particular focus on Gallium Nitride and Silicon Carbide (SiC). The chapter highlights the advantages of WBG semiconductors in addressing the limitations of silicon-based technologies in power electronic systems.

Chapter 2 introduces the reliability challenges of wide-bandgap semiconductor-based power electronic devices, focusing on factors affecting the performance of GaN HEMTs. The chapter presents the failure mechanisms specific to the GaN HEMT chip and addresses reliability issues in WBG power electronic packaging, including failure mechanisms associated with various packaging components. Additionally, it provides an overview of the reliability models developed in the literature to estimate the lifetime of Silicon-based devices.

Chapter 3 investigates the reliability of GaN HEMTs by analyzing stress induced by a novel packaging design in a commercial AlGaN/GaN HEMT provided by STMicroelectronics. In the context of the study, the chapter begins with an introduction to residual stress in electronic packaging and the non-destructive techniques employed for stress assessment, followed by a presentation of GaN HEMT devices. In the experimental study, micro-Raman spectroscopy is used to quantify localized residual stress at the GaN layer and GaN/Si interface by analyzing the frequency shift of the GaN E2(high) phonon mode along the AlGaN/GaN heterostructure. A comparative analysis of packaged and bare devices provides insights into the impact of packaging on stress distribution within the device, therefore its performance and reliability.

Chapter 4 focuses on assessing the reliability of GaN HEMTs by investigating the behavior of dynamic ON-resistance during operation. The chapter begins with an overview of the causes of dynamic ON-resistance. In the experimental study, an in-depth characterization of the device is performed to examine the impact of thermal and thermomechanical effects on the evolution of dynamic ON-resistance during power cycling. Advanced characterization techniques such as high-speed infrared imaging and scanning vibrometry are employed to analyze, respectively, the thermal behavior and mechanical deformation of GaN HEMTs under stress. The findings provide comprehensive insights into the reliability of GaN HEMTs under thermal, mechanical, and electrical effects.

By addressing these two aspects of GaN HEMTs reliability, packaging-induced stress and thermomechanical effects on dynamic ON-resistance, this thesis aims to provide a global understanding of significant factors influencing their performance and operational lifetime. The findings contribute to the development of more reliable GaN-based power devices, enhancing their lifetime and performance for deployment in critical applications.

Chapter 1

Principle and applications of semiconductor materials

This chapter explores the principles and applications of semiconductor materials, emphasizing their critical role in power electronics. It begins with an overview of the fundamental properties, historical evolution, and classifications of semiconductors, followed by an introduction to the epitaxial growth techniques used for semiconductor-based electronic devices, and an explanation of the electronic band structure. The chapter then presents a detailed discussion of wide-bandgap semiconductors, including the key selection criteria for power electronic semiconductors, and provides an in dept discussion about Gallium Nitride and Silicon Carbide. The chapter highlights the advantages of WBG semiconductors in addressing the limitations of silicon-based technologies in power electronic systems.

Background

The dramatic increase in global energy consumption is one of the main factors behind the environmental crisis, which has intensified considerably by anthropogenic factors and now represents one of the most pressing challenges of our time. The surge in worldwide consumption of electrical energy is driven by the rapid pace of technological progress, as evidenced by the widespread adoption of electric vehicles, smart devices, and digital networks. In light of these challenges, innovative technological solutions, such as targeted advancements in power electronics, represent an imperative approach to mitigate energy waste and the adverse effects of energy consumption [1-2]. The transition to advanced energy systems requires the deployment of high-performance electronic components that can effectively minimize energy losses while enduring elevated operating conditions [3].

Power electronics is a critical field of electrical engineering that involves the control and transformation of electrical power using switching-mode power semiconductor devices [4]. Power electronics are playing a crucial role in energy conservation by reducing energy consumption and emissions, and promoting sustainable practices [4-5]. In recent years, power electronics technology has rapidly evolved, leading to numerous applications across various sectors, including industrial, aerospace, renewable energy systems, and transportation [4]. This growth is driven by the technological advancements in the semiconductor industry, the expanding markets for renewable energy applications, the progress in microelectronics, and the increasing demand for smaller, lighter and higher performance power systems [6]. Semiconductor materials, in particular silicon (Si), offer several advantages to power circuit designers, however, silicon technologies approach their intrinsic limitations, and their performance is becoming constrained. In this context, wide-bandgap semiconductors represent a promising alternative capable of overcoming the limitations associated with silicon-based technologies. Thanks to their unique electronic properties, WBG semiconductors can enhance device performance by enabling lower energy consumption, higher power density, and the development of more compact and lightweight systems. This introduces a true revolution in the generation, conversion, and management of electrical energy [7-9]. Among wide-bandgap semiconductors, Gallium Nitride and Silicon Carbide are the main candidates offering significant advantages for high-power electronics [7-8, 10-11]. These materials have very appealing electronic properties, the most notable being their significantly

wider energy bandgap compared to silicon's 1.1 eV. Specifically, SiC has a bandgap of about 3.26 eV, and GaN has approximately 3.4 eV [11]. Additionally, these materials exhibit higher electron mobility and greater thermal conductivity. The much wider bandgap compared to silicon allows WBG-based power devices to operate at higher temperatures and with greater breakdown voltages, while simultaneously achieving lower on-state resistances. This results in reduced energy losses during switching processes. Furthermore, the exceptional electron mobility of GaN ($\sim 2200 \text{ cm}^2/\text{V}\cdot\text{s}$ compared to $1500 \text{ cm}^2/\text{V}\cdot\text{s}$ for Si and about $200 \text{ cm}^2/\text{V}\cdot\text{s}$ for SiC) enables higher switching speeds with rise times on the order of 50 V/ns. This characteristic allows for the development of power converters operating at frequencies of several hundred kilohertz (exceeding the typical $\sim 100 \text{ kHz}$ for Si or SiC). The high breakdown voltage, which is roughly ten times that of silicon, makes WBG semiconductor-based devices ideal candidates for next-generation power electronics, which typically operate at high voltages to reduce current levels [8, 10-12].

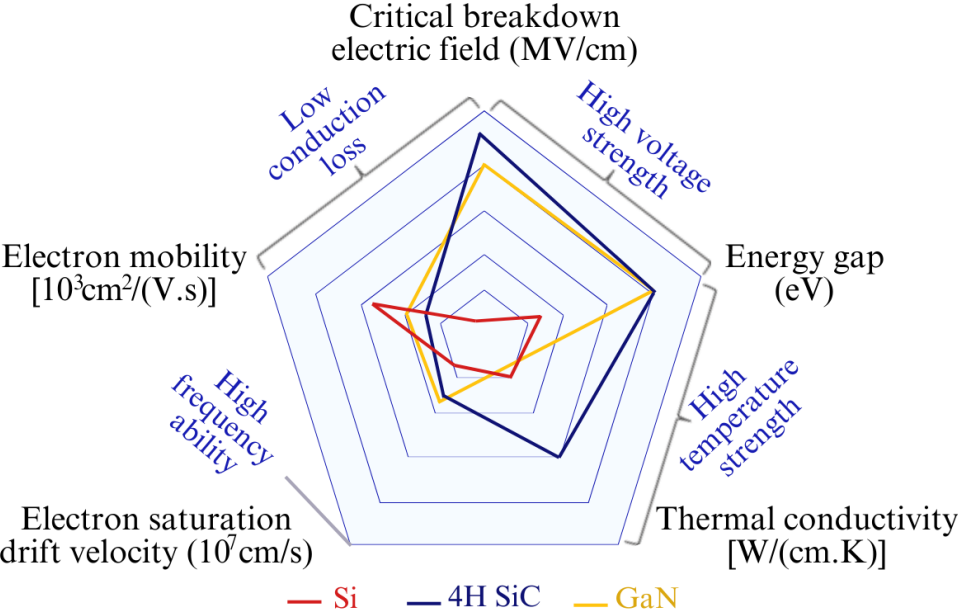


Figure 1. Comparison of Key Properties of Semiconductor Materials [11].

The integration of such materials into semiconductor technology is crucial for enhancing the performance and reliability of electronic devices. However, for these materials to be effectively used in the semiconductor industry, understanding their intrinsic properties is not enough; it also requires the development of suitable and scalable manufacturing processes, which are currently not yet mature. This drives up production costs, limiting their range of applications [13]. For instance, silicon carbide is suitable for applications requiring high voltages (over 650

V). However, the high cost of SiC, primarily due to the epitaxy of the SiC substrate and fabrication costs, restricts its widespread applicability. On the other hand, GaN-based devices are more economically viable because of lower production costs, but these devices can only be used in applications operating at lower voltages (below 650 V) [11].

1.1. Semiconductors - Basic Overview

1.1.1 Introduction to Semiconductor Materials

A crystalline semiconductor is a material in which the atoms are arranged in a highly ordered, repeating pattern called a crystal lattice. The main characteristic of crystalline solids is the presence of “*energy bands*”, which represent the set of energy states that can be occupied by the electrons in the solid. When electrons are in a crystalline system, they lose their atomic characteristics. Indeed, a simple model used to describe the possible energy states for the electrons in a crystal, it is found that only certain energy ranges can be occupied by the electrons, known as “*energy bands*”. The number of available states in each band is $2N$, where N is the number of atoms in the structure.

With this simple scheme, it is easy to see that a crystal made of atoms with an even number of electrons will have the last band completely filled and the next one completely empty. In this case, we refer to *insulators* because if an electric field is applied, no current can flow, as there are no available higher-energy states for the electrons to occupy (and thus, they cannot absorb any energy provided by the field). On the other hand, crystals whose atoms have an odd number of electrons will only half-fill the last band. Therefore, an electric field can provide energy to the charge carriers, which, accelerating in the opposite direction to the field, will occupy higher-energy free states within the band. In this case, we refer to *metallic conductors*, and the occupied energy band is called the *conduction band*. Between the conduction band and the valence band, there is an energy range forbidden to electrons, known as the “*energy gap*” or “*band gap*”. Materials with relatively small energy gaps, which range between 0 eV and about 4 eV (typical for insulators) are named semiconductors. Recently, also some materials such as diamond, with a wide band gap of 6 eV, are classified as *wide band semiconductors*. In addition, semiconductors demonstrate electrical resistivity ranging from 10^{-2} to $10^9 \Omega \text{ cm}$ [13]. The transport mechanism in semiconductor materials requires some clarifications: if, in some way, an electron is moved from the valence band to the conduction

band (excitation), a "charge absence" called a "hole" will remain in the valence band. In the presence of an electric field, this hole can gain energy in the direction of the field and contribute to transport phenomena. This framework differentiates semiconductors from metals because, in semiconductors, charge transport can be supported by both negative carriers (*electrons*) and positive carriers (*holes*). In general, the electrical conductivity in semiconductors is mainly attributed to the presence of free charge carriers, which can be generated, for example, by photon absorption. A more complex discussion involves the contribution to electrical transport due to the inevitable presence of impurities in the crystal. Impurity atoms can create localized electronic states within the forbidden energy gap. These states can provide electrons (by releasing the carrier to the conduction band) or holes (by capturing an electron from the valence band), even through simple thermal excitation. Furthermore, it is possible to "engineer" the crystal by intentionally introducing atoms of a different nature from the crystalline matrix. In this case, if the impurity atom has one more bonding electron than the matrix atoms, the material is said to be "N-type"; conversely, if it has one fewer bonding electron, the material is said to be "P-type", and the process is named "doping". From an energetic perspective, the presence of an impurity atom in the crystal with an extra electron creates a situation where, at $T = 0$ K, the extra electron remains bound to the donor atom in a hydrogen-like structure, but with a very small ionization energy. At room temperature, the thermal energy is sufficient to ionize this structure, exciting the donor atom and moving the electron into the conduction band. In this way, an N-type semiconductor conducts current through negative charge carriers (electrons). Similarly, an impurity atom with fewer outer shell electrons than the crystal atoms creates a localized empty state spatially around the impurity and just above the valence band energetically. Thus, thermal excitation can move an electron from the valence band to the localized impurity state, leaving behind a hole. In this case, the material is referred to as a P-type semiconductor, where transport occurs through the movement of holes [14-15]. Semiconductors play a fundamental role in electronics and photonics due to their unique ability to modulate their electronic properties in response to external factors such as light, voltage, magnetic fields, temperature, or mechanical stress. These characteristics make them indispensable for a wide range of applications, including electronics and computing, sensing technologies, electro-optical displays, and more [13-16].

1.1.2 Evolution of semiconductors

The history of semiconductors is rich and complex, dating back to 1782 when Alessandro Volta first used the term “semiconducting”. In 1822 Seebeck reported the first semiconducting property in lead sulfide (PbS). However, it was Michael Faraday who made the earliest documented observation of a semiconductor effect in 1833, noting that the resistance of silver sulfide (Ag_2S) decreased with temperature, which is in contrast to the behavior of metals. Building on this, Johann Hittorf quantitatively analyzed the temperature dependence of electrical conductivity in Ag_2S and copper sulfide (Cu_2S) in 1851. And the first practical application of semiconductors as a device came in 1874 when Karl Ferdinand Braun demonstrated conduction and rectification in metal sulfides when probed with a metal point. Around the same time, Arthur Schuster discovered copper oxide (CuO) as a new semiconductor, which eventually formed the foundation for the development of copper oxide rectifiers in 1926. Three years later, Walter Schottky has proved experimentally the presence of a barrier in a metal semiconductor junction. Later, by 1839, Alexander Edmund Becquerel had uncovered the photovoltaic effect at a junction between a semiconductor and an electrolyte, and in 1873, Willoughby Smith discovered photoconductivity in selenium (Se), followed by Adams and Day's 1876 discovery of the first photovoltaic effect in the same material. In 1883, Charles Fritts built the first functional solar cell, but its efficiency was less than 1%. Then, the discovery of the Hall effect in 1878—where charge carriers in solids are deflected in magnetic field—provided a powerful tool for studying semiconductor properties. In 1930, Bernhard Gudden attributed semiconductor characteristics to the presence of impurities, arguing that pure semiconductors did not exist. This was followed by Alan Wilson's 1931 development of band theory of solids, explaining semiconductor properties through the concepts of filled and empty energy bands. History culminates in the revolutionary invention of the bipolar junction transistor by Shockley, Bardeen, and Brattain in 1947, which laid the foundation for the modern electronics. [14, 17] In the early stages, semiconductor research focused exclusively on crystalline materials. However, the discovery of amorphous semiconductors began in 1950 with the development of amorphous selenium ($\alpha\text{-Se}$), marking a significant shift in the field alongside the rise of the transistor. By 1968 chalcogenide glasses, another class of amorphous semiconductors, were introduced, and more recently, amorphous silicon alloys have garnered substantial attention due to their unique properties. In addition to

these materials, organic semiconductors and artificially engineered compounds have expanded the landscape of semiconductor materials. Today, advanced materials can be purposefully designed to exhibit specific characteristics tailored to applications such as high-temperature superconductivity [14].

1.1.3 Classification of Semiconductors

Semiconductors can be classified according to their different compositions and structures, each with distinct properties suited for specific applications.

Elemental semiconductors

Elemental semiconductors, such as silicon (Si) and Germanium (Ge), exhibit a tetrahedral bonding structure and are fundamental to modern electronics. Certain elemental components from groups V and VI of the periodic table (e.g., phosphorus (P), sulfur (S), selenium (Se), tellurium (Te)) also display semiconducting behavior, featuring diverse crystal structures.

Binary compound semiconductors

In addition to elemental types, binary compound semiconductors combine elements from different groups in the periodic table, such as ZnS (II-VI), GaAs (III-V) and GaN a wide-bandgap III-V compound which plays a critical role as optoelectronic material in blue light-emitting diodes and lasers.

Ternary and quaternary semiconductors

Semiconductors can also exist in ternary and quaternary forms, e.g., Aluminium Gallium Arsenide (AlGaAs) and $Ga_xIn_{1-x}As_yP_{1-y}$.

Diverse classes of semiconductors and their unique properties

Some oxides can also act as semiconductors; although most oxides are insulators, some, like cuprous oxide (Cu_2O), have been extensively studied for their semiconducting properties. Additionally, organic semiconductors, such as polyacetylene $(CH)_n$, offer the possibility of modifying their properties for specific applications by altering their chemical structures. Semiconducting compounds containing magnetic ions, like $Cd_{1-x}Mn_xTe$, possess unique semiconducting and magnetic properties, including ferromagnetism. Other semiconductors exhibit ferroelectric characteristics (for example, antimony sulfide (Sb_2S_3)) or superconductivity, as in the case of GeTe. Furthermore, recent studies on layered

semiconductors, such as gallium selenide (GaSe), allow for quasi-two-dimensional electronic behavior, facilitating the manipulation of interlayer interactions. This variety of semiconductor materials supports their wide-ranging roles in multiple applications [13]. Among these semiconductors, silicon (Si) remains the most widely used due to its numerous advantages. Its high natural abundance makes it cost-effective for large-scale production. Additionally, silicon can be easily doped with impurities to create both n-type and p-type semiconductors. Furthermore, the stable oxide layer of silicon makes it an ideal substrate for electronic circuit manufacturing, establishing it as a fundamental material in modern electronics [15].

1.1.4 Epitaxial growth techniques for semiconductor-based electronic devices

Semiconductors are highly valued in the electronics industry not only for their intrinsic properties but also due to the availability of advanced growth techniques. Advanced semiconductor devices typically incorporate critical sophisticated components, such as quantum wells and superlattices, characterized by atomically sharp and abrupt interfaces. The fabrication of such intricate structures is achieved exclusively through epitaxial growth techniques, which enable the precise deposition of ultra-thin layers with high accuracy [14]. Superlattices and low-dimensional structures, including quantum wires and quantum dots, are engineered through the sequential deposition of thin layers of different semiconductor materials. By precisely managing layer thickness and chemical composition, these structures exhibit customizable material properties, offering substantial opportunities for the development of optimized next-generation devices [14].

Several epitaxial growth techniques are available, each with distinct benefits and constraints. For instance, in silicon-based devices, epitaxial layers can be grown using vapor-phase epitaxy (VPE), liquid-phase epitaxy (LPE), or solid-phase epitaxy (SPE). However, VPE is particularly the preferred technique for producing high-quality silicon layers suited to device applications, whereas LPE and SPE are typically reserved for research context rather than large-scale industrial production [18]. Silicon VPE encompasses Chemical Vapor Deposition (CVD) and Molecular Beam Epitaxy (MBE), both of which enable the precise deposition of crystalline monolayers onto a substrate with atomic-level control over the thickness of the grown layers [13, 18]. These techniques, along with LPE, remain the most frequently used methods for fabricating electronic and optoelectronic devices [14].

Chemical Vapor Deposition (CVD)

CVD is a widely used technique for growing thin, high-quality epitaxial layers (typically around 1 μm or less) on a bulk substrate. Achieving high crystalline quality of the deposited layer requires that the thin film and the substrate share similar crystal structures and closely matched lattice parameters, minimizing interfacial strain. A key advantage of CVD is its precise control over the growth rates, achieved by regulating the flow of gaseous precursors.

In silicon epitaxy, for instance, silane (SiH₄) gas decomposes to deposit highly pure silicon films onto a substrate, with hydrogen (H₂) as a by-product. This process enables precise control over layer thickness and high film purity.



III–V Compound semiconductors, can also be synthesized via CVD by employing gaseous metal-organic compound precursors such as trimethylgallium Ga(CH₃)₃. This method of growing epitaxial films from metal-organic gases is known as **Metal-Organic Chemical Vapor Deposition (MOCVD)** and is particularly effective for fabricating compound semiconductors like GaAs, indium phosphide (InP), and GaN.



Molecular Beam Epitaxy (MBE)

MBE is a technique for depositing high-quality layers under ultrahigh vacuum (UHV) conditions, typically below 10⁻¹¹ torr. The system comprises a UHV growth chamber where reactants are introduced as molecular beams, produced by heating source materials in a Knudsen cell with a narrow orifice. As vapor escapes through the orifice, molecules or atoms form a highly collimated beam directed at the substrate, enabling epitaxial layer growth. MBE provides precise control over film composition and thickness, however, its high cost restricts its widespread application in large-scale commercial film production [13].

Liquid-Phase Epitaxy (LPE)

LPE is a technique in which a crystalline layer is grown from a supersaturated solution or melts on a substrate. This well-established method enables the growth of layers with exceptional structural quality and high deposition rates, often up to 1 μm per minute. Operating near thermodynamic equilibrium, LPE minimizes the density of points and dislocation defects, resulting in high-quality crystal structures. It has been effectively used to grow various materials, including III-V, II-VI, and IV-IV compound semiconductors, as well as magnetic and superconducting oxides. LPE is particularly advantageous for applications requiring thicker layers due to its substantial deposition rate [14].

1.1.5 Crystal bonding

The intrinsic characteristics of semiconductors are profoundly influenced by their crystal bonding and crystal structure. A comprehensive understanding of crystal bonding is essential for engineering semiconductors to meet the demands of advanced technologies [14].

The formation of solids is governed by interatomic forces comprising both attractive and repulsive components, which establish an equilibrium distance at the point of lowest potential energy. Attractive interatomic forces are primarily electrostatic - such as ionic, metallic, or hydrogen bonding - or arise from the sharing of valence electrons in covalent bonding. Most materials exhibit mixed bonding, where multiple bonding types contribute to interatomic interactions. In contrast, repulsive interatomic forces result from the strong resistance of atomic electronic shells to overlap. These competing forces determine the stability and structural characteristics of semiconductor crystals.

Elemental semiconductors such as Si, Ge and diamond are bonded exclusively by covalent bonding. Covalent bonds form through quantum-mechanical interactions resulting from the overlap of atomic orbitals, where two electrons are shared between neighboring atoms, creating a "bridge" of electron density that binds the atoms together. Quantum mechanically, this bond is characterized by a nonspherical electron density distribution that stretches between the bonded atoms. This distribution can change depending on the specific energy states of the participating electrons [14].

1.1.6 Electronic band structure

A fundamental property of semiconductors lies in the distinct behavior of their electrons at the microscopic level, especially the presence of energy gaps in their electronic excitation spectra. This unique characteristic, described through the electronic band structure of the material, differentiates semiconductors from both metals and insulators. Silicon atom, for instance, exemplifies this behavior with an electron configuration of $1s^2 2s^2 2p^6 3s^2 3p^2$. In this configuration, the inner orbitals ($1s^2$, $2s^2$, and $2p^6$) are fully occupied by core electrons, which remain close to the atomic nucleus. Conversely, the outer $3s$ and $3p$ orbitals, which are only partially filled, contain valence electrons that play an active role in forming bonds with neighboring silicon atoms, thereby shaping the material's electronic properties. [16] In crystalline silicon, each atom's four valence electrons ($n=3$) engage in interactions with adjacent atoms. Through overlap and coupling of the $3s$ and $3p$ orbitals, a collective sharing of electrons occurs across atoms, forming a band of allowed energy states ($8N$ states). At the equilibrium inter-atomic distance, this interaction results in the splitting of these states into two distinct energy bands, each with $4N$ states: a lower-energy valence band, populated with bonding electrons (binding states), and a higher-energy conduction band, generally empty under standard conditions, containing anti-binding states. The distribution of these energy states within the $n=3$ electron shell for tetrahedrally bonded silicon (diamond structure) varies with distance from the atomic nuclei, shaping the material's electrical behavior (**Figure 2**). The energy gap between the top of the valence band and the bottom of the conduction band, known as the band gap or forbidden energy gap (E_g), defines the minimum energy required to promote an electron into the conduction band and leave a positively charged hole in the valence band. This band gap energy is critical to the operational mechanisms of semiconductors [14, 16].

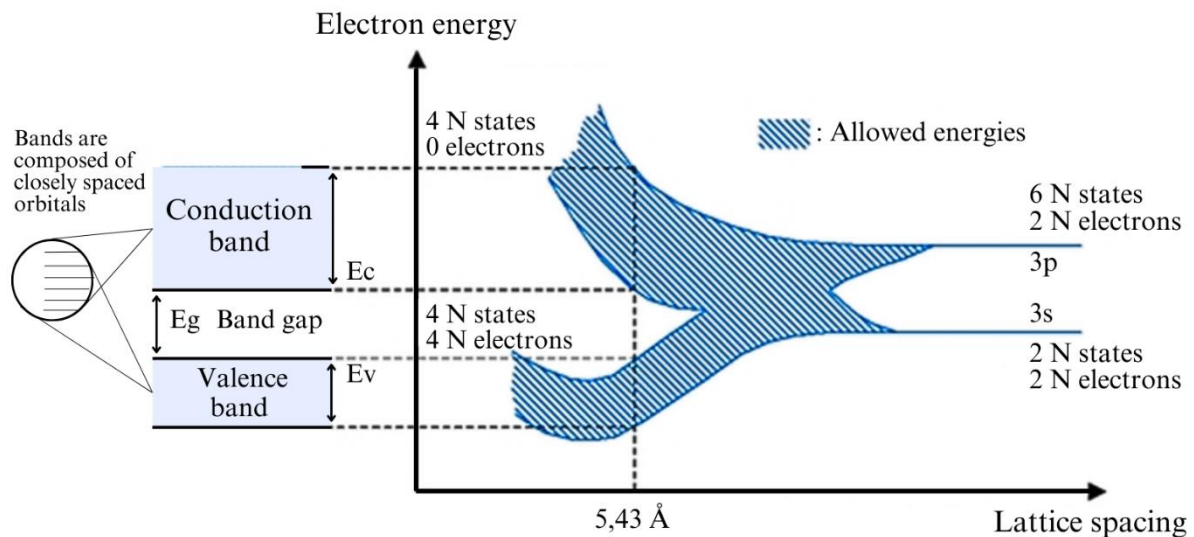


Figure 2. Electron energy levels in diamond structure silicon as a function of the distance of the atomic nuclei (schematic).

1.2. Wide-band gap semiconductors

Since the development of semiconductor technology in the early 1950s, silicon has been the primary material for fabricating electronic devices used in current switching and microelectronics. However, inherent material limitations constrain silicon's performance in power electronic applications primarily due to its moderate breakdown electric field and thermal conductivity. Silicon's low breakdown field constrains its conductivity at a specific breakdown voltage, while its moderate thermal conductivity hampers efficient dissipation of excess power during operational stresses like overcurrent and short circuits, increasing the risk of device failure. In contrast, WBG semiconductors offer superior material properties for power electronics. They exhibit a high breakdown field far exceeding that of silicon, enabling enhanced performance in high-power applications with greater voltage blocking capability (see **Table 1**). Also, WBG semiconductors feature high thermal conductivity enabling power electronic devices to withstand higher power densities compared to Si devices.

1.2.1 Key selection criteria for power electronic semiconductors

Several criteria and properties are used to evaluate semiconductors for power electronics applications, the most important are:

Baliga's Figure of Merit (BFOM)

Baliga's Figure of Merit (BFOM) is a key parameter used to evaluate and compare the performance of different semiconductor materials for power electronics, particularly in high-efficiency power switching devices like MOSFETs and IGBTs. It is defined as:

$$\text{BFOM} = \epsilon\mu E_B^3 \quad (3)$$

With ϵ denotes dielectric strength, μ is charge carrier mobility, and E_B represents the breakdown field. Although BFOM values are frequently derived from theoretical material properties, that may not fully represent real operating conditions, they still serve as a comparative reference for assessing the ultimate potential of semiconductor materials in power electronics. Among the wide-bandgap semiconductors presented in **Table 1**, SiC is distinguished by a high BFOM value, surpassing that of silicon, which makes it an attractive choice for high-performance power electronics [19].

Johnson Figure of Merit (JFOM)

WBG semiconductors possess ideal characteristics for high frequency switching applications. Johnson's Figure of Merit (JFOM) is a key metric used to evaluate the performance of semiconductor materials for high-frequency and high-power applications. It was introduced by E. H. Johnson in the 1960s as a way to compare the capabilities of different semiconductor materials, particularly in applications where both high-speed switching and high power-handling capabilities are crucial. It is defined as:

$$\text{JFOM} = \frac{v_s E_B}{2\pi} \quad (4)$$

Where v_s is the saturation velocity of charge carriers and E_B is the critical electric field. JFOM highlights the material's capacity to energize charge carriers essential for electronic signal processing. The Johnson Figure of Merit (JFOM) suggests that at high frequencies, the short duration for energy transfer limits the amount of energy a charge carrier can receive, leading to lower power output from the device. Consequently, device physics dictates an inverse relationship between power and frequency, regardless of thermal dissipation factors.

Table 1 presents the JFOM values of various semiconductors, where GaN exhibits the highest value. From a practical perspective, epitaxial GaN layers grown on semi-insulating SiC

substrates are commonly utilized to fabricate high-frequency and medium-power switching devices, which are critical in mobile communication networks [19]. The figures of merit values listed in **Table 1** are normalized with relation to silicon, with higher values indicating superior material performance in each respective category.

Table 1. physical properties (room temperature values) of wide-bandgap semiconductors for power electronic applications in comparison to Silicon [19].

Property	4H-SiC	GaN	Si
Lattice parameter (Å)	a= 3.08	a= 3.19	5.43
	Hexagonal	Hexagonal	Cubic
Bandgap E_g (eV)	3.2	3.44	1.1
Breakdown field, E_B (10^5 V/cm)	40	50	3
Dielectric constant, ϵ_r	9.7	10.4	11.9
Thermal conductivity, λ (W/cm/K)	3-5	1.3	1.5
Saturated E-drift velocity, V_{sat} (10^7 cm/s)	2.5	2.5	1
Electron mobility, μ_n ($cm^2/V/s$)	<900	<1000	1400
Doping capability	n-type p-type	n-type p-type	n-type p-type
Baliga FOM $\epsilon\mu EC^3_B$ with relation to Si	500	1100	1
Johnson FOM $v_s E_B / 2\pi$ with relation to Si	25	31	1

To provide high power and low loss operation in power switching devices, low on-state resistance (R_{on}), high breakdown voltage (V_B) and fast switching capability are desired [19].

Low On-resistance (R_{on})

The On resistance is a crucial parameter for assessing semiconductors for power MOSFET. Wide-bandgap semiconductors lead to a significant reduction in on-resistance at a given operating voltage which implies lower conduction losses and superior conversion efficiency. In this frame, SiC is the best material among WBG semiconductors, offering an ON resistance around 10 times lower than the equivalent device based on silicon [8].

High breakdown voltage (V_B)

WBG materials exhibit higher breakdown voltage compared to Si due to larger bandgap. In power electronics, high-voltage capabilities are often required, yet minimizing on-resistance is

also essential. The compromise between these two parameters is illustrated by Baliga's figure of merit:

$$R_{on} = \frac{4V_{BR}^2}{\mu_n \epsilon E_c^3} \quad (5)$$

Where V_{BR} denotes the breakdown voltage, μ_n represents the mobility of charge carriers, ϵ is the dielectric constant, and E_c signifies the critical field.

However, evaluating Baliga's figure of merit is complicated, as the critical field depends on doping concentration, and mobility depends on doping concentration and on the field. A more generic formula that depends only on the design parameters and mobility is presented as:

$$R_{on} = \frac{W_{PP}}{q\mu_n N_D} \quad (6)$$

Here, W_{PP} represents the depletion width or the thickness of the depletion layer, μ_n is the mobility of charge carriers, and N_D indicates the doping level.

Fast switching capability

Some WBG semiconductors can operate at fast switching speed for high frequency switching devices. This property directly depends on the saturation drift velocity. As can be seen from **Table 1**, GaN is the most suitable material in this case as it has the highest JFOM value.

High thermal conductivity

A high thermal conductivity of semiconductor materials is essential for improving heat dissipation in power electronic devices and allowing higher current flows while maintaining lower temperatures. SiC has the highest thermal conductivity compared to the other semiconductors listed in **Table 1**.

Capability to carry out dopants

The ability to incorporate dopant atoms into the crystal structure, and thus the possibility of obtaining P-type or N-type doping, is one of the most important characteristics of semiconductor materials used in the fabrication of electronic devices (and beyond). In fact, all electronic devices are manufactured by selectively doping specific areas of the crystal (**Table 1**).

1.2.2 Characteristics of wide-bandgap semiconductors - SiC and GaN

Silicon Carbide (SiC)

Silicon carbide, IV–IV WBG semiconductor, is a promising material for next-generation power devices designed for high power, high temperature, high frequency, and radiation-intensive applications. SiC material supports the development of faster, more compact, lightweight, and more powerful power electronic systems. SiC exists in several polytypes; however, only the 6H– and 4H–SiC forms are commercially available in both bulk wafers and customizable epitaxial layers. Among these, 4H–SiC is the favored one for power devices due to its higher carrier mobility along the c-axis, and its low dopant ionization energy - The letter H refers to the hexagonal crystal structure, while the number refers to the number of atomic bi- layers. Thanks to its strong covalent bonding, SiC exhibits substantially higher thermal conductivity compared to the standard Si, allowing SiC-based devices to manage much greater power densities. Moreover, SiC offers enhanced electrical properties positioning it as a favorable alternative to standard semiconductors which are considered to have reached their limits.

The development of cost-effective high quality SiC epitaxial layers has enabled the creation of several wide-bandgap devices based on SiC, including metal-semiconductor field-effect transistors (MESFETs), static induction transistors (SITs), bipolar junction transistors (BJTs), metal-oxide-semiconductor field-effect transistors (MOSFETs), PIN diodes, insulated gate bipolar transistors (IGBTs), and gate turn-off thyristors (GTOs), which have shown superior performance compared to their Si and GaAs counterparts. Notably, SiC Schottky diodes and MOSFETs have been skyrocket due to their commercial and industrial applications with further expansion expected especially in electric vehicle applications [19-20].

Gallium Nitride (GaN)

Over the past three decades, gallium nitride, III–V WBG semiconductor, has become a highly promising material for the development of high-performance energy-efficient power electronic devices and optoelectronic components. This capability has accelerated the growth of the GaN market, positioning it as a competitive alternative to standard semiconductor materials. [21] GaN is characterized by its high critical electric field (E_c) of ~ 3.3 MV/cm, advantageous for the development of high-efficiency GaN electronic devices operating under high voltages. This characteristic enables the fabrication of transistors with breakdown

voltages exceeding 1 kV, enhancing their reliability in demanding applications[22]. Additionally, GaN has a higher saturation electron velocity of around 3×10^7 cm/s comparing to the Si one (1.5×10^7 cm/s). This high saturation velocity of carriers is attributed to the substantial energy separation of electrons between the Γ conduction band and the L valleys, which results in a reduced transit time. This allows GaN devices to operate at both high power and high frequency with improved conversion efficiency. Another unique advantage of GaN is the generation of free carriers at the heterointerface, neutralizing fixed spontaneous and piezoelectric polarizations. This process enables GaN-based devices, HEMTs, to exploit the high-mobility of the two-dimensional electron gas (2DEG) at the heterointerface, which allows for very low on-resistance values (e.g., less than 50 m Ω for a 30 A device), enhancing device efficiency. The low product of on-resistance and gate charge ($R_{on} \times Q_g$) further minimizes switching losses, allowing them to operate at higher frequencies [22]. GaN's high switching capabilities also allow the downsizing of power systems, reducing system costs by miniaturizing passive components like inductors, capacitors, and transformers. In terms of performance metrics, GaN significantly outperforms silicon in Johnson's limit, underscoring its potential for high-frequency applications. Furthermore, GaN demonstrates high temperature stability, advantageous to simplify the attached cooling system for the high-power dissipation systems. GaN is widely adopted across multiple sectors, including RF power, photonics, high-frequency communication, and power conversion. The inherent robustness of GaN devices enables them to expand into markets such as military and aerospace, as well as automotive sector which is increasingly focusing on GaN technology driven by the strong incentives for vehicle electrification and the need to enhance driving range through improved system efficiency [22-23]. In summary, SiC and GaN each offer distinct advantages, making them well suited to specific applications and market needs. The selection between these materials depends on the requirements and limitations of the application; for instance, SiC is preferred for high-power and high-voltage applications, whereas GaN is ideal for high-frequency and high-speed applications. The future of these technologies is focused on continued improvements in performance, cost-efficiency, and manufacturability, which will further expand their range of applications.

Chapter 2

Reliability of Wide-bandgap Power Electronic Semiconductor

This chapter introduces the reliability of wide-bandgap semiconductor-based power electronic devices, focusing on the challenges affecting GaN HEMTs performance. It begins by discussing failure mechanisms specific to GaN HEMT chip, including gate leakage and thermally activated mechanisms. The discussion then continues with the reliability issues in WBG power electronic packaging, addressing failure mechanisms associated with various packaging components, focusing on wire bonding package. Finally, it briefly discusses the reliability models used to estimate the lifetime of Silicon-based devices, emphasizing the need to evaluate their applicability and accuracy for WBG devices experiencing similar failure modes.

Introduction

WBG semiconductor-based power electronic devices, such as GaN HEMTs and SiC MOSFETs, are widely utilized for their outstanding mechanical, thermal and electrical characteristics [24-25]. Their ability to operate under extreme conditions has increased the reliability requirements of WBG power electronics, making it a primary area of research for both industry and academia. Ensuring the reliability of these devices is crucial, as it directly affects the overall performance of the entire electronic system [26]. In this context, this chapter provides a general overview of reliability research, covering the failure mechanisms of GaN HEMT chips, the reliability of WBG power electronic packaging focusing on wire bonding packaging, and reliability models used to predict the lifetime of Silicon-based devices.

2.1. Failure mechanisms of GaN HEMT chips

WBG semiconductors are designed to endure extreme operating conditions, which can unavoidably lead to WBG device failures, directly affecting the overall system's reliability. This section focuses on failure mechanisms of GaN HEMT, one of the most widely adopted and commercially available WBG devices. It is a field-effect transistor distinguished by its exceptional carrier mobility, ranging from 1200 to 2000 cm^2/Vs , due to the presence of a 2DEG within the AlGaN/GaN heterostructure. This physical structure enables superior performance; however, it also gives rise to, till unknown, failure mechanisms that impact device reliability [27].

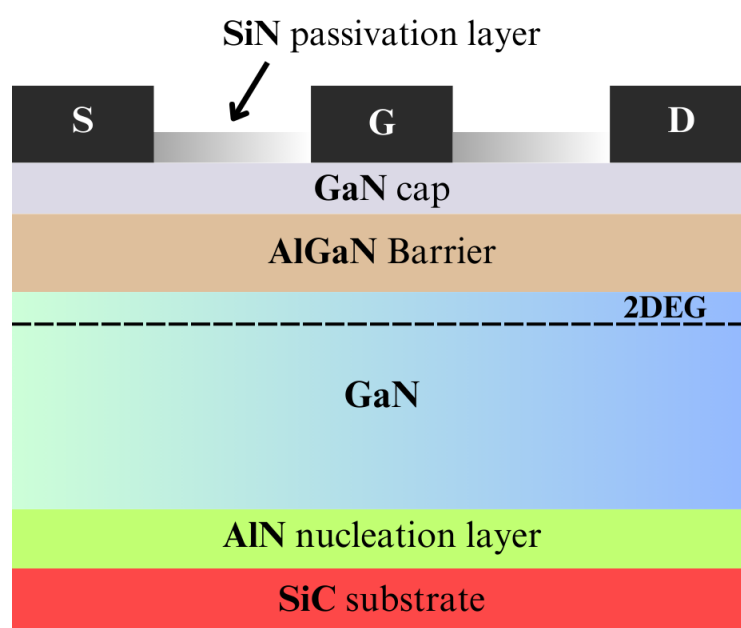


Figure 3. Schematic cross-section of GaN HEMT.

Gate leakage is a main contributor impacting the reliability of AlGaN/GaN HEMTs [28]. Theoretically, the electric field near the gate electrode can reach sufficiently elevated values that induce electron injection into the AlGaN layer via the tunneling effect. These electrons can demonstrate three possible behaviors as illustrated in **Figure 4** [29]: Accumulation on the AlGaN Surface, leading to surface leakage; migration between traps after injection into the AlGaN, generating a gate-to-drain leakage current; or being injected through the AlGaN into the 2DEG layer.

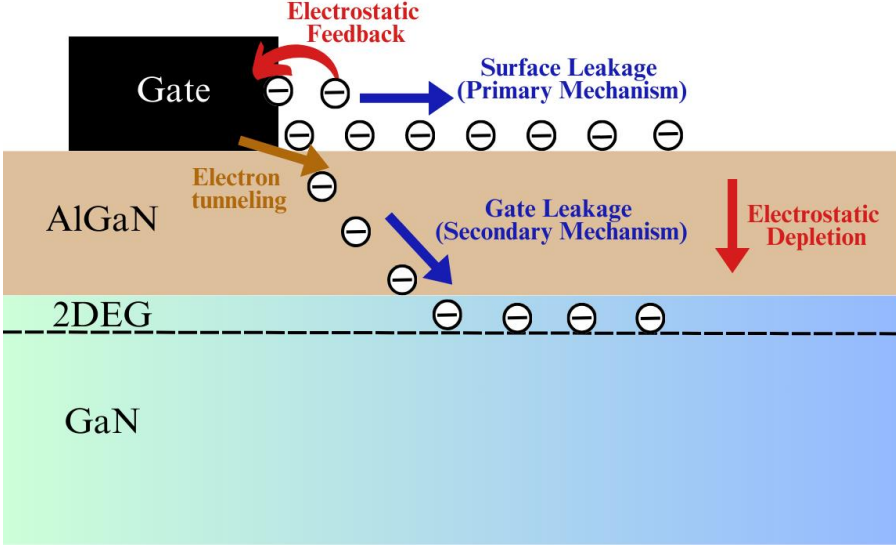


Figure 4. Electron tunneling leakage from the gate electrode and possible current paths [29].

Gate leakage can manifest both on the surface and within the bulk of the material. In practical applications, surface leakage is typically the dominant factor. To mitigate this effect research focuses on surface modifications (e.i., Passivation) [29-33], as well as the introduction of a GaN cap for reducing the gate edge electric field and improving surface morphology [34]. In contrast, bulk leakage is primarily attributed to defects resulting during the epitaxial growth, which create leakage paths for electrons and lower the gate Schottky barrier [35]. Overall, GaN HEMT’s reliability is heavily influenced by the electrical degradation resulting from interactions between the injected electrons and trap states.

Beyond gate leakage, thermally activated mechanisms also contribute to device degradation, through the degradation of feed metal interconnects, degradation of ohmic contacts, wear of gate metal, and delamination of passivation (**Figure 5**) [36].

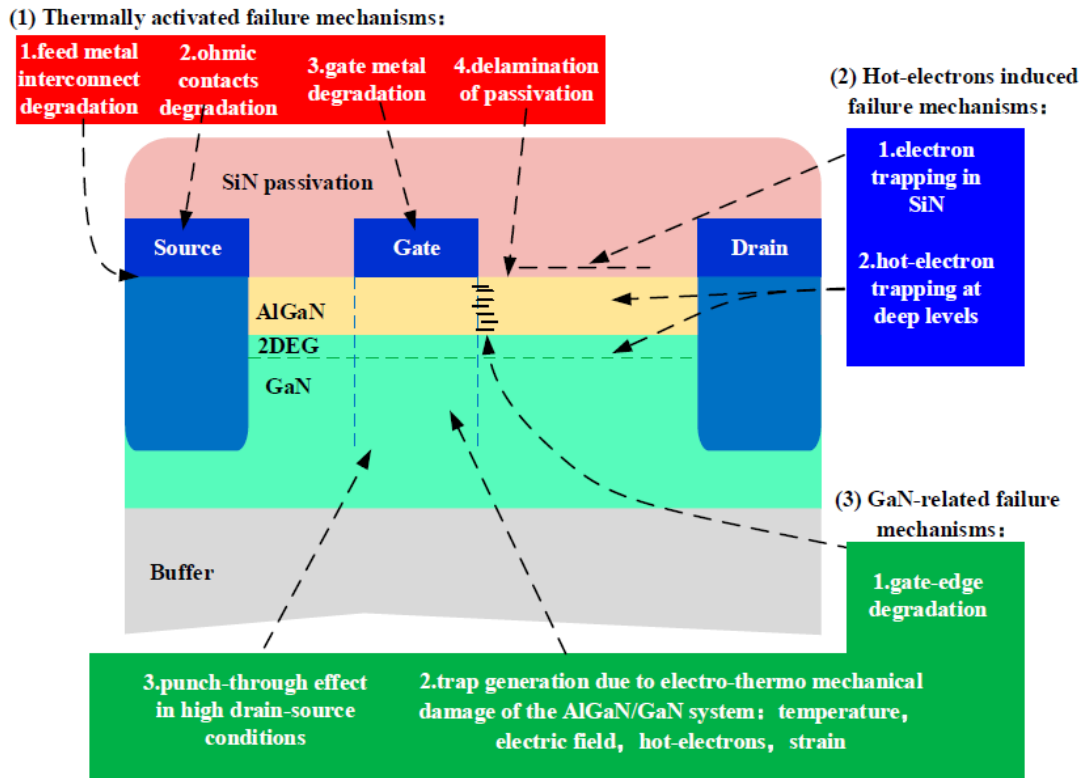


Figure 5. Schematic diagram illustrating the mechanisms influencing GaN HEMTs reliability [36].

2.2. Reliability of WBG power electronic packaging

The failure of WBG devices may also arise from issues related to the packaging. Given the critical role played by the packaging in the overall performance of these devices, ensuring its reliability is of paramount importance. Furthermore, adopting innovative designs and materials leads to developing packaging solutions capable of withstanding higher temperatures and thermal cycling. Various packaging configurations tailored to specific power chips operating conditions and application requirements are available, including flip-chip package, press-pack package, wire-bonding package, etc. The standard structure of packaging, an example of wire bonding package, typically comprises the semiconductor chip, bonding wires, encapsulant, substrate, solder layer, base plate and heat sink (Figure 6).

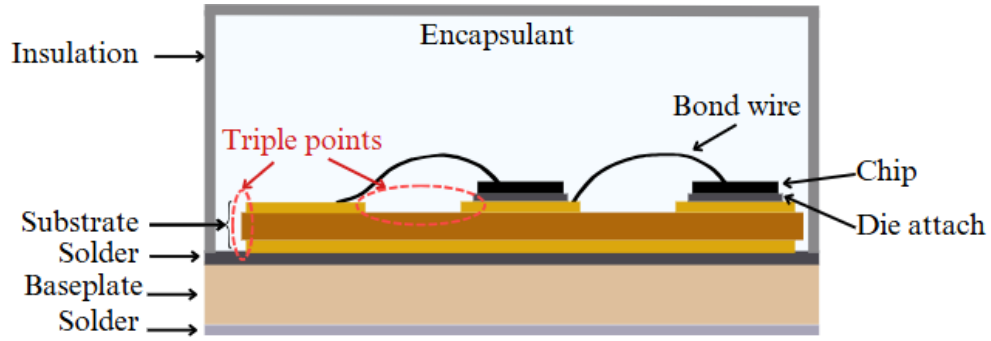


Figure 6. Schematic of power electronic wire bonding packaging [37].

Packaging reliability challenges primarily stem from thermomechanical fatigue and the discharge degradation of materials used for insulation. Thermomechanical fatigue occurs during power and thermal cycling due to mismatched Coefficient of Thermal Expansion (CTE) among the various materials. The degradation of insulation materials is driven by exposure to high applied voltage. The failure mechanisms associated with different components of the packaging are briefly introduced:

Solder

Solder serves as the material that joins the semiconductor chips to the substrate and/or the substrate to the base plate. The failure of solder joints arises primarily from the formation of micro-voids and the mismatch in CTE between the solder and the intermetallic layer/compound (IMC). The stress concentrated at the solder/ IMC interface during thermal cycling results in crack formation within the IMC adjacent to the solder, which progressively propagate under the influence of shear stress [38].

The solder lifetime, measured in terms of the number of cycles until failure, is expressed by the Coffin-Manson relationship [39]:

$$N_f = \frac{1}{2} \left(\frac{\Delta\alpha\Delta TL}{\gamma x} \right)^{c-1} \quad (7)$$

Where:

$\Delta\alpha$: CTE mismatch between the joint materials

ΔT : Temperature swing

L : Lateral size of solder

γ : Ductility factor of solder

x : Thickness of solder

c : Fatigue exponent

Bond wire

The wire bonding technique serves to connect the chips, and to the substrate, it is widely employed in power electronic packaging. However, its reliability is compromised by two primary fatigue mechanisms: bond wire lift-off and heel cracking. The bond wire lift-off occurs due to crack formation at the wire termination, resulting from shear stress and temperature fluctuations experienced by the bond wire [39]. On the other hand, bond wire heel cracking typically emerges after prolonged endurance tests [40]. These failure mechanisms are predominantly attributed to the CTE mismatch between the bond wire and the WBG chip materials [41-42]. The number of cycles to failure regarding the bond wire lift-off is mathematically described by the Coffin-Manson relationship [39]:

$$N_f = a(\Delta T)^{-n} \quad (8)$$

Where:

ΔT : Temperature swing

a and n : Calculated by thermal or power cycling experiments

Substrate

The substrate in WBG electronic packaging serves a dual purpose: providing insulation and mechanical support for chips and other components. Positioned between the power chip and the base plate, the substrate's CTE should closely match those of the chip and base plate. Commonly used substrates, such as direct bond copper (DBC) and direct bond aluminum (DBA), are generally made of a ceramic layer sandwiched by two metal layers. Failures in the substrates typically manifest as delamination of the metal layer and crack on the ceramic layer [43].

Encapsulant

Encapsulation serves to shield WBG devices from environmental influences and insulate the electric connections. The encapsulant plays a critical role in defining the operational temperature limits of WBG devices, with its adhesion quality being critical to ensure packaging reliability. Consequently, selecting materials capable of withstanding elevated temperatures, exceeding 300 °C, is essential [44].

Electric discharge

WBG-based devices operate under elevated temperatures and voltages, necessitating precisely engineered insulation structures and materials. Electric discharge failure is important during device development, with partial discharges frequently occurring at a critical triple junction - where the encapsulant, the substrate's metal edge, and the ceramic under the metal converge- regarded as the most electrically vulnerable point [45-46]. Enhancing packaging quality (i.e., optimizing the insulations), and employing composite materials to reduce electric field intensity below the discharge inception threshold, are generally efficient strategies to address this issue [47].

2.3. Reliability models for estimating device lifetime

Failure mechanism investigation is crucial for accurately assessing device conditions, enhancing their operational lifetime, and improving reliability. In this regard, several reliability models have been developed by researchers to calculate the remaining life of power electronic devices. These include Time-Dependent Dielectric Breakdown Models (TDDB) [48], stress strain models [49], and thermal cycling models [39], which are commonly used. These models were primarily designed for **Si-based devices**, however, (theoretically) their applicability and accuracy for WBG devices, experiencing similar failure modes, should be carefully evaluated [39].

Time-Dependent Dielectric Breakdown (TDDB) Models

TDDB arises from the prolonged application of high electric fields on the gate oxide, ultimately leading to the formation of a conduction path between the electrode and the substrate. This failure mechanism is driven by carrier injection which is influenced by both the electric field and temperature. Consequently, various TDDB models can be formulated based on these two factors. One such model is the thermochemical model developed by McPherson, which illustrates the impact of thermally activated trapping on the oxide dielectric degradation, expressed as [50]:

$$t = A \exp\left(\frac{H}{kT}\right) \exp[-\gamma(T)(E_B - E)] \quad (9)$$

Where:

t : Time-to-failure

A : Constant

H : Change in enthalpy required to activate the poly-filament growth at the breakdown

k : Boltzmann constant

T : Temperature

E_B : Breakdown strength

E : Applied electric field below E_B ,

γ : temperature-dependent parameter

with γ given by:

$$\gamma(T) = B + \frac{C}{T} \quad (10)$$

Where:

B and C : Constants

Another model was developed by Chen et al. and Schuegraf, based on the Fowler–Nordheim tunneling effect [51]:

$$t = \frac{A}{E^2} \exp\left(\frac{B}{E}\right) \quad (11)$$

Where:

t : time-to-failure

A and B : parameters related to the dielectric

E : Applied electric field

An additional model based on the Poole–Frenkel effect was proposed in [52]:

$$t \propto \frac{Q_{BD}}{E} \exp\left[\frac{q\left(\Phi_B - \sqrt{\frac{qE}{\pi\epsilon_0\epsilon_\infty}}\right)}{kT}\right] \quad (12)$$

Where:

t : Time-to-failure

Q_{BD} : Critical charge to breakdown

E : Applied electric field

q : Elementary charge

Φ_B : Trap depth

ϵ_0 : Vacuum permittivity

ϵ_∞ : Dielectric constant in the optical limit

Stress–Strain Models

Stress–Strain models describe the thermo-mechanical fatigue mechanisms (solder, bond wire, substrate delamination). These models estimate the number of cycles until device failure and are categorized into: stress-based, plastic strain-based, creep strain-based, energy-based, and damage-based models. One example of plastic strain-based model, known as the Englmaier model, is represented in [53]:

$$N_f = \frac{1}{2} \left(\frac{\Delta\gamma_t}{2\varepsilon_f} \right)^{\frac{1}{c}} \quad (13)$$

Where:

N_f : Number of cycles to failure

$\Delta\gamma_t$: Total shear strain

ε_f : Fatigue ductility coefficient

c : Related to temperature and frequency of the cycle

Energy-based models represent the largest subset of stress–strain models [49]. Within this category, Akay introduced a model based on total strain energy [43].

$$N_f = \left(\frac{\Delta W_{total}}{W_0} \right)^{\frac{1}{k}} \quad (14)$$

Where:

N_f : Mean cycles to failure

ΔW_{total} : Total strain energy

W_0 and k : Fatigue coefficients

Liang et al. proposed another model focusing on solder joint lifetime, based on both elastic and creep analyses [43] :

$$N_f = C(W_{SS})^{-m} \quad (15)$$

Where:

W_{SS} : Stress–strain hysteresis energy density

C and m : Material constants depending on temperature, determined through low-cycle fatigue testing

These studies demonstrated that while the models account for factors related to solder geometry and bond wire, they overlook the influence of the microstructure, which can lead to inaccuracies [39].

Thermal cycling model

Thermal cycling is a major factor contributing to WBG chip failure and packaging fatigue. Thermal cycling models are frequently based on the Coffin-Manson relationship, expressed as [39]:

$$N_f = \frac{\delta}{(\Delta T)^\alpha} \quad (16)$$

Where:

N_f : Number of cycles to fail

ΔT : Temperature swing of the cycle

δ and α : Parameters related to the material and test setup respectively

A revised version of the Coffin-Manson model, tailored to predict solder fatigue and other failure mechanisms, is formulated as [54]:

$$N_f = A f^{-a} \Delta T^{-b} G_{Tmax} \quad (17)$$

Where:

N_f : Number of cycles to fail

ΔT : Temperature swing of the cycle

f : Cycling frequency

A : a coefficient

a and b : cycling frequency and temperature exponents respectively

G_{Tmax} : Arrhenius term evaluated at the maximum temperature in each cycle

These reliability models have been developed by researchers to predict the lifetime of Silicon-based power electronic devices. However, with the increasing deployment of WBG-based devices in high-voltage and high-temperature applications, the associated reliability challenges are expected to intensify. Therefore, their theoretical applicability and accuracy for WBG devices, experiencing similar failure modes, must be carefully evaluated.

Chapter 3

Reliability assessment of GaN HEMTs: Investigating Stress effects induced by novel packaging using Raman spectroscopy

This chapter explores the evaluation of stress induced by electronic packaging in GaN HEMTs using Raman spectroscopy. It begins with a general introduction to residual stress in electronic packaging, followed by a brief discussion of the non-destructive techniques employed for stress assessment, before transitioning to the experimental study. An introduction to the GaN HEMT device is provided to set the context of the study. The central focus of the chapter is an experimental analysis of the impact of a novel wire-bonding-free packaging design on stress distribution within the semiconductor layers of the GaN HEMT device. Raman spectroscopy is used to accurately quantify the localized stress distribution.

3.1. Residual Stress in Electronic Packaging

3.1.1. Introduction

With the rapid advancements in the electronics industry sector, the demand for highly reliable packaging solutions is becoming critical. However, failures induced by residual stress present a significant challenge, posing a major barrier to the progression of electronic packaging technologies. Residual stress in electronic components may be implemented at various stages of the fabrication process, significantly influencing materials properties and leading to structural degradation. Residual stresses in the electronic packaging materials significantly impact the entire device performance, including bond strength, thermal cycling resistance, corrosion resistance, and other essential properties [55]. As such, residual stress is recognized as a major contributor to packaging failures. Therefore, investigating and evaluating the residual stress generated in the packaging is essential, and plays a significant role in enhancing device reliability [56]. In fact, residual stress refers to the stress present within an object in the absence of any externally applied forces. It maintains the internal equilibrium of an object when no stress is being transmitted from its surface [55]. The internal stress can be classified into two categories based on its range of influence, macroscopic stress and microscopic stress [56-57]. The macroscopic stress, refers to as residual stress, occurs at the macroscopic level, and can be evaluated using conventional physical techniques, while the microscopic stress is distributed on a smaller scale, divided into two classes. Microstructural stress is present at the individual grains level within the material. While Intragranular substructural stress is localized within the single grain boundaries, impacting its structure. Understanding the different classes of residual stress and the factors leading to its formation helps evaluate the material's behavior.

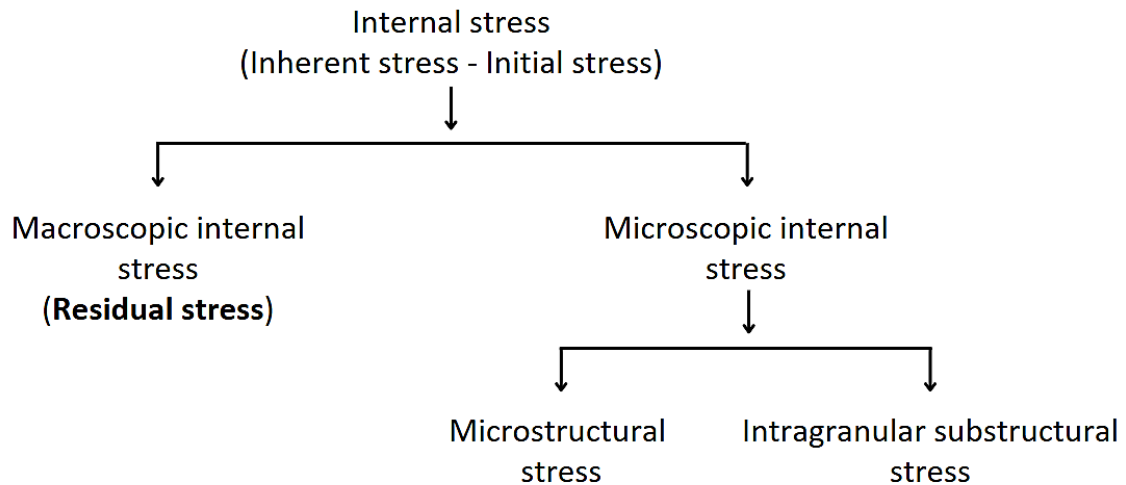


Figure 7.Classification of internal stress.

Factors leading to macroscopic residual stress:

Residual stress mainly arises from non-uniform plastic deformation, thermal factors and chemical effects [58]. The non uniform plastic deformation occurs during processing methods such as extrusion or cutting, etc., leading to material segmentation with varying levels of plastic deformation. These variations generate compressive or tensile stresses between the affected regions, resulting in residual stress. Residual stress can also be generated by temperature gradients during heating or cooling processes, causing irregular thermal expansion and contraction within the material leading to thermal stress. Additionally, structural changes such as phase transformations can lead to uneven volume changes, generating stress. Thermal-induced plastic deformation can further alter the material's mechanical properties, impacting the stress levels. Additionally, the residual stress may result from chemical and physical transformations between a material's internal and external regions, leading to differences in expansion coefficients or volumes, or densities inducing tensile or compressive stress. Each of these factors contributes to the residual stress influencing material performance and reliability.

Factors leading to microscopic residual stress:

Microscopic stress can originate from multiple factors, including crystal anisotropy, grain-level plastic deformation, and the formation of precipitates, inclusions, or phase transformations

[55]. In an electronic device, the microscopic stress within grains typically affects metals and often results from the anisotropic properties of crystals, (crystal orientation, elastic moduli, ...). Since grains in a material have diverse orientations, they deform variously under stress, generating internal stress, particularly during plastic deformation. Microscopic stress can also result from plastic deformation within grains, such as the accumulation of dislocations or their interaction with grain boundaries, creating microstructural defects, which contribute to residual stress at the microscopic level. As well as the formation of precipitates or inclusions or phase transformation in the microstructure contributes to residual stress.

3.1.2. Non-Destructive evaluation of stress and strain in electronic packaging

With the growing requirements of modern electronic devices, packaging solutions are becoming increasingly compact and complex, leading to a rise in associated failure mechanisms. Assessing these factors is important for mitigate packaging defects, and enhancing device reliability [59-60]. Among these challenges, residual stress plays a critical role, as it induces multiple packaging failure mechanisms. Notable examples include warping, caused by the CTE mismatch between various packaging materials during curing and cooling. Additional issues include fracture formation in solder balls, solder material fatigue, and crack formation within the packaging structure. These phenomena can severely compromise the performance and reliability of the device [61-63]. The evaluation of stress and strain can be performed using various approaches, broadly categorized into destructive and non-destructive techniques. Among the non-destructive methods are X-ray diffraction (XRD), photoluminescence (PL), terahertz time-domain spectroscopy (THz-TDS), and micro-Raman spectroscopy (μ RS). Each technique has unique advantages and limitations. While XRD and THz-TDS offer high sensitivity, their relatively low spatial resolution (mm scale) limits their applicability for heterogeneous structures. On the other hand, micro-Raman spectroscopy has emerged as a highly effective tool for measuring localized strain and residual stress, with the high spatial resolution (μ m scale) required for intricate structures [64].

The following section presents a comprehensive analysis of the impact of device packaging, evaluating the distribution of residual stress within GaN HEMT using Raman spectroscopy.

3.2. Assessment of Stress induced by Novel packaging in GaN HEMT devices using Raman Spectroscopy

AlGa_xGa_{1-x}N High Electron Mobility Transistor

GaN possesses a Wurtzite-type hexagonal crystal structure, with its primary axis, c-axis, aligned along the length of the hexagonal column. The notable difference in electronegativity between nitrogen (3.04 on the Pauling scale) and gallium (1.81 on the Pauling scale) leads to electric polarization. Although polarization is balanced within the bulk of the material, spontaneous polarization develops along the c-axis due to the asymmetry at the cut face. When epitaxial layers of Al_xGa_{1-x}N are deposited on GaN, tensile strain results from their differing lattice constants, inducing an additional polarization known as piezoelectric polarization P_{PE} , that adds to the spontaneous polarization P_{SP} . These combined polarization effects generate an electric field that bends the conduction band downwards at the interface, creating a triangular potential well at the AlGa_xN/GaN interface. To neutralize the polarization-induced charge density, free electrons accumulate in this confined region at the heterointerface, forming a two-dimensional electron gas (2DEG). This 2DEG is a defining characteristic of nitride-based devices, exhibiting high electron mobility, and underpinning the operational principle of GaN-based field-effect transistors (FETs) such as HEMTs.

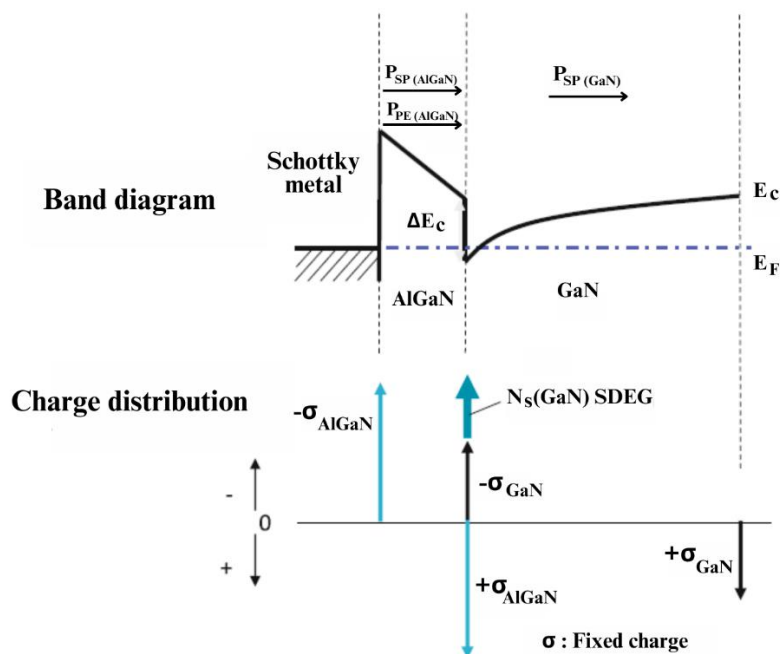


Figure 8. Band diagram of Schottky junction formed over Al_{0.25}Ga_{0.75}N grown on Ga-face GaN [22].

AlGaN/GaN heterostructures are highly valued for high-speed and high-power electronic applications due to the exceptional electron mobility and high electron density inherent to the 2DEG layer. The sheet carrier density of the 2DEG, denoted as n_s can be controlled by implementing a Schottky metal electrode on the AlGaN surface. The maximum sheet carrier density of the 2DEG can be expressed using the following expression:

$$n_s(x) = \frac{+\sigma(x)}{q} - \left[\frac{\varepsilon_0 \varepsilon_{\text{AlGaN}}(x)}{d_{\text{AlGaN}} q^2} \right] \cdot [q\Phi_B(x) + E_F(x) - \Delta E_C(x)] \quad (18)$$

Where d_{AlGaN} and $\varepsilon_{\text{AlGaN}}$ represent the thickness and the permittivity of the $\text{Al}_x\text{Ga}_{1-x}\text{N}$ barrier layer respectively. $q\Phi_B$ denotes the Schottky barrier height of the gate contact, while E_F is the Fermi level with respect to the conduction-band-edge of GaN. Additionally, ΔE_C indicates the conduction band offset at the AlGaN/GaN interface. The 2DEG formed in AlGaN/GaN heterostructures typically demonstrates high sheet carrier density, approximately 10^{13} cm^{-2} , along with impressive mobility values ranging from 1000 to 2000 $\text{cm}^2 \text{ V}^{-1} \text{ s}^{-1}$. [65] In a standard AlGaN/GaN HEMT, the current moving through the 2DEG channel, between the source and drain contacts, is controlled by applying a negative voltage to a Schottky contact, which works as the transistor's gate. Such device operates in a normally-ON state. The output current can be regulated by applying a negative gate bias, until the threshold voltage (V_{th}) is reached, at which point the Fermi level is shifted below the conduction band edge of the AlGaN layer, leading to the depletion of the 2DEG channel. The threshold voltage is defined as follows:

$$V_{\text{th}} = \Phi_B - \Delta E_C - \frac{qN_{D_{\text{AlGaN}}} d_{\text{AlGaN}}^2}{2\varepsilon_0 \varepsilon_{\text{AlGaN}}} - \frac{\sigma}{\varepsilon_0 \varepsilon_{\text{AlGaN}}} d_{\text{AlGaN}} \quad (19)$$

Where $N_{D_{\text{AlGaN}}}$ represents the doping density of the AlGaN barrier layer, measured in atoms/ cm^3 [65]. Clearly, the presence of the 2DEG in the AlGaN/GaN heterostructures resulted in GaN HEMTs inherently operating in depletion mode (d-mode), making them normally-ON devices. In standard normally-ON HEMT configurations, the AlGaN layer typically has a thickness of around 25 nm, with an aluminum concentration between $x=0.25$ and $x=0.30$, and 2DEG sheet carrier density generally around 10^{13} cm^{-2} , resulting in negative threshold voltages (V_{th}) of approximately $-1 \div -4 \text{ V}$ [65-66]. While depletion-mode (d-mode) devices have proven effective for RF applications, normally OFF devices with $V_{\text{th}} > 0$ (e-mode) are generally preferred

in power electronics. This preference is due to safety considerations and ease of control in the absence of input or control (gate) voltage (gate driver failure), when the GaN power device, and the associated circuit, is off. However, achieving reliable normally-OFF operation is a significant challenge in the advancement of HEMT technology [22]. To shift the threshold voltage into the enhancement mode and enable normally OFF characteristics, various procedures have been reported in the literature. These include thinning the AlGaN layer to decrease the 2DEG carrier concentration, reducing the 2DEG concentration by lowering the aluminum content, and increasing the gate material's work function. Each method reduces the current handling capacity. Among these approaches, enhancing the work function of gate material through the use of a p-type GaN gate (p-GaN gate), as illustrated in **Figure 9**, stands out as one of the most promising techniques and the only commercially available today. It is clearly evident (in **Figure 9**) that the introduction of the p-GaN gate into a HEMT raises the conduction band of the AlGaN, resulting in the depletion of the 2DEG and thus the formation of a normally off HEMT [22, 66].

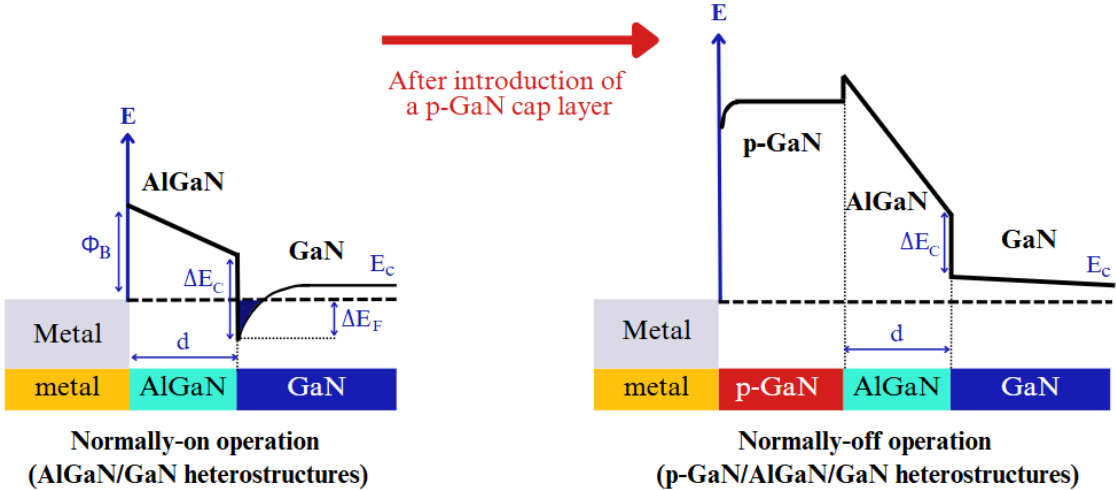


Figure 9. Schematic diagram illustrating the operating principle of a normally-off HEMT with a p-GaN gate [66].

3.2.1. Background of study

The widespread adoption of GaN-based electronics is often constrained by the limited commercial availability of bulk GaN substrates [67]. Consequently, GaN devices are typically fabricated on alternative substrates such as sapphire (Al₂O₃), SiC, and silicon [68]. Nevertheless, Si substrate is favored due to its cost-effectiveness and availability in larger wafer sizes e.g., 12 inch wafers, compared to the smaller dimensions of SiC and Al₂O₃ substrates (6 or 8 inches) [69]. Furthermore, silicon mature technology and fabrication processes enhance

its suitability. Also, the integration of an AlGaIn modulation layer on silicon substrates plays a pivotal role in mitigating defects within GaN semiconductor materials. This, along with the higher costs associated with SiC, has solidified Silicon's position as the preferred substrate for electronic manufacturing. Although silicon is the predominant choice and more commonly used for electronic applications, there are applications where SiC or sapphire substrates may be more appropriate depending on the performance requirements and characteristics of the devices being developed.

The packaging of electronic devices is paramount for ensuring their functionality, reliability, and protection against external environmental factors such as chemicals, light exposure, and mechanical impacts [64]. Additionally, effective packaging guarantees a good connection between the chip and the circuit board. Consequently, extensive research has been conducted to identify the optimal packaging solutions for the desired applications, exploring various designs and materials [70]. Among the numerous factors that can affect both the performance and lifetime of electronic devices, the impact of mechanical stress on the chip surface is rarely taken into account [71]. Due to the lattice mismatch between the AlGaIn/GaN HEMT and the chosen substrate, along with the difference in thermal expansion coefficients [72], there is a significant built-in strain/stress capable of modifying the overall performance of GaN-based devices. Moreover, regardless of the type of substrate employed, AlGaIn/GaN HEMTs must be encapsulated within specific packaging. Minimizing the stress and strain experienced by the devices has been one of the main goals of the research on new packaging materials and designs. Typically, stress and strain can be induced mechanically and thermally; therefore, for different kinds of device, different materials have to be employed. For instance, polymer-based packaging materials provide flexibility and shock absorption, while ceramics offer high stiffness and thermal stability. Furthermore, the overall effect on the device lifetime and performances induced by the packaging is not predictable since there are many elements that constitute the packaging (e.g., wires, solders, die, etc. [71]).

This study investigates a commercial AlGaIn/GaN HEMT equipped with wire-bonding-free packaging designed to be integrated around the chip to save space and optimize thermal dissipation. The investigation proposed in this study emphasizes the critical importance of selecting and designing appropriate packaging solutions to ensure optimal performance and lifetime suitable for the device's mission profile [73]. The proposed packaging comprises a lead

frame structure onto which the semiconductor die is soldered using a silver sinter paste. The intermediate space is leveled using fiberglass. Holes are then dug into the glass fiber, into which copper is deposited, and subsequently etched down selectively using a dedicated mask, leaving the final connections. However, the packaging encapsulation process may inadvertently introduce unwanted additional mechanical residual stresses across various layers of the device and at the critical die/package interface. These additional stresses can be exacerbated under normal operating conditions due to the mismatch in thermal expansion coefficients between the various materials comprising the device [74]. This phenomenon results in a continuous stream of reliability challenges in the field of advanced packaging technology.

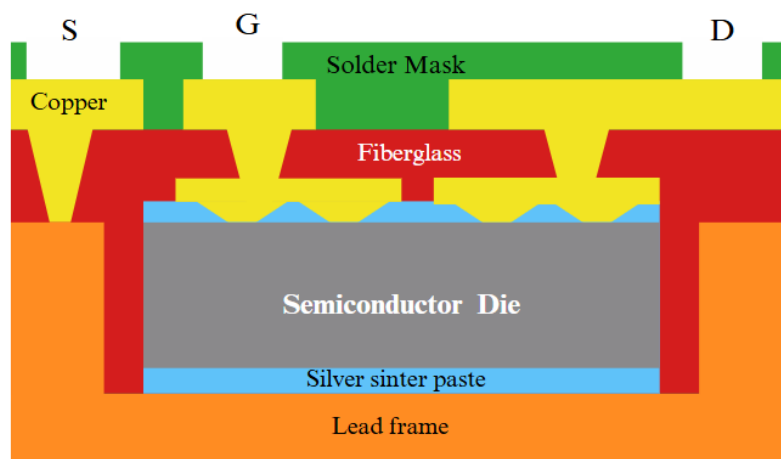


Figure 10. Wire-Bonding-free packaging design integrated around the semiconductor die.

We focus our investigation on the impact of packaging on stress distribution within the semiconductor layers of the HEMT device. In particular, thermomechanical stress can contribute to premature device failure through various mechanisms, including cracking of the packaging, die, wires, and solder bump, as well as delamination at critical interfaces. Understanding the aging effects and failure mechanisms induced by thermal and thermomechanical phenomena on electronic devices is currently an active area of research [71, 75], emphasizing the need to evaluate the built-in stress and strain to accurately estimate device lifetimes and reliability. To investigate this issue, micro-Raman spectroscopy stands out as a powerful non-contact, local, and non-destructive characterization technique [76] capable of assessing localized residual strain and stress throughout the entire thickness of the AlGaN/GaN HEMT [77] with sub-micron lateral resolution. Micro-Raman spectroscopy operates on the principle that when crystals are subjected to mechanical stress, the

frequencies of their characteristic Raman modes shift due to stress-induced crystal deformations [64]. The Raman spectrum of GaN features eight distinct optical modes, four of which are Raman-active in our geometry: A1(TO), E1(TO), E2(low), and E2(high) [78]. Among the detectable phonon modes, the E2(high) mode, which arises from atomic oscillations along the c-plane, is particularly sensitive to lattice strain elongations, making it an effective marker for quantifying residual stresses in AlGaIn/GaN HEMT devices [79]. According to the previous consideration, the frequency center (ω) of the E2(high) mode was monitored along a vertical axis spanning from the bottom to the top of the HEMT devices, effectively crossing the entire AlGaIn/GaN heterostructure. This comprehensive analysis was conducted comparing the results acquired on two AlGaIn/GaN HEMTs, one (HEMT-PD) with the package and another (HEMT-B) bare. This approach, along with employing a specific strain/stress relationship, enables correlation of the optical data as obtained through micro-Raman spectroscopy with the residual stress present within the layers of the devices under investigation [68, 80-82].

Knowledge of the aforementioned aspects not only helps evaluation of the performance of GaN-based electronics in various applications, but also provides valuable information for the understanding of the unknown failure mechanisms which compromise their lifetime. The impact of the packaging on the stress of a GaN-based HEMT has never been investigated, but this aspect must be taken into account to design the packaging of high-performance devices. In **Table 2**, for ease of reading, a list of all the symbols and notations used hereafter is provided.

Table 2. List of symbols and notations used in this chapter.

Symbols and Acronyms	Description
MOSFET	Metal–Oxide–Semiconductor Field Effect Transistor
HEMT	High-electron-mobility transistor
HEMT-B	Bare HEMT
HEMT-PD	Packaged HEMT
WBS	Wide-Bandgap Semiconductors
2-DEG	Two-dimensional electron gas
RT	Room temperature
MOCVD	Metal–Organic Chemical Vapor Deposition
SEM	Scanning Electron Microscopy
DPSS	Diode-Pumped Solid State
CCD	Charge-Coupled Device
ω	Measured frequency center of the E2(high) Raman peak
ω_0	Stress-free frequency center of the E2(high) Raman peak
$\Delta\omega$	Frequency shift of the E2(high) Raman peak

σ	Residual stress
K	Stress coefficient

3.2.2. Experimental section

GaN HEMT Device Under Study

In this study, we explore the influence of packaging on localized stress by conducting a comparative analysis of the Raman spectral characteristics of the packaged (PD) AlGaN/GaN HEMT and its unpackaged (bare, B) AlGaN/GaN HEMT, both provided STMicroelectronics S.r.l. **Figure 11** presents images of the bare AlGaN/GaN HEMT (a) alongside its packaged counterpart (b).

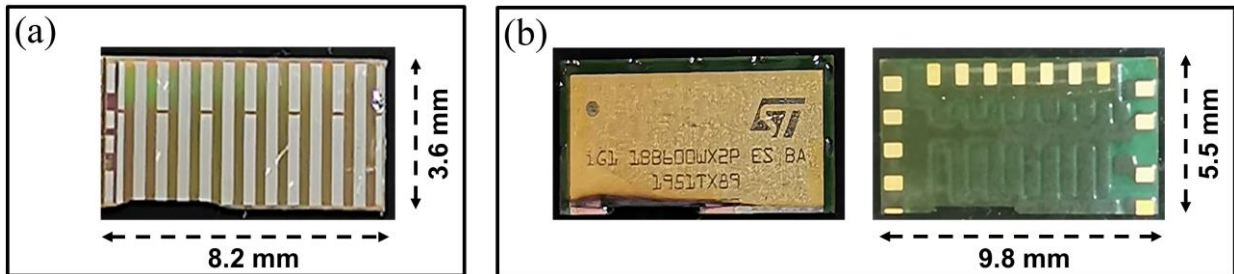


Figure 11. Photographs of the AlGaN/GaN HEMT-B (a) and AlGaN/GaN HEMT-PD (b).

AlGaN/GaN HEMTs are fabricated by STMicroelectronics S.r.l. using the Metal-Organic Chemical Vapor Deposition (MOCVD) technique. The fabrication process initiates with the growth of a 5 μm thick GaN(0001) layer on an n-Si(111) substrate, which is subsequently followed by the deposition of a 16 nm $\text{Al}_{0.25}\text{Ga}_{0.75}\text{N}$ barrier layer. Afterwards, a p-GaN capping layer is added to the gate region, after which metallic contacts are deposited to establish electrical connectivity. Subsequently, a SiO_2 passivation layer is deposited to ensure electrical isolation for the AlGaN/GaN HEMTs, a, and ultimately, the packaging. **Figure 12** provides a cross-sectional view of the AlGaN/GaN HEMT structure.

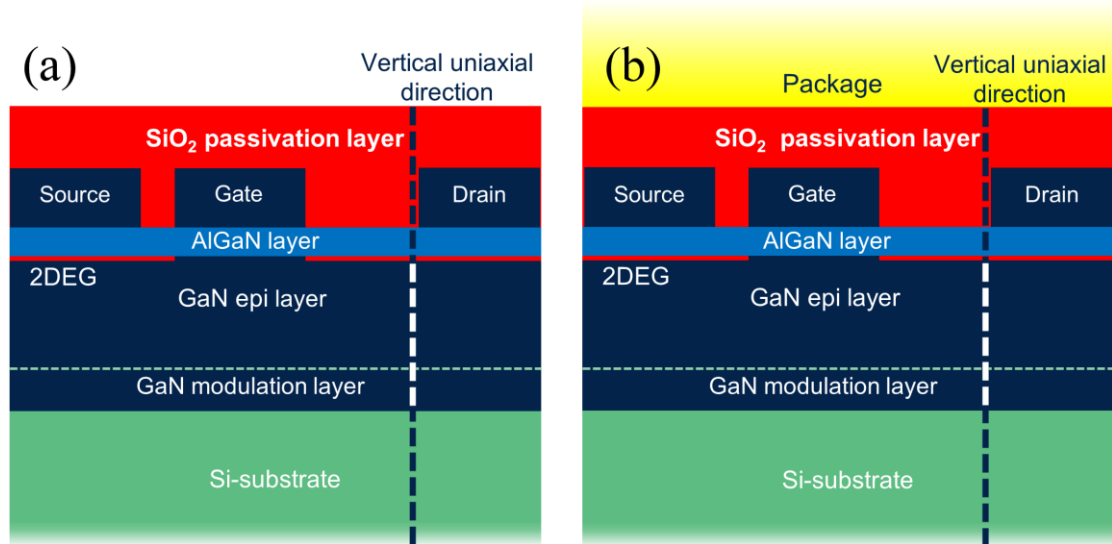


Figure 12. Schematic cross-sectional representation (not to scale) of the internal structure of the unpackaged AlGaIn/GaN HEMT-B (a) and the packaged AlGaIn/GaN HEMT-PD (b) investigated in this study. The vertical dashed line indicates the uniaxial direction along which micro-Raman measurements were performed.

As displayed in **Figure 12**, the GaN layer can be split into two layers. The first layer, approximately 2 μm thick, serves as a strain modulation layer at the GaN/Si interface, significantly reducing the lattice mismatch between the two semiconductors. In this way, the GaN epitaxial layer will experience a lower built-in mechanical stress. The employment of the p-GaN cap gate, along with the equilibrium between the aluminum molar fraction and the thickness of the AlGaIn layer, enables the normally-off HEMTs with a reasonably positive threshold voltage [66]. Additionally, the formation of a two-dimensional electron gas (2-DEG) sheet at the GaN epitaxy/AlGaIn interface results in efficient charge depletion processes. Two identical devices were prepared: one was at the wafer level (HEMT-B), while the other was encapsulated (HEMT-PD). The primary objective of this comparative analysis was to analyze their Raman spectral characteristics and to highlight the impacts of encapsulation on residual stress within the devices .

To obtain the Raman spectra of the device layers, it was necessary to perform a transverse cut on the samples. However, a simple cutting method followed by mechanical polishing is inadequate, as this approach would result in very high surface roughness. Such roughness could introduce significant additional stress to the layers, compromising the accuracy of the measurements. To mitigate these issues, an ion beam milling technique was employed on both samples. The ion milling procedure employed for preparing the samples involves the amorphization of the semiconductor's surface layers; thus, in principle, the Raman spectrum could be influenced by the cleaning treatment. However, this would lead only to a slight peak

broadening without significantly affecting its position. In this regard, it can be observed that thanks to the focal depth of the objective used, limited to about 500nm, with a correct focus, it is possible to ensure that most of the Raman signal comes from the deeper layers of the material, and only a minimal part from the amorphized surface, thus reducing to a minimum the influence of surface modifications on the spectral data [83-85]. To attest the quality of the growth and to confirm the absence of defect or phase transformations induced by the ion milling process, a Scanning Electron Microscopy (SEM) analysis was performed on a milled HEMT-PD device. The SEM analysis was conducted using a beam energy of 5 keV. **Figure 13(a)** presents a cross-sectional view of the HEMT-PD device following the ion milling process, while **Figure 13(b)** shows a magnified view of the red-framed area in **Figure 13(a)**, which corresponds to the specific region where the stress distribution was studied. The detailed structure of the device across all layers is clearly visible, with each layer distinctly identified and labeled in both figures.

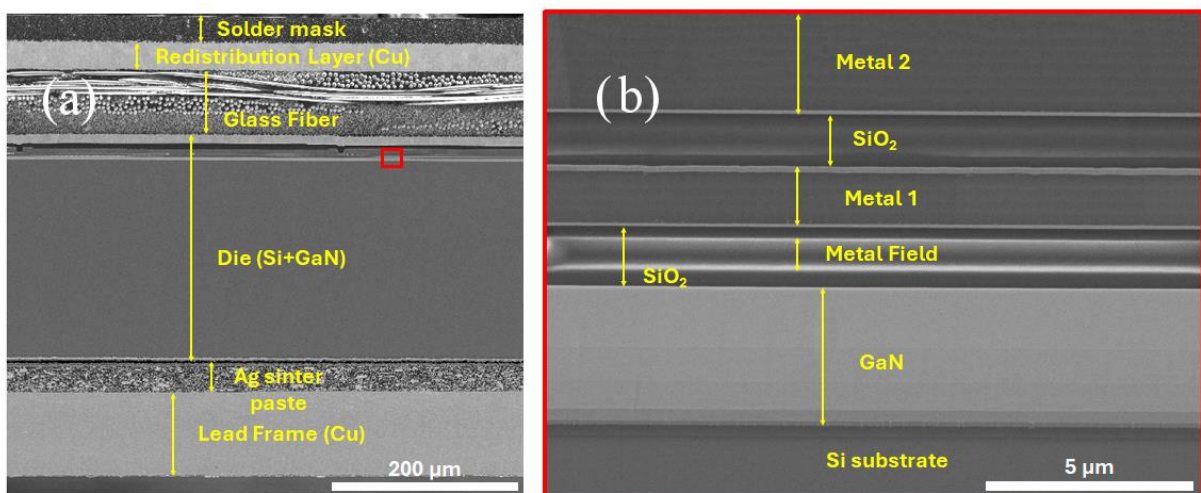


Figure 13. (a) SEM image of the cross-sectional view of the HEMT device following the ion milling process, and (b) a magnified SEM image of the region highlighted within the red square in the image (a). The distinct layers comprising the device are clearly visible and appropriately labeled.

μ-Raman measurements

Micro-Raman spectra were systematically collected along the cross-sections of both HEMT-B and HEMT-PD samples to investigate the spectral changes induced by the residual stress across the device layers [86]. The measurements were conducted at room temperature (RT) using an NT-MDT NTEGRA Spectra confocal micro-Raman system operating in reflection mode. This sophisticated system is based on a MS3504i spectrometer from SOL Instruments Ltd.

(Augsburg, Germany) and is equipped with a 2400 lines/mm grating blazed at 400 nm. For excitation, a 30 mW linear polarized DPSS laser operating at 532 nm (Nd:YAG laser mod GLK 3250 T01, LASOS Lasertechnik GmbH, Jena, Germany) was utilized. A neutral filter was incorporated into the laser path to prevent excessive heating of the samples, limiting the maximum power incident on the sample surface to approximately 400 μW . This precaution is critical as it prevents any displacement of the Stokes peak that could arise from temperature increases [87]. An IDUS-401 CCD camera from Andor, Oxford Instruments Italia s.r.l. (Milan, Italy), cooled by a triple Peltier stage, served as the detector.

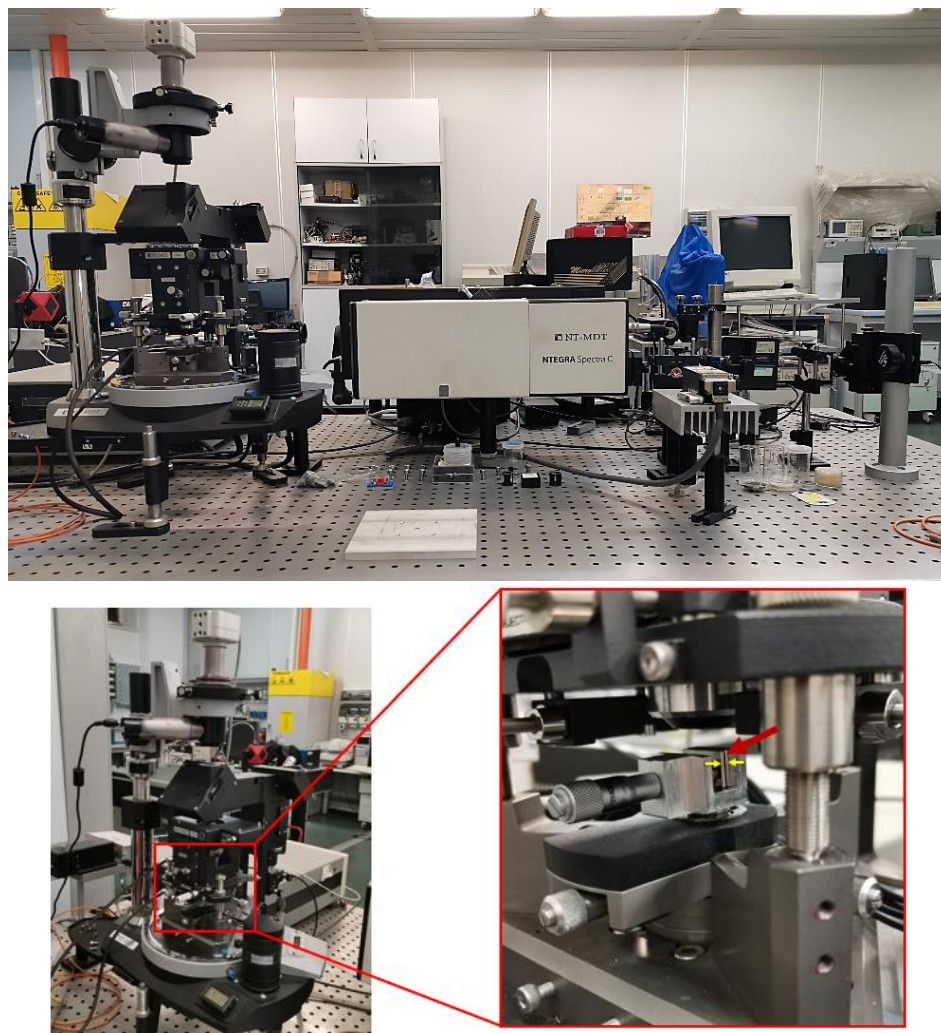


Figure 14. Raman spectroscopy setup.

The spectral range analyzed in this study spanned from 500 to 600 cm^{-1} , with a resolution well below 1 cm^{-1} . A 100 \times objective lens with a working distance of 6 mm and a numerical aperture of 0.75 was employed to focalize the laser beam onto the sample surface, resulting in a spot size of approximately 350 nm. All measurements were conducted in backscattering geometry,

utilizing the microscope objective to capture the scattered light. The samples were positioned with their cross-sections facing upwards, employing a homemade sample holder set-up developed specifically for this study, as illustrated in **Figure 15**. Importantly, during the experiment, the spring applied no force to the device; it merely secured the sample in place. For each sample, a total of 128 micro-Raman spectra were collected along a direction orthogonal to the layers' growth, with a step size of 78 nm, thus covering a total path of 10 μm path and crossing through the GaN heterostructure (refer to **Figure 12**). Each spectrum was acquired with an exposure time of 30 s, and the entire data collection process took approximately 64 minutes.

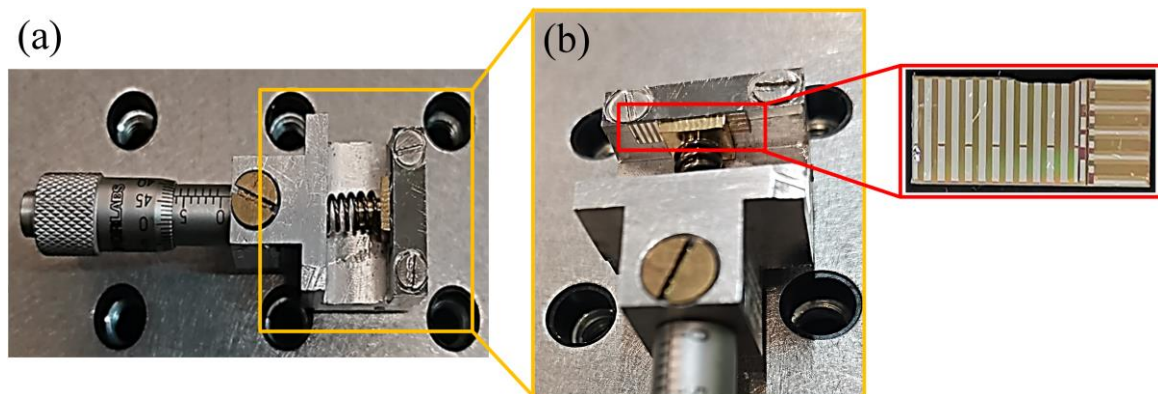


Figure 15. (a) image of the homemade sample holder (b) a detailed view highlighting the precise positioning of the sample within the holder.

3.2.3. Results and Discussion

Figure 16(a) presents an optical microphotograph of the cross-section of the sample used in this study. Specifically, 128 Raman spectra were acquired along a vertical line traversing the layers, as indicated by the red line in **Figure 16(a)**. This approach enables us to observe how the Raman peaks shift from one layer to another, thereby highlighting the presence of stress at the interfaces. Since obtaining a sufficient signal-to-noise ratio required integrating the signal for a very long time, we chose to proceed with acquiring the Raman spectra along a line rather than performing a full Raman mapping. Indeed, the latter would have required extremely long measurement times, potentially leading to results affected by thermal drift and unpredictable variations in experimental conditions, without providing additional useful information beyond what is obtained from the line scan. **Figure 16(b)** displays the 1D map of

the Raman spectra acquired during the experiment along the 10 μm investigated (i.e., the Raman intensities acquired point by point plotted against the Raman shift).

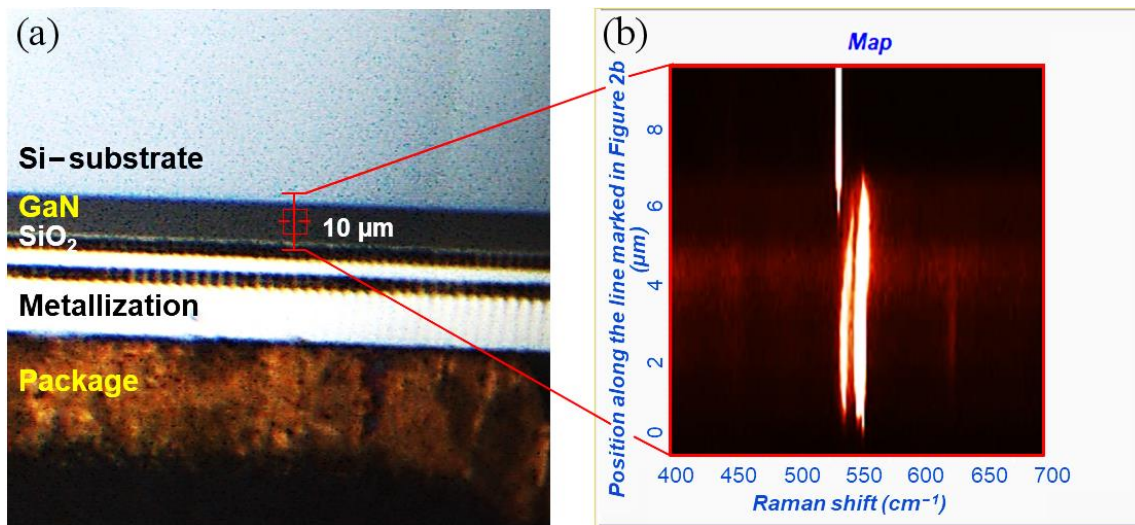


Figure 16. High-magnification view of the AlGaIn/GaN HEMT-PD heterostructure (a) and the resulting one-dimensional Raman intensity map acquired along the 10 μm scanned path.

The spectral characteristics exhibit a notable shift when moving from silicon through the layers of GaN, indicating the presence of intrinsic stress within the material. Specifically, the Raman peaks associated with GaN in the lower section of the map begin to redshift as the measurement area approaches the GaN/Si interface. The frequency center of Raman peaks is intimately correlated to the interatomic potential between atoms [88]. Consequently, any alterations in this potential due to intrinsic stress within the crystal result in Raman shifts of specific and characteristic vibrational modes of the structure, regardless its origin [88].

Figure 17 illustrates typical micro-Raman spectra acquired at two critical locations: the GaN epitaxy layer (**Figure 17(a)**) and the GaN/Si interface (**Figure 17(b)**). The micro-Raman profile obtained from the GaN epitaxy layer (**Figure 17(a)**) reveals distinct spectral contributions at 531.7 cm^{-1} , 558.7 cm^{-1} , and 567.7 cm^{-1} , which correspond to the A1(TO), E1(TO), and E2(high) modes of the hexagonal wurtzite structure, respectively. At the GaN/Si interface (**Figure 17(b)**), as expected, a characteristic Si Raman peak centered at 521.4 cm^{-1} , arising from the silicon substrate, was clearly distinguished. Additionally, the Raman mode derived from the GaN structures, E₂(high) at 569.6 cm^{-1} , was also observed.

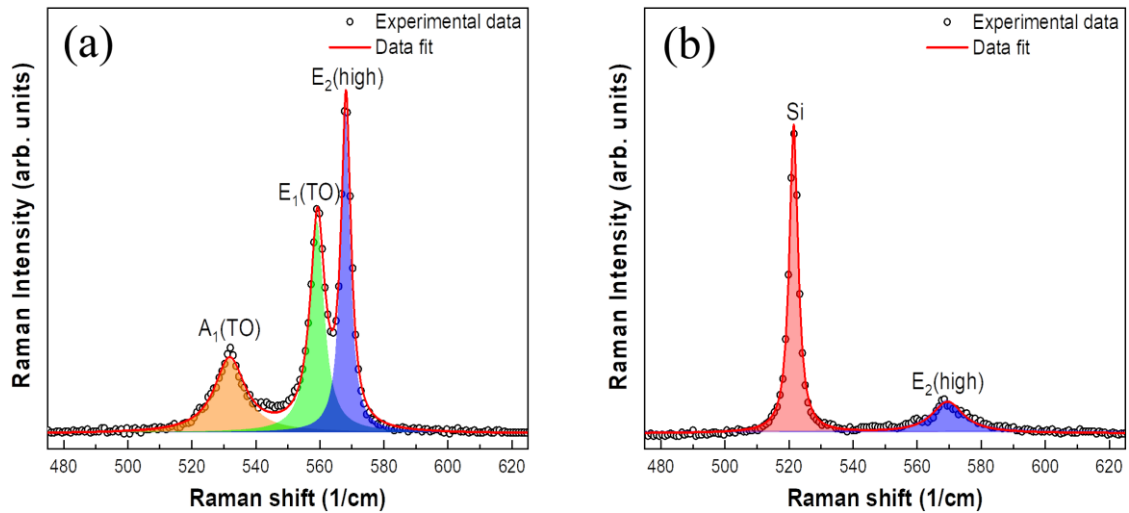


Figure 17. Micro-Raman spectra acquired at the GaN epitaxy layer (a), and at the GaN/Si interface (b) of HEMT-B device.

The observed frequency shift of the E2(high) mode, occurring from the GaN epitaxy layer to the GaN/Si interface, can be attributed to the differing stress conditions in these two regions.

Since the main purpose of this study was to identify the presence of stress among the layers using Raman spectroscopy, it was imperative to measure the Raman peak positions with the highest precision. Despite the rather high spectral resolution of the measurement instrument, obtaining accurate information required fitting the experimental data using an appropriate fitting model. In particular, the model used consists of three Lorentzian lines describing the Raman modes of GaN, A1(TO), E1(TO), and E2(high), and takes also into account the presence of silicon when needed. Each of the 128 spectra was fitted using this model described above to extract the characteristic frequency ω of the modes at each point along the scanned line. Notably, the E2(high) mode was found to be particularly sensitive to biaxial stresses compared to the A1(TO) and E1(TO) modes. Consequently, and in alignment with literature, the E2(high) mode was utilized as a marker for quantifying residual stresses within the structure [89]. This sensitivity may be reasonably due to the nature of the E2(high) mode, which is characterized by atomic oscillations that occur predominantly perpendicular to the c-axis of the wurtzite structure, and hence more sensitive to stress along the chosen axis (see **Figure 12**).

The inset of **Figure 18** illustrates the trend of the frequency of E2(high) mode in the HEMT-B sample (represented by the red line) and the HEMT-PD sample (depicted by the blue line) when moving along the vertical path indicated by the red line in **Figure 16**, i.e., crossing the AlGaIn/GaN heterostructure beginning from the packaging side and moving towards the silicon

substrate. The ω values of the E2(high) mode allow the calculation of residual stress point by point within the AlGaIn/GaN HEMT devices. Indeed, the frequency shift ($\Delta\omega$) linearly depends on the residual stress (σ) according to the relationship:

$$\langle\Delta\omega\rangle = K\langle\sigma\rangle \quad (20)$$

Where K is the stress coefficient, equal to $4.3 \text{ cm}^{-1}/\text{GPa}$ for GaN grown on c-direction silicon [90]. The frequency shift, $\Delta\omega$, is defined by the equation:

$$\Delta\omega = \omega - \omega_0 \quad (21)$$

Where ω is the peak frequency center, and ω_0 accounts for the corresponding stress-free E2(high) peak frequency center, fixed at 568 cm^{-1} [91].

It should be noted that, even if there was a slight influence on stress due to the ion milling treatment, this influence would be the same in both samples since the milling conditions were the same. Therefore, the calculated frequency shift $\Delta\omega$ was not affected by the preparation of the samples.

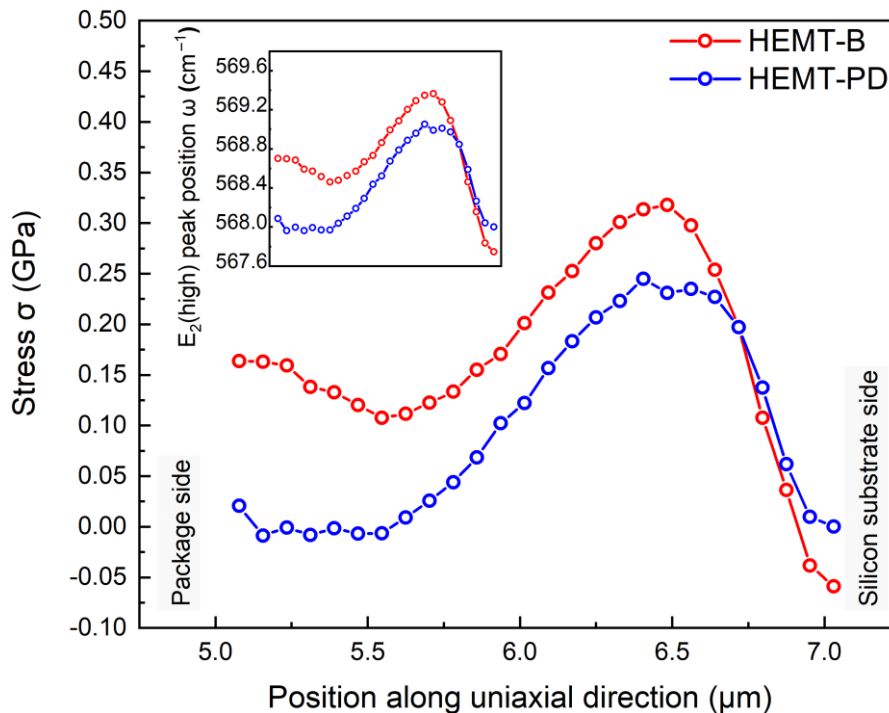


Figure 18. Stress distribution along the uniaxial direction, covering a range from $5 \mu\text{m}$ to $7 \mu\text{m}$ within the GaN layer, for both AlGaIn/GaN HEMT-B and AlGaIn/GaN HEMT-PD devices. The inset graph represents the E2(high) peak frequency center plotted against the position along the uniaxial direction in μm .

Figure 18 shows the residual stress (σ) in GPa, inferred from the frequency shift ($\Delta\omega$) of the E2(high) mode as a function of position along the analyzed path for both the HEMT-B (red line) and HEMT-PD (blue line) devices.

Due to the linear correlation between stress and frequency shift, the E2(high) mode frequency center follows a pattern mirroring that of the stress, as observed in the inset of **Figure 18**. A detailed analysis of the residual stress trend along the AlGaIn/GaN HEMT structure (**Figure 18**), reveals that the influence of package was mainly visible in the region between 5 μm and 6 μm , which is identified as the zone of interest. In contrast, from 6.55 μm to 7 μm , the lattice mismatch at the GaN/Si interface induced a more pronounced tensile stress compared to that generated by the packaging, as evidenced by the observed redshift (a shift towards lower frequencies) of the E2(high) mode. Furthermore, the non-monotonic behavior observed can be attributed to both the characteristics of the multilayer structure and/or the doping levels of the layers comprising the device. The behavior of E2(high) mode in HEMT-B device (represented by the red curve in **Figure 18**) showed a slight initial shift towards lower frequency values as it traverses the layers from 5 μm to approximately 5.5 μm , indicating the presence of tensile stress. This is followed by a clear shift towards the blue in E2(high), attributed to compressive stress likely induced by additional forces or applied loads. Subsequently, near the silicon substrate, a noticeable tensile stress is observed, characterized by a frequency shift towards lower frequencies, probably stemming from the lattice mismatch between GaN and silicon. The behavior of the E2(high) mode in the HEMT-PD device was entirely similar. However, the observed stress values are generally lower across the entire device (as indicated by the blue curve in **Figure 18**).

The influence of packaging was only evident within the specified area of interest, (from 5 μm to 6.55 μm) located near the surface of the device. Within this region, the packaged device (HEMT-PD) showed a decrease in stress levels of approximately 0.1 GPa compared to its bare counterpart (HEMT-B). This stress mitigation was attributed to the compression introduced by the packaging, which compensates for the intrinsic tensile stress present between the layers of the device. This result stems from a proper choice of material and packaging design, which must be optimized in terms of shape, dimensions, and thermal properties. Additionally, the incorporation of intermediate layers or buffer materials with more similar thermal properties

contributes to reducing stress at interfaces between different materials and ensures effective stress mitigation across the mold.

The mitigation of stress within the active layers of the AlGaN/GaN HEMT devices has a direct impact on its reliability and performance. Indeed, thermal-mechanical stresses and deformations are already well-known and extensively studied failure mechanisms. In general, lower stress leads to slower aging of the device. Furthermore, when current flows through a device, it undergoes thermal expansion proportional to the current itself due to the increase in temperature in the active region of the device [71]. Generally, this deformation is not uniform across the entire device but depends on the shape and arrangement of the semiconductor part through which the current flows. Particularly, in power switching applications, current values can be very high, resulting in intense heat release and consequent mechanical deformation. Since the crystal can withstand defined stress values beyond which it breaks, it is evident that the presence of residual stress when the device is in the off state can limit the maximum current that can flow through the device without destroying it. This aspect, along with more specifically thermal aspects, must be taken into account when defining the device's mission profile. Considering the above, residual stress mitigation is, among all other advantages, a potential way to improve the device performance and extending its lifetime [92-93]. Therefore, we can conclude that proper packaging design can effectively enhance the quality and overall reliability of the devices.

3.2.4. Conclusion

In this study, micro-Raman spectroscopy was employed as a powerful non-destructive technique to assess the stress and deformation induced by packaging in AlGaN/GaN HEMTs supplied by STMicroelectronics S.r.l. To evaluate the packaging's impact, we acquired 128 micro-Raman spectra by vertically scanning along the AlGaN/GaN heterostructure of the device. The data were analyzed using a fitting procedure employing a model consisting of three or four Lorentzians to accurately measure the frequency shift of the phonon modes' center. Particular attention was focused on the E2(high) phonon mode, which is highly sensitive to crystalline stress and therefore can be effectively used for its quantification. Two GaN devices supplied by STMicroelectronics S.r.l were studied, one packaged (HEMT-PD) and the other bare

(HEMT-B), to assess the influence of packaging on the residual stress present within the active layers of the device.

In the HEMT-PD device, a blue shift of the E2(high) mode near the packaging was observed, while a slight redshift followed by a blue shift was observed for the bare device. A linear correlation between the Raman frequency shift $\Delta\omega$ and stress σ was used to evaluate the compression stress induced by packaging. The packaged device showed a decrease in stress levels of about 0.1 GPa compared to the bare HEMT. In conclusion, the study states that the compression stress induced by the packaging process strongly mitigates the residual tensile stress present on wafer-level HEMT-B devices. Therefore, packaging, which provides mechanical support and protects the sensitive semiconductor wafer from external environmental factors, can play a dual role by also contributing to stress mitigation, compensating for the inherent tensile stress in these devices, and thereby improving performance in terms of reliability, dynamics, and lifetime.

The findings of this study show the importance of considering the impact of packaging on the distribution of stress in the devices during the stages of design and development.

Chapter 4

Assessing the reliability of a GaN HEMT through dynamic ON-resistance analysis - Thermal, Electrical, and Mechanical perspectives

This chapter focuses on the experimental investigation of the dynamic ON-resistance ($R_{DS(ON)}$) behavior of GaN HEMTs, a critical parameter that directly affects the performance and reliability of power devices. It begins with an overview of the causes of dynamic ON-resistance, before delving into the experimental investigation. Through detailed thermal, electrical, and mechanical characterizations, the study examines the impact of thermal and thermomechanical phenomena on the dynamic ON-resistance ($dR_{DS(ON)}$) of GaN HEMTs under power cycling conditions. It outlines the techniques employed to measure the induced heating and displacement effects. The findings aim to provide valuable insights into GaN HEMTs reliability.

4.1. Introduction

GaN HEMTs benefit from the formation of a 2DEG channel which facilitates efficient electron conduction between the source and drain. This characteristic results in a significantly low drain-source ON-resistance, denoted as $R_{DS}(ON)$ [94-97]. However, despite continuous advancements in GaN technology, certain challenges persist. A key reliability concern is the progressive increase in ON-resistance during device operation, deviating from its nominal DC value. This phenomenon, known as dynamic ON-resistance ($dR_{DS}(ON)$) or current collapse, leads to a decrease in drain current [98-99].

4.2. Causes of dynamic ON-resistance

Dynamic ON resistance is a phenomenon resulting primarily from charge-trapping mechanisms, as undesired accumulation of electrons in specific regions of the device structure. For GaN HEMTs, these regions may include the passivation layer, the surface, the AlGaN barrier layer, or the GaN buffer layer. The negative trapped charges affect the distribution of electrons within the channel. They deplete the free electrons and trigger recombination in the 2DEG electron concentration to ensure charge neutrality. This process reduces the drain-source current, and induces an increase in $R_{DS}(ON)$ above its intrinsic value [99].

Trapping mechanisms are divided into surface and deep mechanisms. Surface trapping arises from charge accumulation at the gate terminal near the drain edge when the device is in the OFF state. The hot electrons crossing the barrier layer are captured by surface traps, they act as a virtual gate when the device is turned ON, restricting the channel and inducing the dynamic ON-resistance phenomenon. However, deep trapping occurs as a result of doping in the buffer layer, which introduces deep traps capable of capturing hot electrons. This phenomenon arises when the device is in the ON state, leading to trapped charges that weaken the 2DEG channel [97].

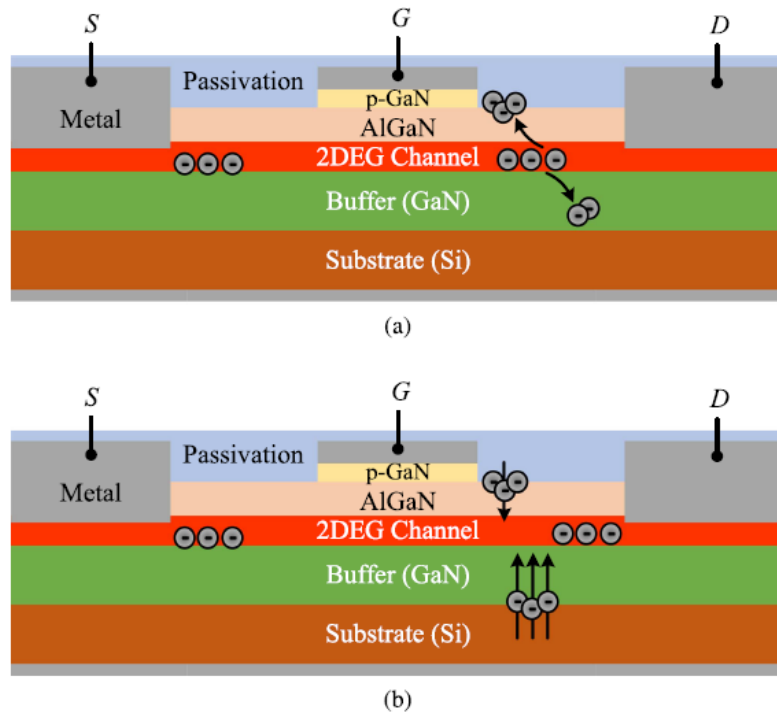


Figure 19. A Cross-sectional view of a simplified GaN-on-Si structure, illustrating charge trapping mechanisms: (a) trapping of hot electrons in dielectric layer along the surface and buffer layer, and (b) OFF-state traps caused by charges ionization of surface and buffer [99].

Charge trapping mechanisms are further influenced by a variety of factors, with the device's operational conditions playing a significant role in increasing the dynamic ON resistance. The key operational parameters for a transistor include: Blocking voltage (V_d), device current (I_d), switching frequency (f_s), switching period (T_s), duty cycle (D), gate voltage (V_g), slew rates (dV_d/dt and dI_d/dt), and switching condition (hard - soft) [99]. In addition to operational factors, environmental parameters also significantly impact trapping mechanisms, including the thermal effects (Junction temperature (T_j)), and radiation effects. Extensive studies have been conducted to assess the effects of these factors on charge trapping characteristics and their contribution to the dynamic ON resistance ($R_{DS(ON)}$). A brief summary of these effects is presented below.

Drain current

$dR_{DS(ON)}$ exhibits a monotonic rise behavior with high drain current levels, which become more pronounced at higher temperatures (e.g., 150 °C), measured at different time intervals of 500 ns and 2.5 μ s [100].

Drain voltage

The dynamic ON resistance increases monotonically with increased voltage stress during hard-switching states, more significantly in a case of 1 MHz compared to 250 and 500 KHz [101].

Temperature

The dynamic ON resistance steadily increases with voltage during hard-switching states until a temperature of approximately 50 °C, after which it shows a non-linear decrease attributed to reduced hot-electron trapping at higher temperatures [102].

Switching frequencies

$dR_{DS}(ON)$ degrades during repetitive hard-switching cycles due to high drain-source voltage stress which induces a reduction in drain current during OFF conditions [103]. Additionally, $dR_{DS}(ON)$ exhibits a monotonic increase with high switching frequencies in the multi-megahertz range, reaching nearly 2 MHz before stabilizing due to reduced trapping and de-trapping durations [104].

Duty ratio

$dR_{DS}(ON)$ decreases with increased duty ratio, due to the shortened period for trapping mechanism during large ON state time, which induces an increased de-trapping process [105].

Additional factors influencing the $dR_{DS}ON$ should be considered:

Gate resistance

Gate resistance impacts the switching period and associated losses, influencing charge trapping duration and energy, thereby affecting $dR_{DS}(ON)$ [106].

Operational mode

$dR_{DS}ON$ varies based on the operational mode of power converters, including the input-output parameters and conditions.

4.3. Assessment of GaN HEMT reliability through dynamic ON-resistance analysis

This study aims to understand the impact of thermal and thermomechanical phenomena on the dynamic ON-resistance ($dR_{DS}ON$) of GaN HEMTs during operation. Specifically, we

investigate the relationship between the induced heating, displacement effects, and their influence on $dR_{DS(ON)}$ under power cycling conditions.

The flow of current within a device generates heat, leading to thermal expansion (device swelling), which acts as a source of internal mechanical stress. This effect occurs whenever the device is in the ON state, and has a significant impact on its overall efficiency, particularly on the dynamic ON-resistance, that can impair their performance. Therefore, these parameters must be carefully considered and accurately quantified. To map and measure the temperature rise induced within the device following current pulses, a high-speed infrared camera was employed. The heat generated consequently induces an internal deformation within the device structure through an out-of-plane displacement of its layers. Quantifying this effect is essential for assessing the device's operational state and reliability. To achieve this, a scanning vibrometer technique was used to measure deformation. The characterization of the device was conducted under short-circuit conditions. Studying device behavior in these conditions provides valuable insights into its robustness and capability to withstand extreme operating scenarios, reflecting its practical performance in real-world applications.

4.3.1. Terminal short-circuit configuration

The experimental setup included a GaN HEMT connected in a terminal short-circuit configuration, as illustrated in **Figure 20**. The configuration includes the following components:

GaN HEMT

WBG semiconductor device serves as the switching element in the circuit.

Programmable signal generator

The “National instrument PCIe 6351” multifunction board is used to send the enabling signal to the driver.

Driver

Amplifies and delivers the necessary voltage and current signals to the gate, enabling the GaN transistor to switch ON and OFF.

Low-capacitance Capacitor (1.1 μ F)

Connected between the drain and source, it manages transient voltages and switching behavior.

High-capacitance Capacitor (150 mF)

Supplies the high drain-source current (I_{DS}) required for the circuit's operation.

Power supply

A DC power supply delivers power to the circuit.

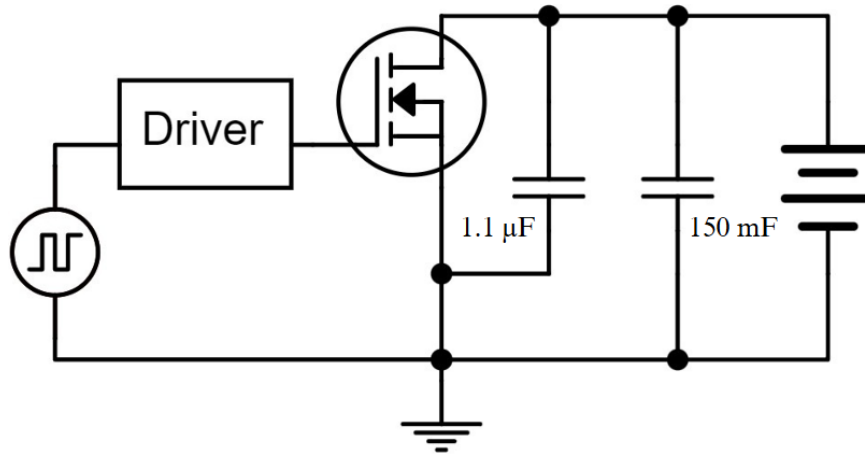


Figure 20. Terminal short circuit configuration.

The input signal is supplied to the driver block, which modulates it to generate the voltage levels required to control the GaN transistor gate. The driver's output is connected to the gate terminal of the HEMT, defining its ON and OFF states. The drain terminal of the HEMT is wired to the positive terminal of the power supply, while the source terminal is grounded, creating the return for current from the power supply. The two capacitors are connected in parallel between the drain and source terminals to manage transient voltages.

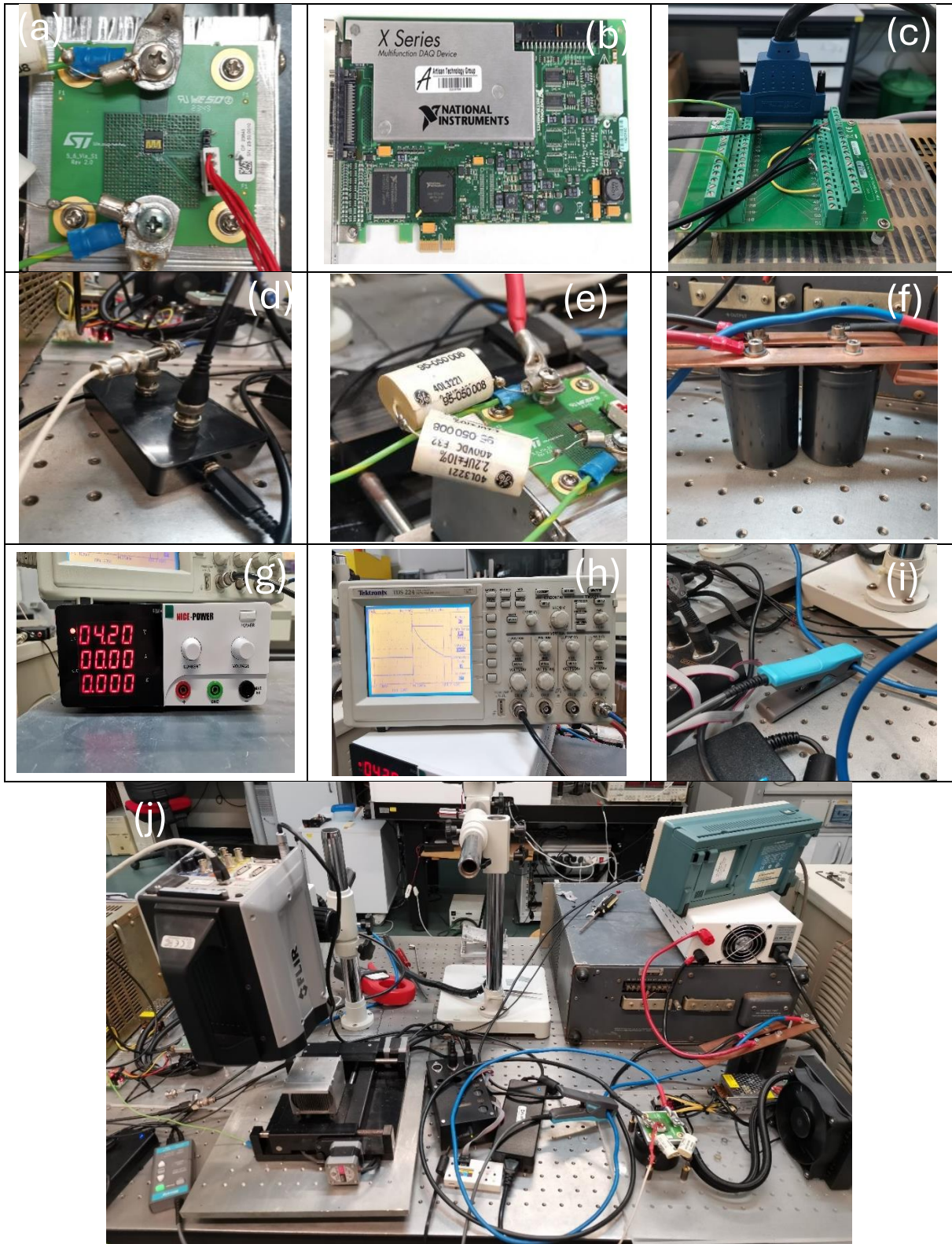


Figure 21. Images of the components used in the terminal short-circuit configuration: (a) DUT soldered onto the PCB, (b)(c) National instrument PCIe 6351 multifunction board and connector block, (d) Driver, (e)(f) Capacitors (low and high capacitance), (g) DC power supply, (h) Oscilloscope, (i) Current probe, and (j) Complete experimental setup.

4.3.2. Device Under Test

The Device Under Test (DUT) is a decapsulated enhancement-mode GaN HEMT soldered onto a board to facilitate precise characterization and analysis, as depicted in **Figure 23**.

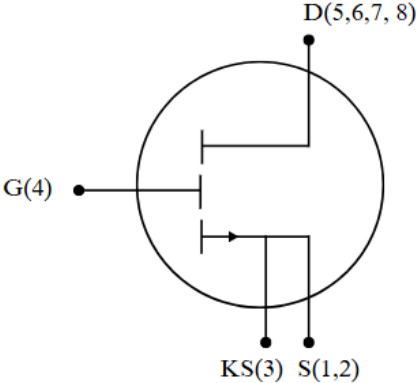


Figure 22.Design schematic of GaN HEMT.

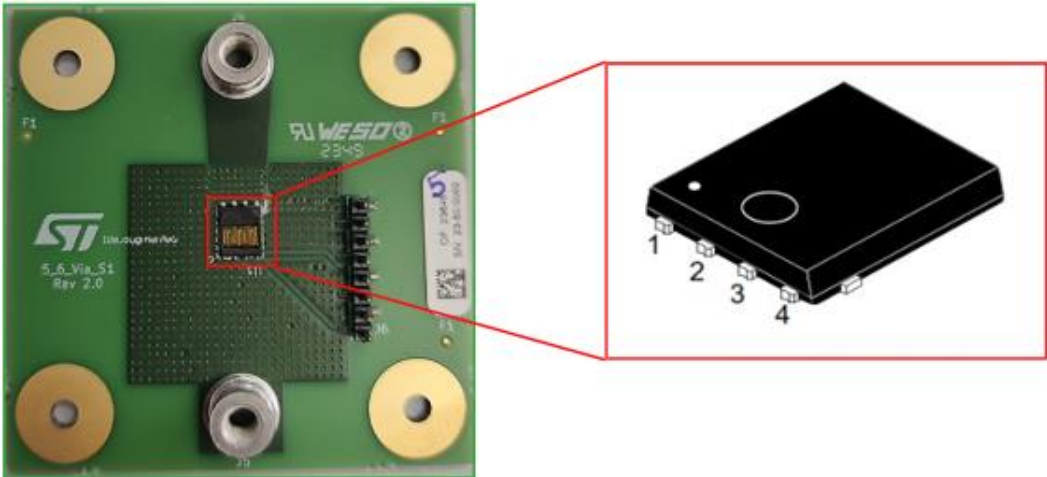


Figure 23. Decapsulated normally OFF GaN HEMT soldered on a board.

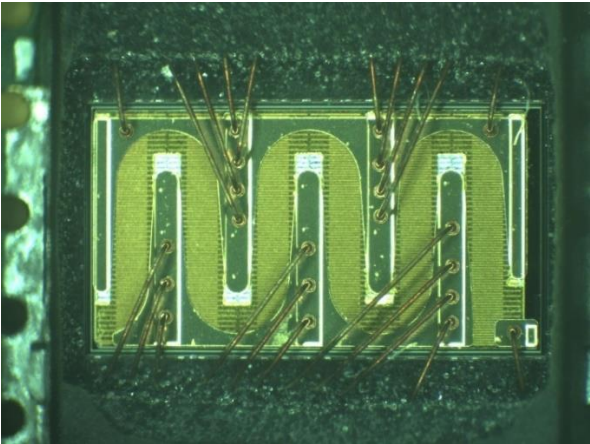


Figure 24. Optical images of GaN HEMT.

The device was configured in the terminal short circuit setup, with the driver applying a gate-source voltage (V_{GS}) of 7 V to open the gate, allowing the current (I_{DS}) to flow between the drain and source through the transistor channel (**Figure 20**). We can tune the current through a DC generator, while monitoring the current signal with a current probe wired to an oscilloscope. The programmable signal generator controls both the frequency of the DUT switch-on and the duty cycle. The specifications of the device under test are detailed in **Table 3**.

Table 3. Specifications of GaN-HEMT.

Characteristic	Value
Typical V_{ds}	650 V
Typical I_{ds}	25 A
Maximum Static R_{DSON}	65 m Ω
Typical switching frequency	1 MHz
Dissipated power at 25 °C	305 W
Maximum operational temperature	150 °C

4.3.3. Device characterization

During device characterization, the drain source current (I_{DS}) represents the discharge current of a set of capacitors, therefore its value depends on the amount of stored charge, thus, on the DC voltage applied across the capacitors’ plates. We applied pulse with an ON time (t_{ON}) of 10 ms and an OFF time (t_{OFF}) of 1990 ms, resulting in a switching frequency of 0.5 Hz. A low t_{ON}/t_{OFF} ratio (~0.5%) was chosen, with peak currents of 60 A. A so small pulse-to-pause ratio needs to give the device enough time to recover from the stress after the current pulse and go back to the ambient temperature by dissipating the generated heat.

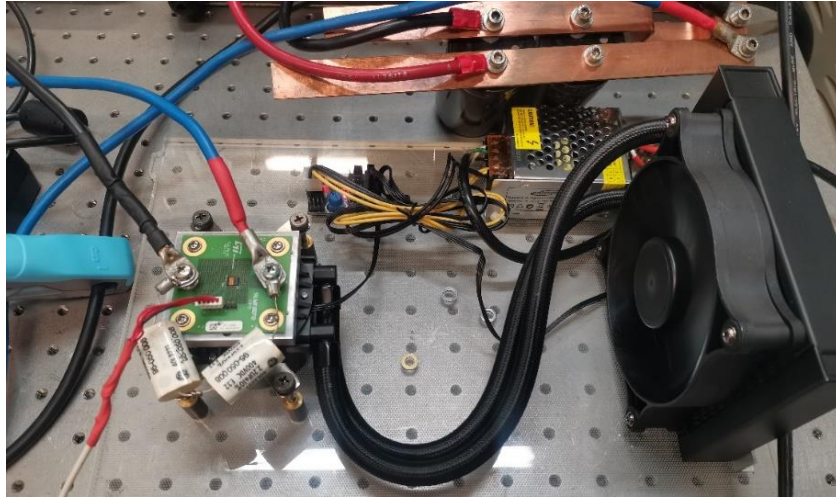


Figure 25. Experimental setup for measuring ON-Resistance in GaN HEMT.

4.3.3.1. Electrical characterization

A significant challenge in evaluating the dynamic ON resistance $R_{DS(ON)}$ is the development of an adapted methodology capable of accurately characterizing the device and extracting its dynamic ON-resistance. The dynamic ON resistance is determined through indirect calculations, based on the measurement of the current and voltage through Ohm's law. Our measurement setup is designed to simultaneously capture both voltage and current values.

The same multifunction board previously used as a signal generator was employed during the turning ON pulses to collect the V_{DS} and I_{DS} data. The I_{DS} measurements were acquired using a current probe, with the data sampled at a frequency of 100 k samples/s. The variation of V_{DS} (**Figure 26**) and I_{DS} (**Figure 27**) over the duration of the pulse is presented in the following graphs. Data acquisition was triggered 8 milliseconds before the pulse application, for this reason, all the graphs and data show values starting at just under 8 ms and ending at just under 20 ms.

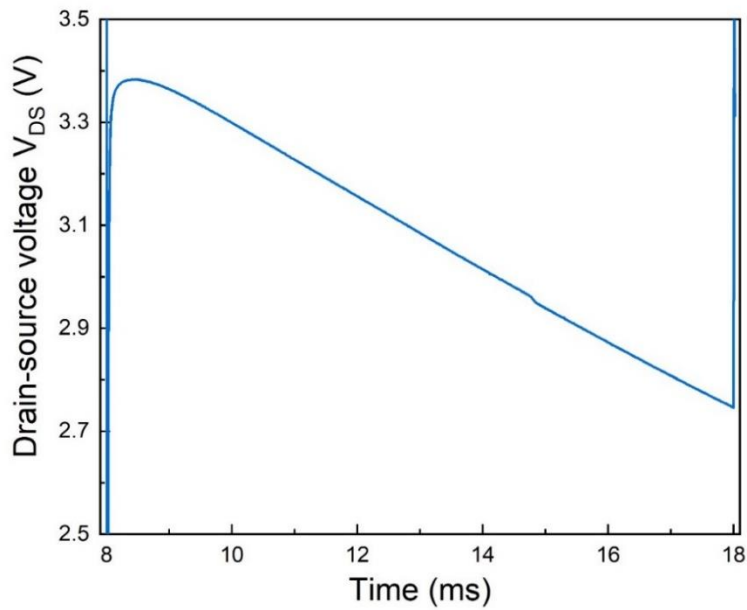


Figure 26. Evolution of V_{DS} during the ON phase of a single pulse.

The graph in **Figure 26** shows the evolution of the drain-source voltage (V_{DS}) over time during a single pulse. At the beginning of the measurement, the voltage increases sharply, reaching a peak value slightly above 3.3 V. This sharp increase corresponds to the moment the pulse is applied to the gate, turning the device ON. After the peak, V_{DS} starts to decrease gradually, reflecting the discharge of the capacitors in the circuit through the transistor channel. This decrease continues over the duration of the pulse, until the end of the ON phase (10 ms), when the gate signal is removed.

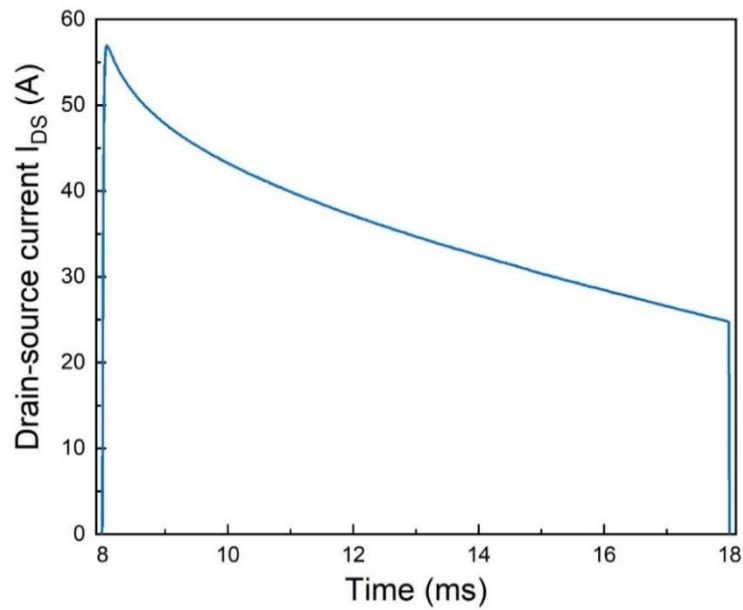


Figure 27. Evolution of I_{DS} during the ON phase of a single pulse.

Regarding Drain-source current (**Figure 27**), the same behavior is observed. When applying the pulse, the I_{DS} increases suddenly to a high value, then, with the discharge of capacitors, it starts to decrease slowly. This graph illustrates the evolution of the drain-source current (I_{DS}) during the application of a single pulse. At the beginning of the pulse, I_{DS} shows an abrupt sharp increase to its peak value of approximately 60 A. This current rise corresponds to the gate pulse, which opens the transistor channel and allows the current to flow driven by the stored charge in the capacitors. After that, I_{DS} starts to decrease, initially in an abrupt way then slows down over time, reflecting the capacitors discharge. At the end of the pulse duration, off state, I_{DS} drops sharply to zero as the channel closes and the current ceases to flow.

The graph in **Figure 28** illustrates the evolution of the drain-source ON resistance ($R_{DS(ON)}$) during a single pulse, calculated using Ohm's law

$$R_{DS} = \frac{V_{DS}}{I_{DS}} \quad (22)$$

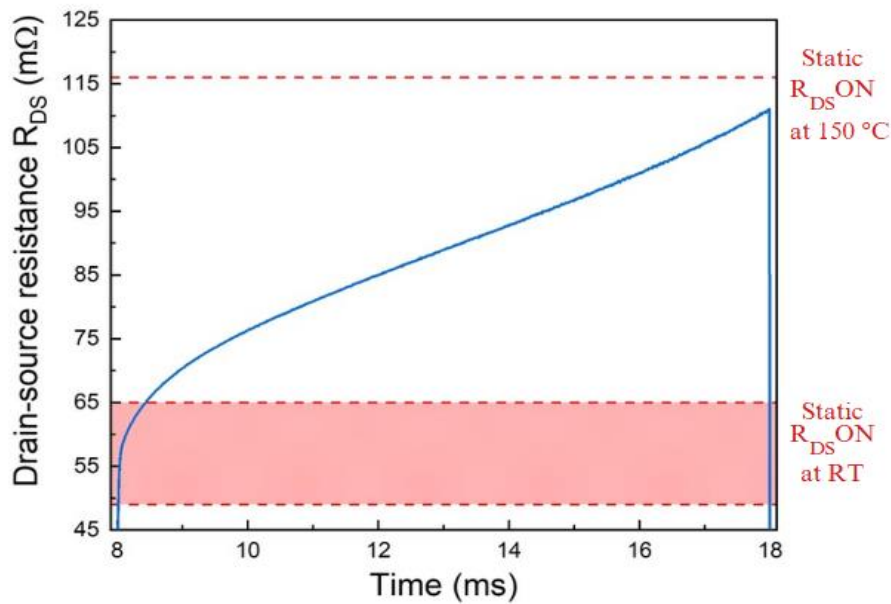


Figure 28. Evolution of $R_{DS(ON)}$ during the ON phase of a single pulse.

$R_{DS(ON)}$ shows initially a rapid increase with the start of the pulse due to the sudden application of a high current (I_{DS}). After the initial rise, $R_{DS(ON)}$ continues to grow gradually throughout the ON phase of the pulse until ultimately reaching a value close to the static $R_{DS(ON)}$ specified in the datasheet for an operating temperature of 150°C.

The dashed red lines mark the static $R_{DS(ON)}$ values at room temperature (RT) (red zone), and at 150°C. Where the $R_{DS(ON)}$ first starts below the static value at RT then eventually approaches the one at high temperature.

The general increase in $R_{DS(ON)}$ during the pulse is indicative of its dynamic behavior under pulsed conditions. This growth is attributed to the effect of hot electron trapping mechanism combined with the thermal effect from the device heating during the pulse. Which provides insights into the thermal and electrical effects on the device performance under switching conditions.

4.3.3.2. Thermal analysis

During the electrical operation of a device, its average temperature increases due to power dissipation, potentially leading to thermomechanical stress. Consequently, it is important to perform a comprehensive thermal characterization to assess and quantify this thermal stress, which can impact the device's reliability.

The thermal analysis of electronic devices is commonly assessed using infrared radiation thermography which provides non-contact temperature measurements.

Introduction to Infrared radiation thermography

All objects with temperatures higher than absolute zero (-273,15 °C) emit electromagnetic radiation due to thermal energy. The spectral power density of the emitted radiation is primarily dependent on the object temperature, as described by Planck's law of black body radiation. As the temperature increases, the peak spectral power density shifts toward shorter wavelengths, following Wien's displacement law, which states an inverse relationship between the peak wavelength and temperature [107].

Planck's law:

$$L_{\lambda,T}^0 = \frac{2\pi hc^2}{\lambda^5 [\exp(hc/\lambda kT) - 1]} \text{ (W/m}^2 \cdot \text{m/sr)} \quad (23)$$

Where:

L : Radiance

h : Planck's constant = 6.6×10^{-34} J.s

T : Temperature in Kelvin (K)

c : Speed of light in vacuum = 3×10^8 m/s

k : Boltzmann constant = 1.4×10^{-23} J/K

λ : Wavelength in meter (m)

Wien's displacement law:

$$\lambda_{max} = \frac{2897.8}{T} \text{ (}\mu\text{m)} \quad (24)$$

With λ_{max} the peak wavelength (in μm), and T is the temperature in Kelvin.

Figure 29 provides the spectral radiant emittance of the black body, with the dashed line demonstrating Wien's displacement law.

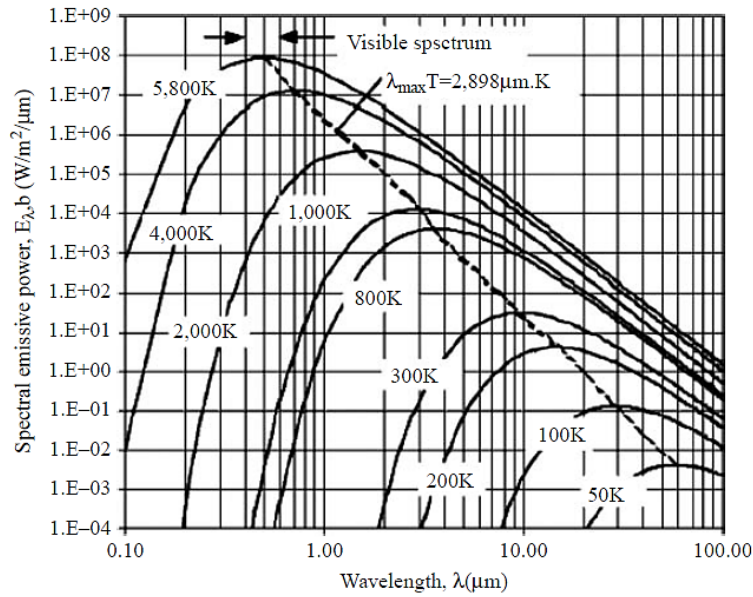


Figure 29. Spectral radiant emittance of a black body.

The total emitted radiation W , obtained integrating the Planck's law across the complete spectral range and over the solid angle, is proportional to the object's temperature, through Stefan-Boltzmann law:

$$W = \sigma T^4 \quad (25)$$

Where:

$$\sigma : \text{Stefan-Boltzmann constant} = 5.7 \times 10^{-8} \text{ K}^{-4}\text{W/m}^2$$

While black bodies are ideally emitting all incident radiation, real objects, known as gray bodies, deviate from this perfect behavior by reflecting portions of the incident radiation, thus not emitting all the incident radiation. In fact, the actual quantity of emitted radiation is dependent on a parameter called emissivity (ϵ), which varies with the object's material properties, surface geometry, wavelength, and temperature:

$$W = \epsilon \sigma T^4 \quad (26)$$

Where:

$$\epsilon : \text{Emissivity, ranging between 0 and 1}$$

Hence, accurate determination of the real temperature of the objects requires measurements of the total radiant emittance and the emissivity.

For measuring an object's surface temperature, it is often blackened or calibrated. The calibration involves scanning the surface at multiple known temperatures to generate its emissivity map. This calibration may be repeated at various temperatures to account for the emissivity variation with temperature.

The emissivity is generally supposed to remain constant across a specific temperature range, enabling the creation of an apparent map of temperature. Then, the accurate map of temperature is generated by aligning the map of the apparent temperature and the map of the emissivity. This approach enables accurate thermal characterization.

Thermal analysis of GaN HEMT

The thermal characterization of GaN HEMT under test was performed using a high-speed, highly sensitive mid-wavelength infrared (MWIR) camera (FLIR mod. X6901 thermal camera) presented in **Figure 30**. This camera is capable of capturing the total emitted infrared radiation (W) within the spectral range of $3\mu\text{m}$ to $5\mu\text{m}$.

For this study, the temperature range of interest was sufficiently narrow to assume that the emissivity of the device surface remained effectively constant across the whole measurement range.



Figure 30. High speed MWIR camera.

The thermal analysis involved configuring the device in the same terminal short-circuit setup shown in **Figure 21(j)**. The device was subjected to a 10 ms ON pulse, with a gate-source voltage of 7 V and a peak drain-source current of 60 A.

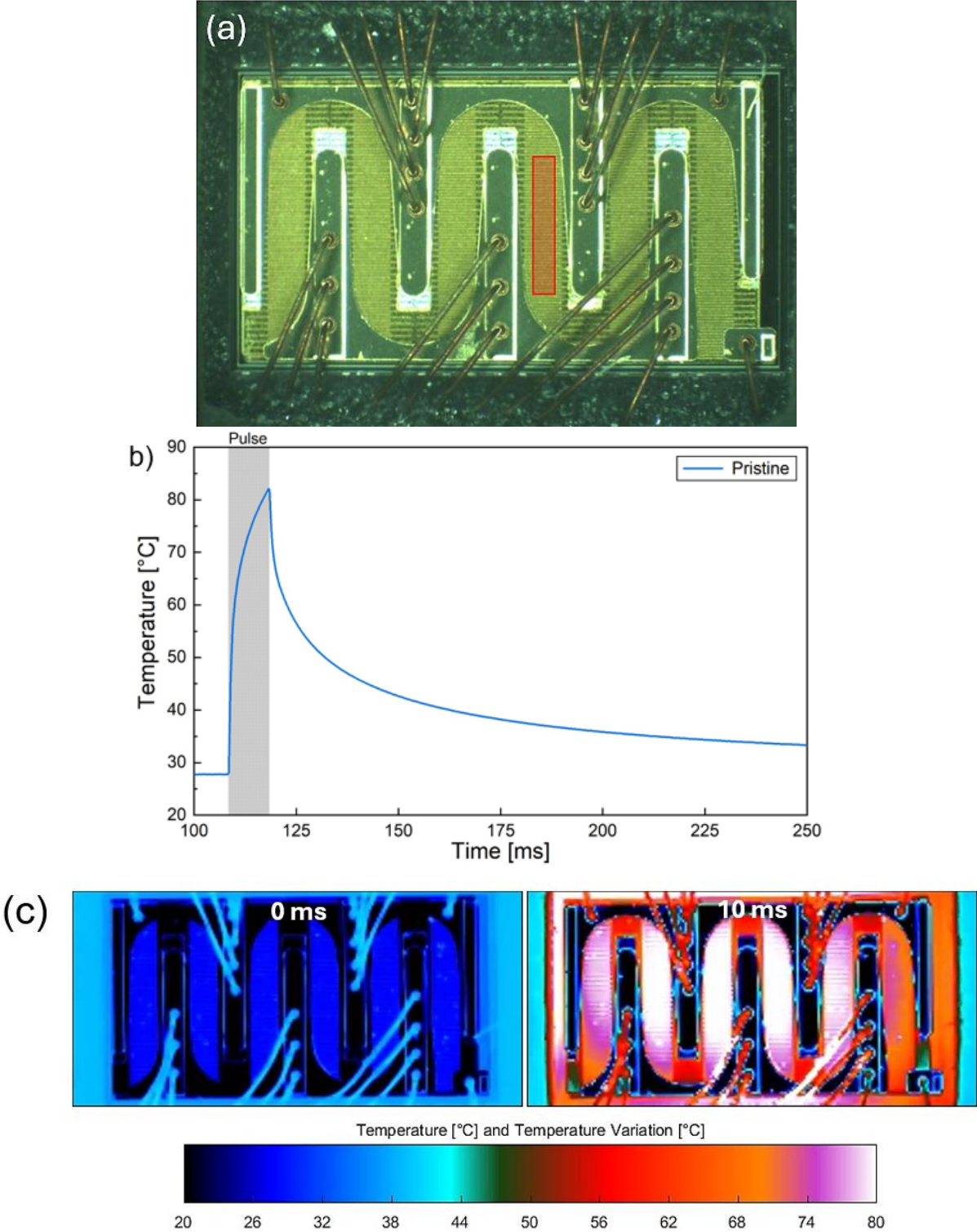


Figure 31.(a) Picture of the device under test, where the scanned zone for temperature measurement is highlighted. (b) Evolution of mean temperature within the defined zone during and after the ON state. (c) Thermal mapping of the entire device, depicting the temperature distribution over the surface when cold and when it reaches its peak temperature, i. e. at the end of the pulse.

The thermal measurements were conducted on a defined area of the device surface marked in **Figure 31(a)**. The temperature evolution within this area during the ON pulse was showed in **Figure 31(b)**. Additionally, a thermal map of the entire device surface was generated, describing the spatial distribution of temperature during the ON pulse (**Figure 31(c)**).

Figure 31(b) illustrates the mean temperature evolution within the defined area of the GaN HEMT during and after the application of a single ON pulse. The graph reveals a sharp increase in device temperature during the pulse, reaching a peak of approximately 80°C at the end of the 10 ms pulse duration. After the pulse, the temperature gradually decreases as the device cools down. To let the device cool down before the next pulse a low duty cycle with a t_{ON}/t_{OFF} ratio of 10 ms/2 s ($\sim 0.5\%$) was selected.

The accompanying thermal map further highlights the spatial distribution of heating across the device surface during the ON pulse. The temperature increase is not uniformly distributed, with the central region of the device exhibiting significantly higher temperatures compared to the extremities. The map demonstrates that the device temperature rises from 20°C to approximately 80°C within 10 ms.

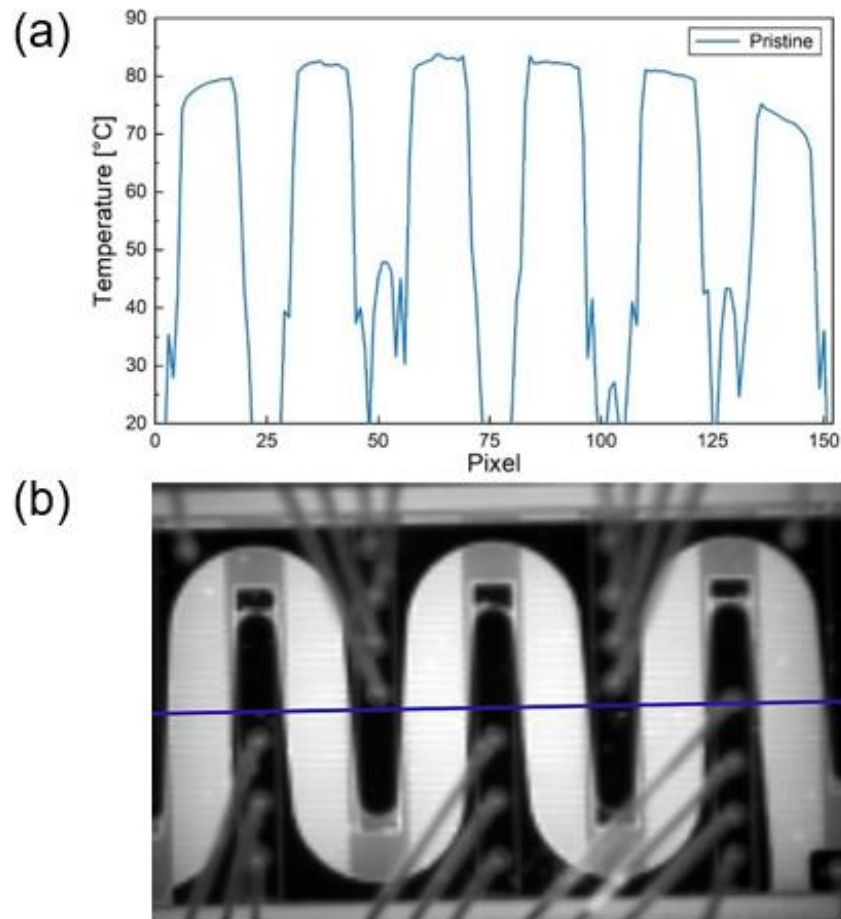


Figure 32. Temperature distribution along horizontal line central to the device structure.

The graph in **Figure 32(a)** illustrates the temperature variation along a horizontal line traversing the device (**Figure 31(b)**). The line, positioned centrally across the device, extends from one extremity to the other.

The interpretation of this graph requires clarification. A cyclical trend with significant temperature variations can be observed. Specifically, it appears that the temperature of the metallizations is much lower than that of the other regions. However, as previously explained, a calibration was performed that accounts for the emissivity of the material only in the area between the metallizations. For this reason, the metallizations, which are characterized by very low emissivity values, appear cold. Moreover, the graph reveals that the external parts of the device have lower temperatures compared to the central ones. This observation obviously aligns with the non-uniform thermal distribution previously observed in the thermal maps and underscores the importance of identifying hottest areas for improved thermal management and overall reliability.

4.3.3.3. Displacement analysis

To further investigate the effects of heat generation within the device structure during electrical operation, an analysis was conducted to measure the out-of-plane displacement of the device under test. This approach aimed at assessing the thermomechanical strain occurring during operation.

To capture and quantify rapid out-of-plane displacements at specific points on the device surface, a Laser-Doppler Vibrometer technique was employed using the Polytec MSA-500 Micro System Analyzer, as depicted in **Figure 33**. This advanced system enables high-precision measurements of surface deformation.



Figure 33. Polytec MSA-500 micro system Analyzer.

Introduction to Laser-Doppler Vibrometer

Laser-Doppler Vibrometer (LDV) is a technique for measuring vibrations without contact, suitable for applications where direct interaction with the object is impractical. This includes lightweight objects, sensitive surfaces, or heat generating devices. Depending on the focusing optics, LDV is capable of operating over distances varying from millimeters to kilometers [108-109]. The technique operates by analyzing the frequency shift (Doppler shifts) of laser light back scattered from the surface in movement. The laser beam is split into two components,

the measurement beam is focused on the surface in movement, which reflects it back toward a detector. The reference beam remains within the interferometer. The measurement beam is recombined with the reference beam at the detector. And the resulting interference of these two beams gives information about the displacement and the velocity of the surface at specific position. The measurements are conducted along the axis of the laser beam, enabling precise out-of-plane displacement analysis. In particular, the displacement is linked to the phase of the Doppler signal, while the velocity is linked to the frequency shift of the Doppler signal. To accurately measure the displacement's magnitude and velocity of an object during motion, LDV utilizes a heterodyne interferometer equipped with Bragg-cell. This approach involves introducing a controlled frequency shift to one of the laser beams, specifically the reference beam in our instrument. The frequency-shifted reference beam then interferes with the measurement beam at the detector to produce an interference signal. The resulting interference pattern provides two critical information: the frequency difference is related to the surface's displacement velocity, and the phase difference is proportional to the displacement magnitude. This approach is advantageous as it allows the reduction of technical noise in the detector, as well as suppression of the harmonic distortions in the detector signal. A simplified scheme of the heterodyne interferometer included into the Polytec MSA-500 is illustrated in **Figure 34**.

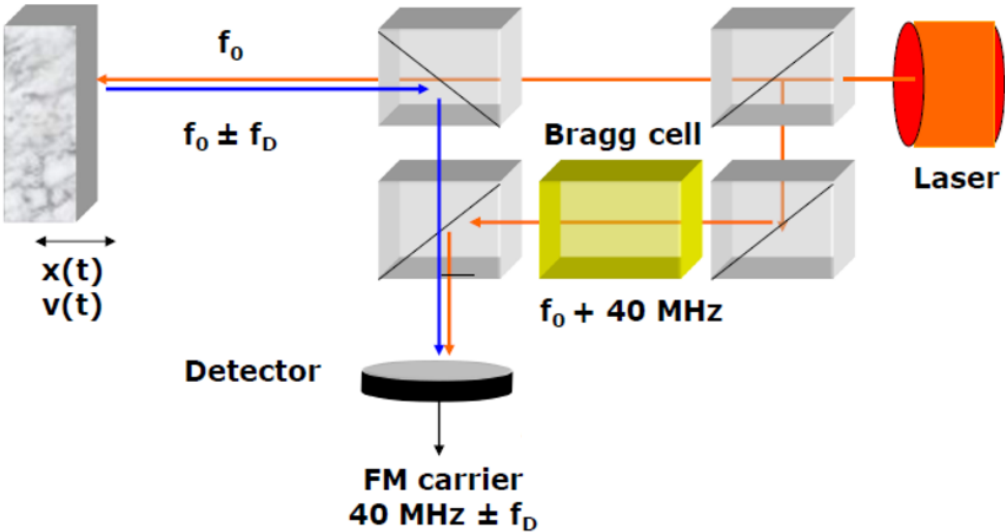


Figure 34. configuration of a Heterodyne interferometer.

Measurements of out-of-plan displacement of GaN HEMT

The measurement of surface displacement occurred with the device connected to the same terminal short-circuit configuration used in previous experiments. The device was operated for 10 ms with a gate-source voltage of 7 V and peak drain-source current of 60 A.

Synchronization of the current pulses with the acquisition system, initiated 8 ms prior to pulse application, allowed for the precise recording of time-resolved surface displacements at predefined points on the DUT as illustrated in **Figure 35**, the scanning mesh utilized during the measurements highlights the specific points on the DUT surface where data were acquired. Each vertex of the triangular mesh represents an individual scanning point, providing insights into the mechanical response of the device under electrical stress. Once the mesh has been defined a galvanometric driven mirror moves the laser beam point by point along the sample surface. The system is synchronized with the current pulses; hence, it will automatically acquire the deformation data, providing a deformation curve at each point of the mesh.

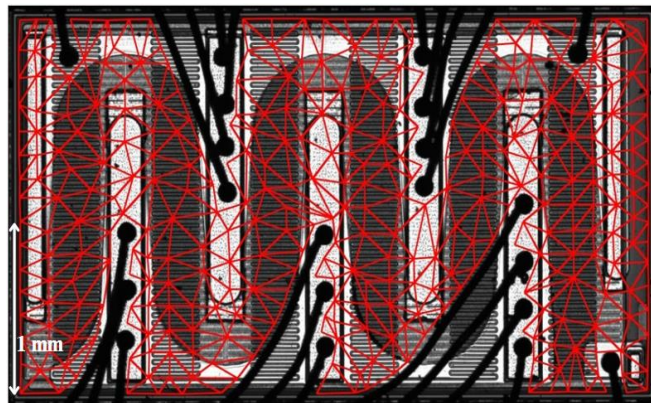


Figure 35. Optical image of the DUT with scanning mesh where each of the triangles' vertices is a scanning point.

The graph in **Figure 36(b)** demonstrates the variation of out-of-plane displacement at a specific position on the device surface indicated in **Figure 36(a)**. The displacement reaches a peak value of approximately 5 μm slightly after 18 ms, i.e. the end of the 10 ms pulse represented by the grey area. This rapid deformation mirrors the thermal response of the device, indicating a strong correlation between heat generation and mechanical strain. The exact position of the maximum is 18.8 ms since the device needs time to expand. Following the pulse, the displacement gradually decreases, reflecting the device's relaxation as the thermomechanical strain dissipates over time. The small $t_{\text{ON}}/t_{\text{OFF}}$ ratio ($\sim 0.5\%$) was deliberately chosen to ensure sufficient relaxation of the strain before the next pulse and to allow efficient heat dissipation.

The surface displacement is presented in **Figure 36(c)**. These maps provide a comprehensive view of how the deformation varies across the DUT surface. The displacement is not uniform, with certain regions exhibiting higher deformation, indicative of heterogeneous distribution of thermomechanical effect, highlighting the areas of the device that are more susceptible to strain during operation.

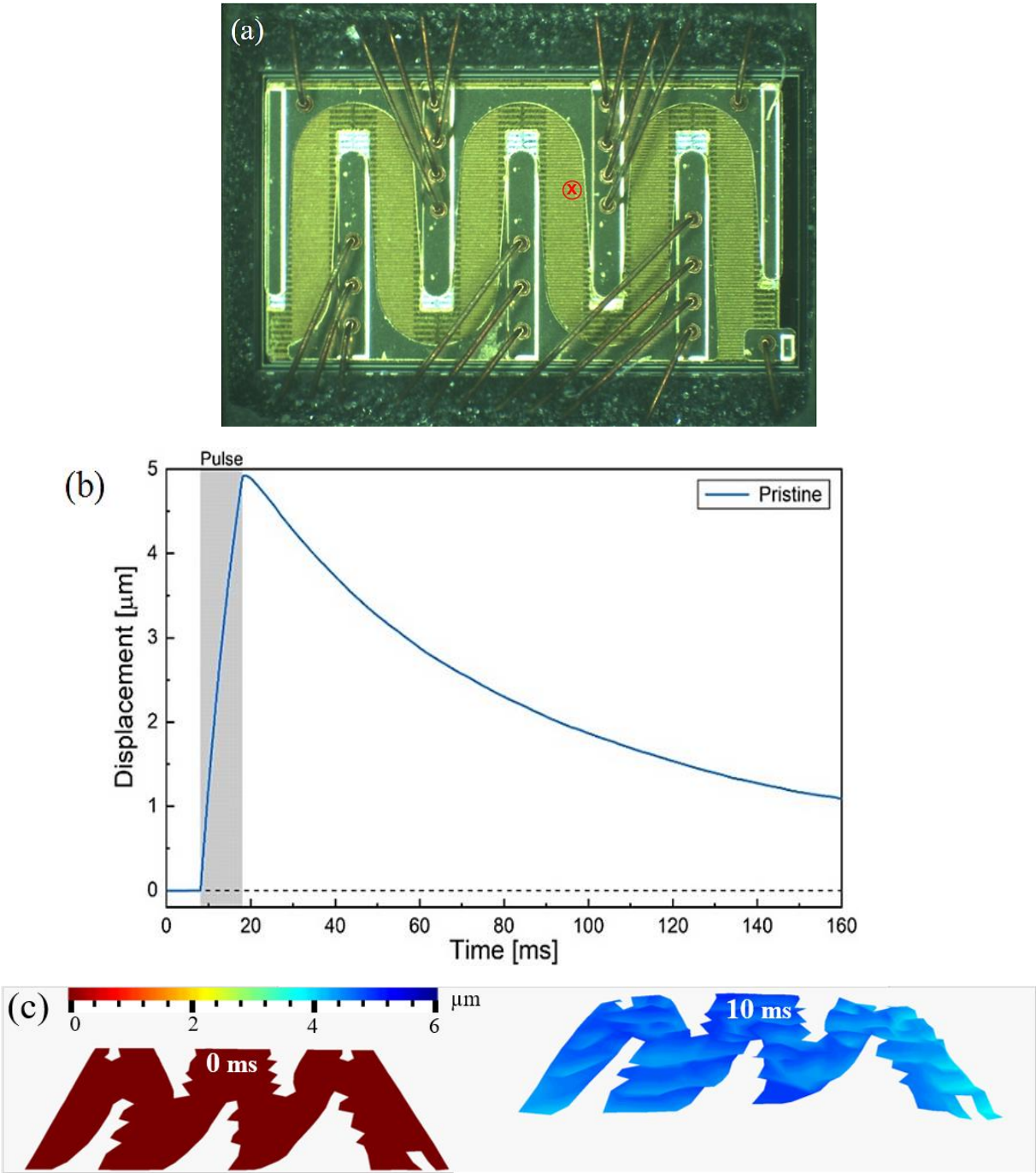


Figure 36.(a) Picture of the device under test. (b) Evolution with time of the displacement measured at the scanning point marked in (a) during the ON and OFF states of a pulse. (c) Scanning map of device deformation, illustrating the out-of-plane displacement, reaching a maximum of 5 μm at the end of the pulse (the frames are extracted from the whole DUT displacement video clip).

4.3.4. Device Aging – Power cycling

In this section we investigate the degradation behavior of the E-mode GaN HEMT during aging test, focusing on its electrical, thermal, and thermomechanical performance after successive power cycling sessions. As switching devices exhibit specific characteristic parameters, it is crucial to define and monitor a relevant aging indicator for assessing the device’s reliability and lifetime [97].

For the studied E-mode GaN HEMT, dynamic ON-resistance ($dR_{DS(ON)}$) was chosen as the primary aging indicator, as it is directly related to thermal and thermomechanical effects.

Power cycling test procedure

The GaN HEMT was subjected to power cycling for nearly one billion switching events (828 million cycles). The test was conducted across 22 sessions, with varying duration. Initial 16 sessions lasted 30 minutes each with continues stress application, during which no significant variations were observed. For the subsequent 6 sessions the stress duration was increased to 150 minutes per session, resulting in an overall stress period of 23 hours. The graph in **Figure 37** represents the progression of the power cycling test over the entire stress period of 23 hours. With sessions representing different total number of stress pulses, corresponding to a specific stress duration.

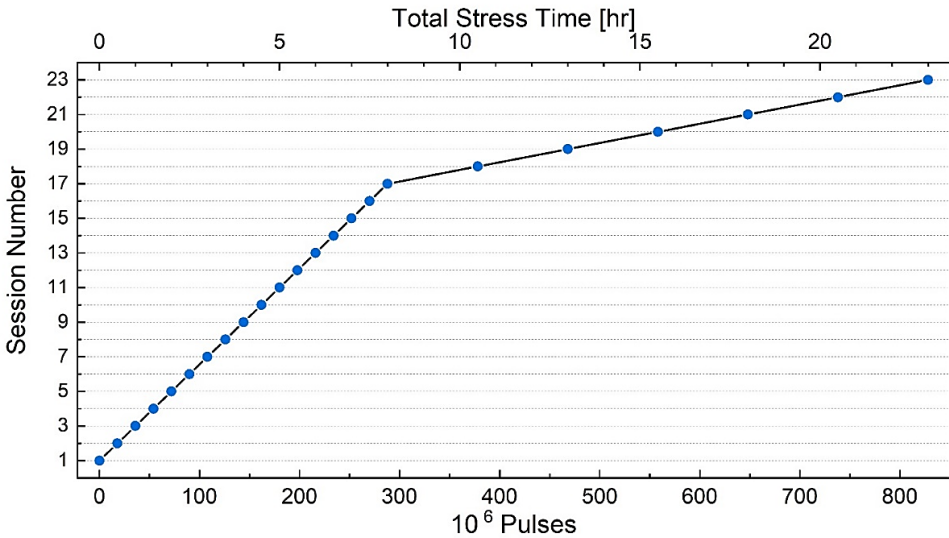


Figure 37. Power cycling test profile: 23-hour stressing period with 22 cycles of varying durations. The figure shows 23 points corresponding to the characterization sessions where the first point represents the measure on the pristine device.

V_{DS} , I_{DS} and $dR_{DS(ON)}$, were experimentally measured to assess their evolution with aging and the resultant effects on device performance.

Experimental Setup

The same experimental setup used for pristine characterization was employed to monitor V_{DS} , I_{DS} and $dR_{DS(ON)}$ after each stress session. The following power cycling conditions were maintained throughout the test:

- Peak drain-source current: 20 A
- Switching frequency: 10 kHz
- Duty cycle: 50 %

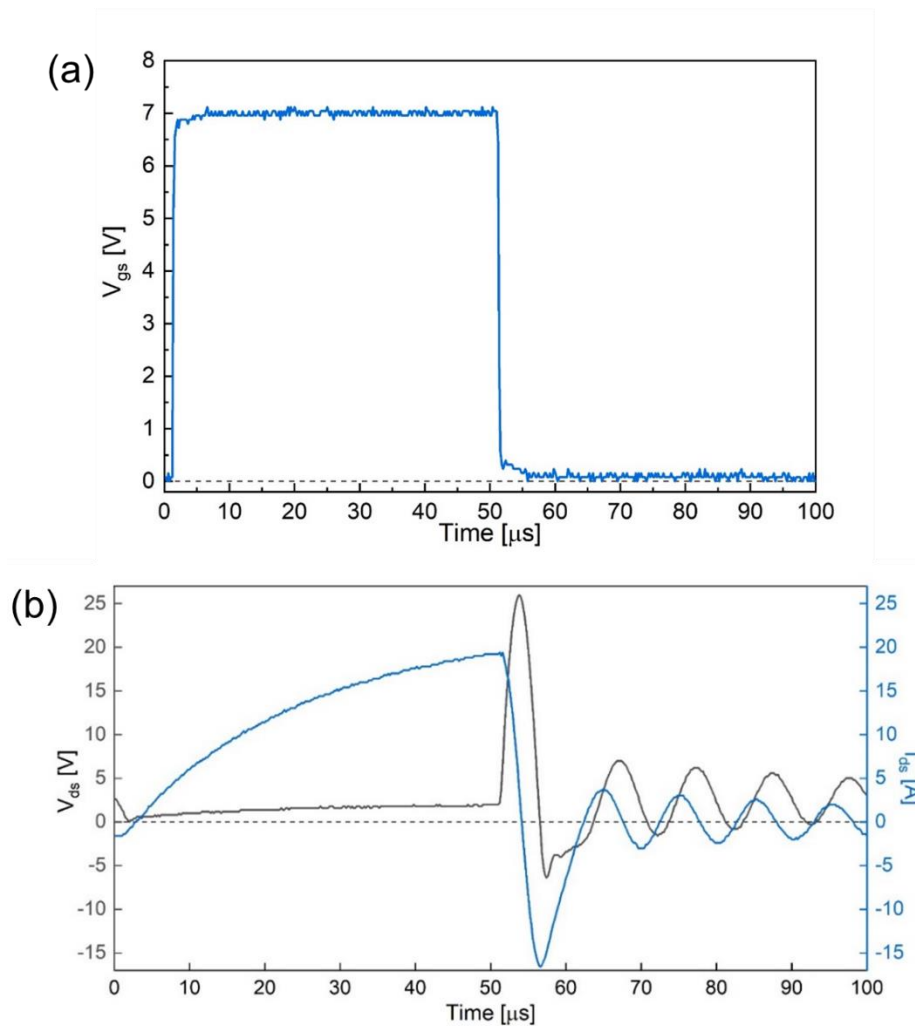


Figure 38. Time-resolved curves of V_{GS} , V_{DS} and I_{DS} during a cycle.

Figure 38(a) illustrates the V_{GS} signal used, characterized by a switching frequency of 10 kHz. This frequency is significantly lower than the maximum switching frequency of the Device Under Test (DUT). In **Figure 38(b)**, the drain-source voltage and current signals are presented. To reach the desired drain-source peak current at the end of the pulse, the V_{DS} was tuned to a low value of approximately 2.5 V. One of the key characteristics of GaN devices is their high switching speed, which stems from their architecture and material properties. This feature has significant implications from an application standpoint, as it requires specific layouts and careful system design. Additionally, it can pose challenges during testing. Due to the high di/dt and the inevitable inductance of the connecting wires, overvoltages and overcurrents can occur at the device terminals, potentially exceeding the operational limits defined by the device's Safe Operation Area (SOA). A simple strategy to mitigate this issue consists in clamping the signal directly at the device terminals by using a capacitor capable of handling the voltage levels induced by the di/dt . In our case due to the DUT high switching speed and the rapid decrease of I_{DS} , we observe an overshoot at approximately 50 μs . This behavior evident at 50 μs is followed by ringing phenomena (**Figure 38 (b)**).

4.3.4.1. Device characterization

DUT's pristine characteristics, prior to the aging test, are detailed in the preceding sections and serve as reference for evaluating the changes induced by stress testing.

After each stress session, we characterized the DUT as previously described, yielding the following results:

Electrical characterization

Figure 39 and **Figure 40** present the evolution during the pulse of the drain-source current (I_{DS}) and voltage (V_{DS}), respectively, after multiple stress sessions (as indicated in the legend).

From the recorded I_{DS} and V_{DS} data, the R_{DSON} values were calculated and presented in **Figure 41**. This graph quantifies the evolution of R_{DSON} with stress cycles, where we observe two distinct aging effects.

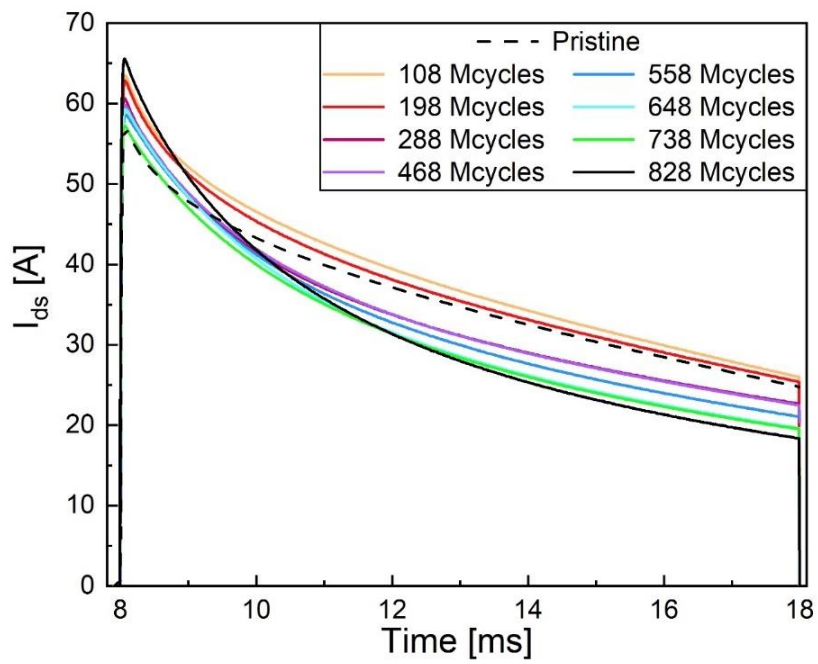


Figure 39. Dynamic behavior of I_{DS} throughout the ON pulse after the stress sessions.

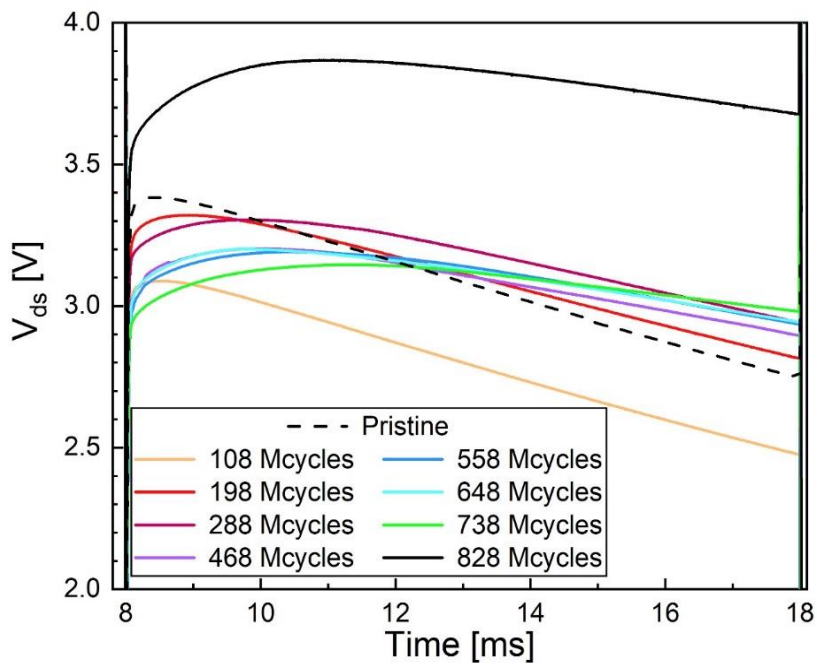


Figure 40. Dynamic behavior of V_{DS} throughout the ON pulse after the stress sessions.

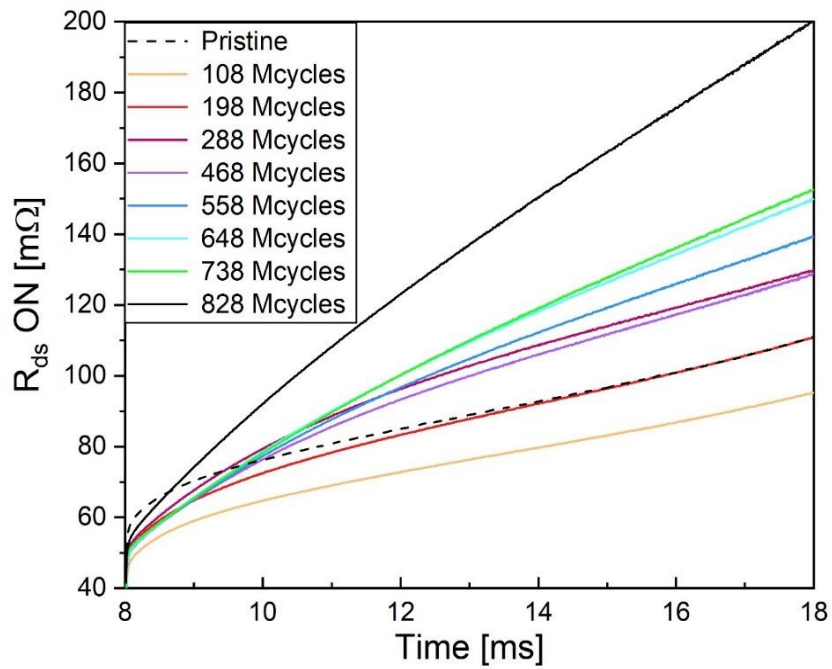


Figure 41. Dynamic behavior of R_{dsON} throughout the ON pulse after the stress sessions.

The most pronounced effect is the significant increase in R_{dsON} at the end of the pulse as stress cycles increase, ultimately reaching double the pristine value. The second important effect is observed in the dynamical behavior of the R_{dsON} , which grows faster as the device ages.

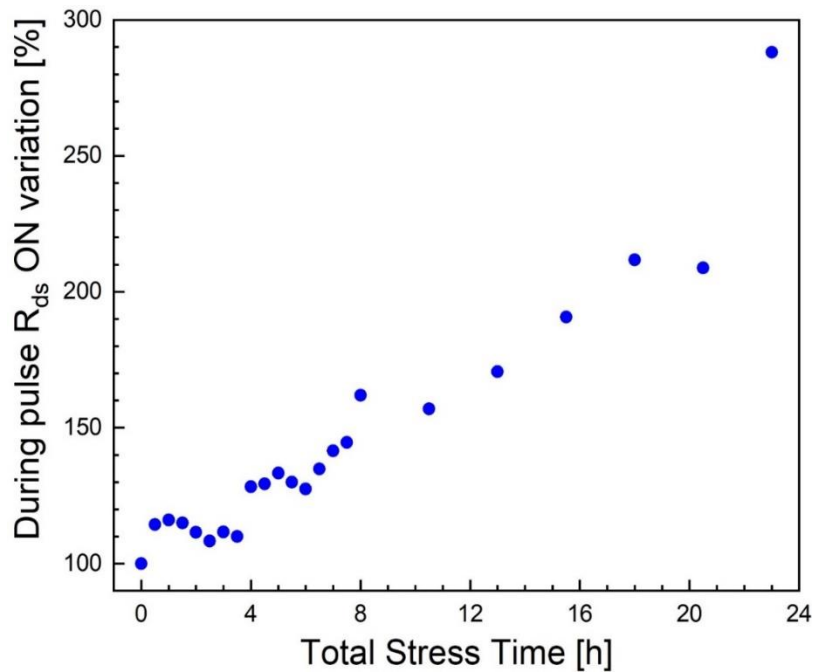


Figure 42. Drift of dynamic ON-Resistance ($R_{ds}(ON)$) over total stress duration (23 hours).

This graph illustrates the evolution of the dynamic $R_{DS(ON)}$ drift as a function of total stress time, expressed in hours.

As depicted in **Figure 41**, the initial measured values of $R_{DS(ON)}$ after each stress session are not exactly identical. Consequently, the y-axis represents the percentage variation of $R_{DS(ON)}$ during the characterization pulse that follows each stress session, calculated as the difference between the final and initial resistance values.

The data points reveal a distinct trend: $R_{DS(ON)}$ drift progressively increases with stress time. Initially, in the pristine state, the ON resistance exhibits a 100% increase (doubling) by the end of the pulse. With regard to the aged device, after 828 Mcycles, the variation becomes significantly more pronounced, reaching nearly a 300% increase (quadrupling) at the end of the pulse after 23 hours of stress.

This behavior underscores the substantial impact of prolonged stress on the device's on-resistance, emphasizing its critical role in the degradation and reliability of the device during operation. These insights are valuable for projecting the device's lifetime and assessing its long-term performance.

Thermal analysis

We measured the time-dependent surface temperature of the DUT following each stress session. In **Figure 43**, we plotted the mean temperature of the area highlighted in **Figure 31(a)**, revealing that the maximum temperature increases with advancing ageing, rising from 80°C to 180°C. Additionally, the device changes its cooling dynamics with time. Initially the device cools down exponentially after the pulse, however, with aging, the cooling behavior changes distinctly.

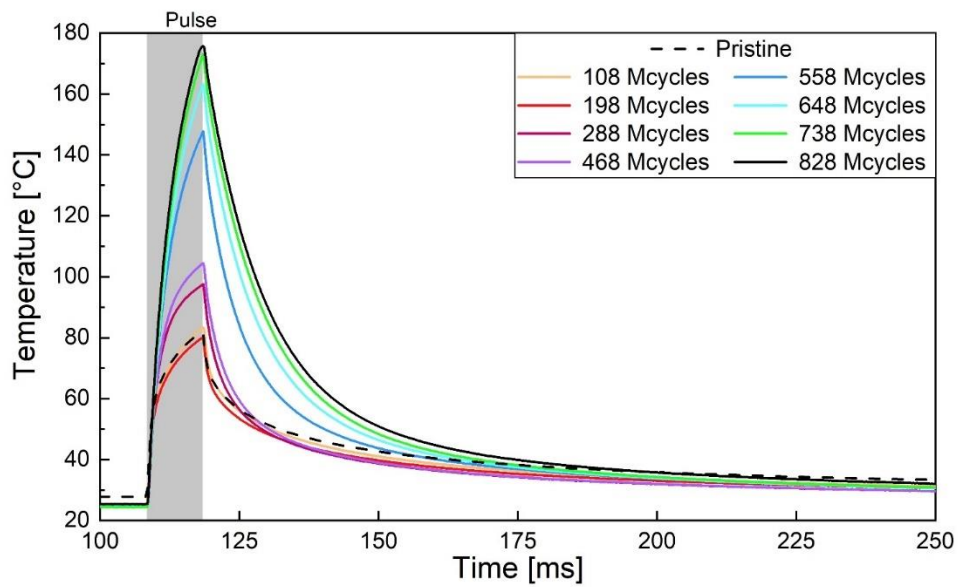


Figure 43. Thermal behavior of the device after power cycling sessions compared to the pristine state, with all measurements conducted in the specific zone indicated in **Figure 31(a)**.

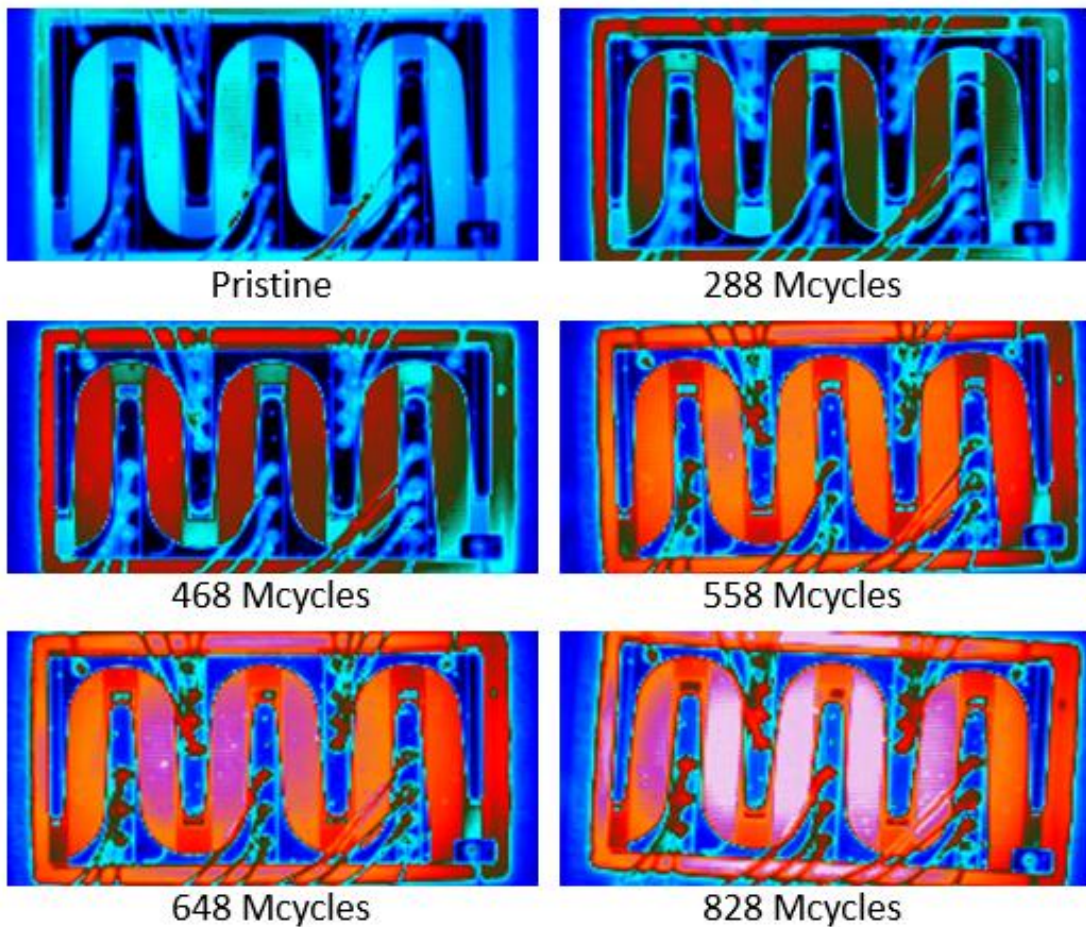


Figure 44. Thermal maps of the device captured at its peak temperature after different power cycling sessions.

The heating and cooling behaviors also change spatially, as clearly shown in **Figure 44**, which compares various snapshots captured at the end of the pulse after different sessions.

Throughout the aging process, the hottest region of the DUT shifts from the center toward one of the edges. In order to assess this asymmetrical trend in thermal distribution, we conducted a further analysis of the thermal measurements.

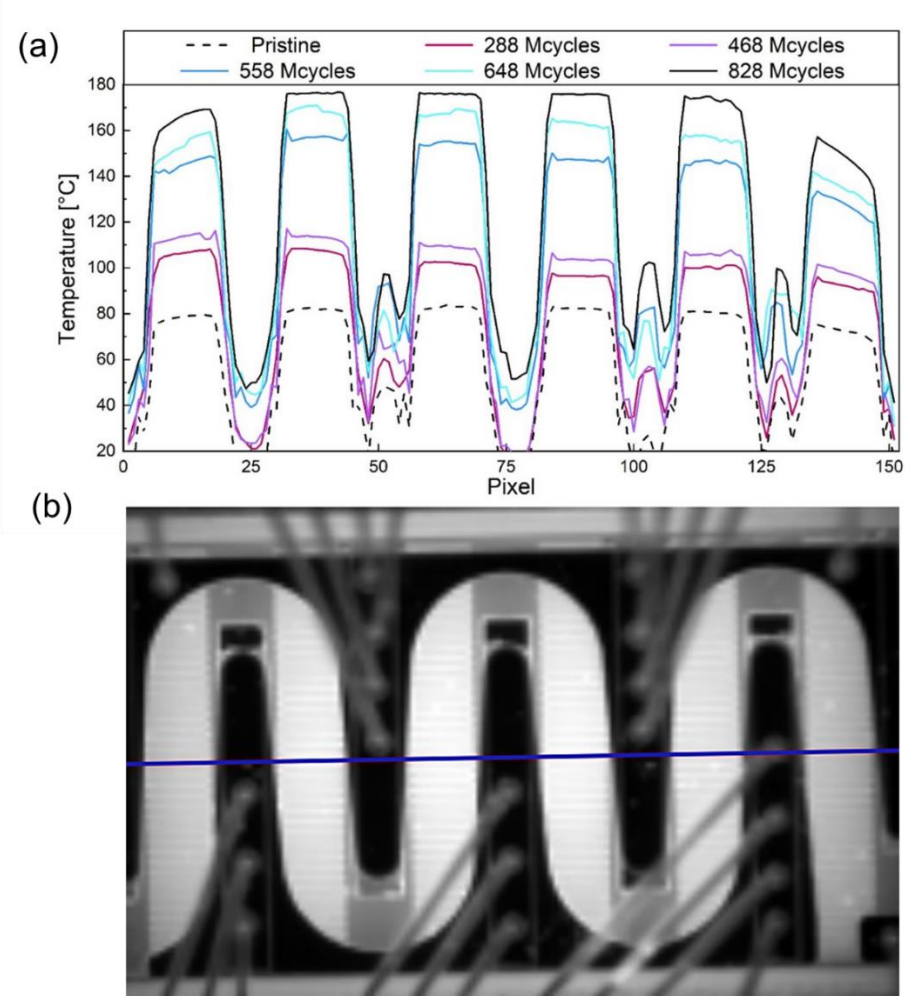


Figure 45. (a) Temperature distribution along horizontal line central to the device structure (demonstrated in (b)) after the stress sessions.

In **Figure 45(b)**, the horizontal line indicates the specific location across the device where the temperature variation analysis was conducted, as depicted in **Figure 45(a)**. The graph compares the temperatures of the six brighter areas along this line after various cycling sessions.

Compared to the pristine state, where the maximum temperature was centered on the device, we observe that the peak temperature shifts toward the left after aging cycles (as shown by the red, purple and blue lines in **Figure 45(a)**). However, after these aging stages, the temperature distribution reverts back to a pattern with central peak, resembling the pristine state.

Displacement analysis

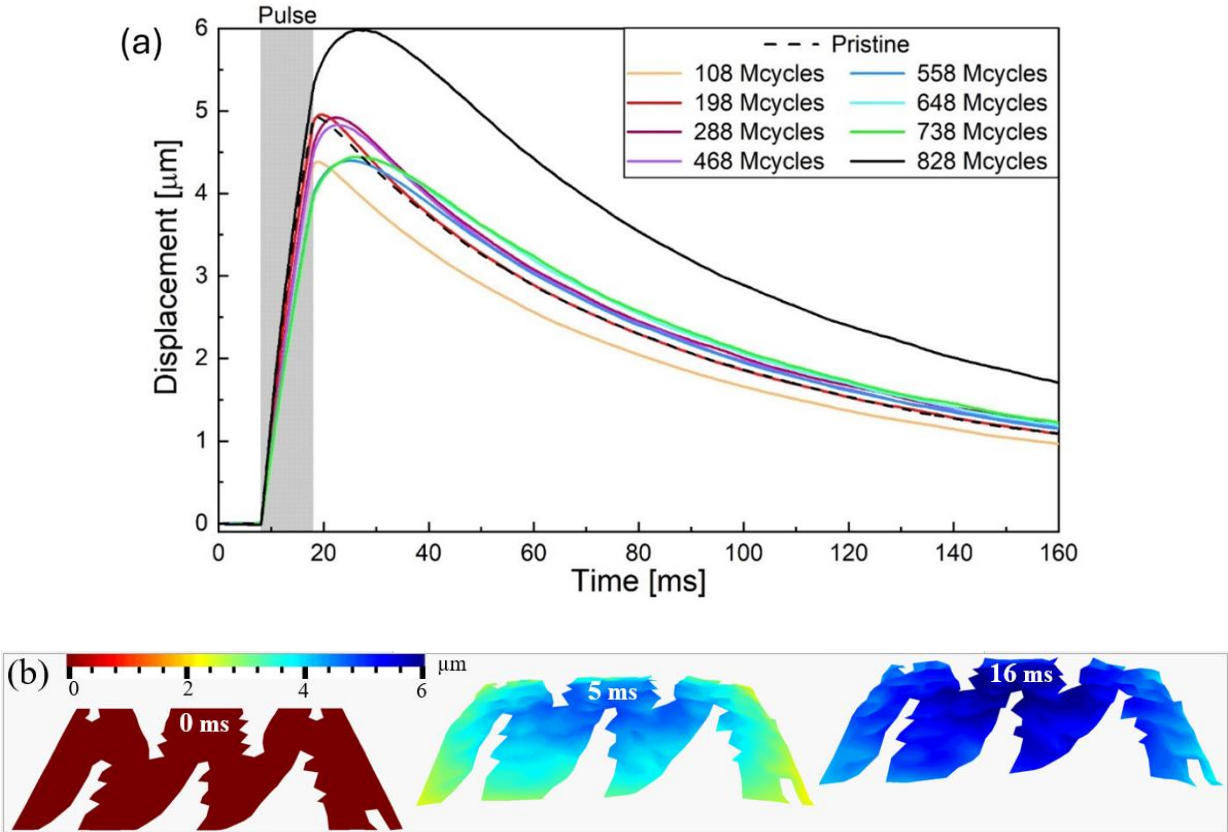


Figure 46. (a) Displacement measurements after each cycling session. (b) Scanning map of out-of-plane displacement recorded after the final cycling session (828 Mcycles).

Figure 46(a) shows the displacement response of the DUT after various levels of cycling sessions. We observe that the displacement increases rapidly during the pulse, however the peak displacement is reached progressively later in time after each cycling session, indicating a temporal shift in the device’s mechanical response.

After the final power cycling session, the device reaches a significantly higher peak displacement of approximately 6 μm , compared to the previous ages.

4.3.5. Discussion

The aging process was terminated at 828 million cycles since the device has reached a peak temperature of approximately 180°C, significantly exceeding its maximum operational temperature of 150 °C, to prevent further degradation and irreversible damage to the device.

A comparison of the data from **Figure 28** and **Figure 41** reveals that the $R_{DS(ON)}$ has substantially exceeded the static $R_{DS(ON)}$ value at 150 °C, 116 mΩ, after increasing cycling sessions. Additionally, variations were observed in the behavior of the dynamical $R_{DS(ON)}$ with aging. These findings reflect the significant degradation induced by the prolonged power cycling. The above highlight that the degradation effect impacts not only the static ON-resistance but influences the dynamic $R_{DS(ON)}$ as well [110] thereby significantly impacting the device's overall performance and reliability. Since higher values of $R_{DS(ON)}$ are reached, it is expected that the device will experience intensified heating phenomena due to Joule's law:

$$P = I^2R \quad (27)$$

To assess this effect, we analyzed the thermal measurement data. As stated by Joule's law, with the $R_{DS(ON)}$ increasing during the aging process, the device maximum temperature also increases. This effect is clearly demonstrated in **Figure 43**. Moreover, **Figure 44** reveals non-uniform heat dissipation across the device, with some areas dissipating more heat than others. These regions are likely to degrade more rapidly, thereby shortening the overall device lifetime. The observed non-uniform heat dissipation may be attributed to variations in local $R_{DS(ON)}$ values across the device. Areas with lower local $R_{DS(ON)}$ value could carry a higher proportion of the total I_{DS} , leading to more intense heating and accelerated degradation in those areas. This localized degradation can alter the current flow paths within the device, shifting the preferred current path to less degraded areas and consequently modifying the thermal distribution, as shown in **Figure 44**. After the 738-million-stress cycles, the device attained a peak temperature of approximately 180°C, which persisted also in the next thermal characterization. This result suggests that the area experiencing the maximum temperature at 738 million cycles had degraded to such an extent that subsequent stress sessions caused other areas to undergo intensified degradation. This process likely expanded the region experiencing the maximum temperature of 180°C.

The aforementioned hypothesis may explain the progression of thermal distribution observed in **Figure 44**, as it reflects the redistribution of thermal heat due to localized damage. These results emphasize the critical role of non-uniform degradation in influencing the thermal and electrical behavior of the device and its eventual failure mechanisms. Further evidence of the increased thermal stress experienced within the central areas is provided by the optical image in **Figure 47**, which shows more pronounced degradation of the DUT's upper layer in these areas compared to the extremities.

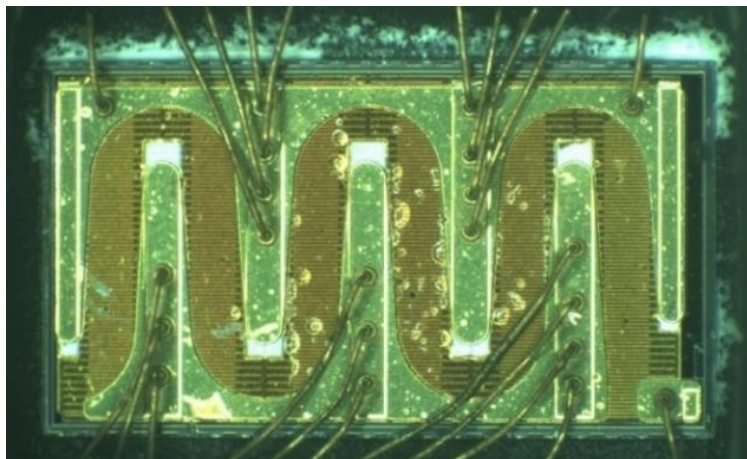


Figure 47. Optical images of Device Under Test after power cycling sessions.

The heating process induces structural deformation due to thermal expansion:

$$\Delta V = \beta V_0 \Delta T \quad (28)$$

Where:

β : Coefficient of volumetric thermal expansion.

As predicted by the equation, the displacement analysis reveals a behavior that closely mirrors the thermal characterization. This is true both for the temporal shift in device response after stress sessions, as shown in **Figure 46(a)**, as well as for the non-uniform spatial distribution of the out-of-plane deformation, as revealed by the analysis of **Figure 46(b)** and the displacement maps after other sessions.

The thermal expansion process affects the entire DUT volume; however, we measure only the displacement in the out-of-plane direction, hence reflecting the linear expansion process along that axis. The measured deformation represents the cumulative effect of the expansion across

all layers of the device, each characterized by distinct thermal expansion coefficients. The disparity in these coefficients between layers introduces, in addition to the mechanical strain, a mechanical stress, significantly contributing to device degradation. This effect is exacerbated by the non-uniform heat dissipation across the device, resulting in intensified deformation in areas experiencing peak temperatures, which accelerates the device degradation. Effectively, according to data in **Figure 46(a)**, the device experiences significant measurable displacement after each cycling session. Initially, the device shows a peak displacement of approximately $5\mu\text{m}$, increasing to $6\mu\text{m}$ after the final cycling session. These displacement values are significant with respect to the device's dimensions, underscoring a considerable mechanical impact that could influence its structural integrity and operational reliability. Furthermore, a notable observation is the deceleration of strain release or relaxation after successive stress sessions. The extended relaxation time has a significant impact since the mechanical stress continues to degrade the device until the strain is fully relieved. This behavior correlates with the observed reduction in cooling rates as the device ages, providing critical insights into its evolving state. These observed effects are likely attributed to material degradation, which compromises the device's thermal management capabilities, thus impairing the efficiency of heat dissipation and further contributing to the thermal and mechanical stresses within the device.

4.3.6. Conclusion

This work has verified that thermomechanical strain plays a critical role in device degradation. This degradation is clearly reflected in the evolution of dynamical $R_{\text{DS(ON)}}$ behavior. The progressive rise in $R_{\text{DS(ON)}}$ induces greater heat generation, which we observed as a significant increase in device's surface temperature. These elevated temperatures, in turn, drive more pronounced thermal expansions, which we assessed through displacement measurements. The displacements induce prolonged mechanical stress, amplifying the extent of degradation per cycle. Additionally, the degradation is further accelerated by the non-uniform distribution of these deteriorating mechanisms across the device, which shortens its overall lifetime.

Conclusion and perspective

The primary objective of this thesis was to conduct a comprehensive reliability assessment of gallium nitride high-electron-mobility transistors (GaN HEMTs), focusing on two critical aspects: analyzing the impact of packaging on stress distribution within the active layers of the device, and evaluating the influence of thermal and thermomechanical phenomena on dynamic ON-resistance ($R_{DS(ON)}$) during power cycling. This research adopted an approach to provide critical insights into enhancing the performance and lifetime of wide-bandgap power electronic devices, with particular emphasis on GaN HEMTs.

In chapter 1, a comprehensive overview of semiconductor materials was presented, emphasizing their fundamental properties and critical role in power electronics. Special emphasis was placed on wide-bandgap semiconductors, including Gallium Nitride and Silicon Carbide, highlighting their advantages over traditional silicon-based technologies and their potential for power electronic systems.

Building on this context, Chapter 2 explored the reliability challenges of WBG-based power devices, with a particular focus on failure mechanisms specific to GaN HEMT chips. Additionally, the reliability challenges associated with WBG device packaging were presented. The chapter concluded by introducing reliability models previously developed by researchers to predict the lifetime of Silicon-based devices.

Chapter 3 provided an experimental evaluation of GaN HEMT reliability by analyzing stress distribution in AlGaN/GaN HEMTs induced by a novel packaging design. The chapter began with an introduction to residual stress in electronic packaging and the non-destructive techniques used for its assessment. Micro-Raman spectroscopy was employed to precisely quantify residual stresses induced by packaging within the device's active layers. A data-fitting approach was applied to analyze the frequency shift of the GaN E2(high) phonon mode, chosen for its high sensitivity to crystalline stress. A comparative analysis of the Raman spectral

characteristics of packaged and bare devices revealed the influence of packaging on stress distribution.

A comprehensive analysis of Raman measurements, combined with the linear correlation between Raman frequency shifts ($\Delta\omega$) and stress (σ), revealed the presence of tensile stress in the bare device, whereas compressive stress was observed in the packaged device. This compressive stress was found to mitigate approximately 0.1 GPa of tensile stress, effectively reducing the intrinsic stress within the wafer-level structure. This finding demonstrated that beyond its protective and structural roles, packaging actively contributes to stress management, enhancing device performance and reliability. These results underscore the importance of optimizing packaging designs to minimize mechanical stress and preserve the structural integrity of GaN HEMTs.

In Chapter 4, the focus shifted to the reliability of GaN HEMTs by examining the effects of thermomechanical strain on dynamic ON-resistance during power cycling. Using advanced characterization techniques, including high-speed infrared imaging and scanning vibrometry, the study identified a strong correlation between thermal, mechanical, and electrical phenomena. Device characterization under short-circuit conditions revealed a general increase in dynamic ON-resistance ($R_{DS(ON)}$) during single-pulse operation, highlighting its transient behavior. Thermal imaging showed significant temperature increases and non-uniform heat distribution across the device, while displacement measurements revealed heterogeneous thermomechanical effects. Together, these findings established a clear correlation between thermal phenomena and mechanical deformation.

Successive stress sessions revealed a progressive increase in $R_{DS(ON)}$, driven by localized heating and thermomechanical strain, which intensified stress in specific regions due to uneven heat dissipation. This accelerates localized degradation, ultimately reducing the device's operational lifetime. These results highlight the critical importance of thermal management strategies and material resilience in mitigating these effects and ensuring the reliability of GaN HEMTs.

By addressing both the initial packaging stage and the challenges associated with operational aging, this thesis contributes to the field of power electronics by providing a dual perspective on GaN HEMT reliability, impacted by both mechanical stress and strain. The insights gained from this work contribute to the ongoing efforts in the field of power electronics to enhance

the understanding of reliability in power devices and provide a foundation for the development of robust and reliable systems capable of meeting the growing demands of energy-efficient and critical applications. Future work could explore extending this study to other wide-bandgap materials or integrating additional factors such as system-level interactions.

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