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METAL-OXIDE-METAL (MOM) CAPACITORS AND GaN-BASED HIGH ELECTRON MOBILITY TRANSISTORS (HEMTs) DEVICES FOR INTEGRATED CIRCUITS: A RELIABILITY STUDY

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ABSTRACT

In the present thesis, Metal-Oxide-Metal (MOM) based on silicon (Si) substrates and high electron mobility transistors (HEMTs) devices based on Gallium Nitride (GaN), both provided by *STMicroelectronics S.r.l.*, underwent to a systematic reliability investigation through, respectively, thermal characterization and micro-Raman spectroscopy. In the first case, the aim was to establish a reliable and efficient alternative approach to detect any non-functional MOM-based devices, evaluating the thermal emission. Such technique allows to overcome the limits arising from the conventional electrical tests that are not able to detect some non-functional devices thus constituting a reliability risk. In particular, ad-hoc devices, known as *test pattern*, characterized by at least 4-times larger MOM area with respect to the "standard" BCD8 device, were utilized to enhance the probability to intercept reliability issue and hence their correct functionality. The obtained results revealed, as a general trend, a close correlation with the preliminary analyses performed through both visual inspection and current-voltage (I-V) analysis, proving that the technique is reliable and quick in the detection of non-functional MOM capacitors.

In the case of HEMTs GaN-based device, two different micro-Raman investigations were undertaken. The first was mainly focused on the evaluation of the internal stresses occurring in GaN crystals, starting from the analysis of the frequency shifts exhibited by specific spectral features, upon the application of an external mechanical perturbation by means of home-made three-point assembly. The second investigation was aimed at quantify the packaging impact on the residual stress along the GaN and GaN/Si interfaces, by analysing the frequency shifts induced by the device packaging on specific spectral components. It is worth of note that the device packaging, although its application typically provides non-negligible residual stresses which can, in principle, originate reliability failures, possesses several key functions in protecting the device core from the external environment.

As main results, a high-frequency shift of the E_2(high) frequency centre in the case of packaged sample was observed, indicating a compressive stress closely to the package.

It is worth of note that the results reported in this thesis appear crucial not only for ensuring better performance and reliability in MOM and HEMTs-based devices and technology, but also could provide, in principle, useful notions to be implemented in large-scale semiconductor industrial processes.

CHAPTER 1
SEMICONDUCTOR MATERIALS

1.1 **A survey of semiconductors**

Semiconductors (SCs) are the fundamental building blocks of modern electronics and constitute the foundation of the electronic-based industries, thus providing a crucial boost to the world of technology. Such materials behave, in terms of their ability to conduct electrical current, between conductors and insulators, making them necessary for the operation of electronic devices, *i.e.* simple diodes, transistors, MOSFET, complex integrated circuits and microprocessors [1,2]. The term “semiconductor” was introduced in 1782 by A. Volta to describe a class of materials with characteristics intermediate between conductors and insulators, but the first documented observation of an effect due to the phenomenon of semi-conductivity is due to M. Faraday who, in 1833, discovered that certain non-metallic compounds, such as silver sulphide (Ag_2S), tend to become better conductors of electricity at high temperatures, unlike common metals. In 1879, the observation by E. Hall of a non-negligible potential difference between the opposite faces of an electric conductor induced by a magnetic field oriented perpendicular to the current flow, known as *Hall effect*, furnished an extremely powerful method to quantify the process of electrical conduction in materials. Such effect was originally observed in few elements, such as germanium (Ge), silicon (Si) and antimony (Sb), or in compounds such zinc-blende (ZnS), galena (PbS), cuprite (Cu_2O) and silicon carbide (SiC). However, the influence of the electrical behaviour by several factors such as chemical composition, presence of impurities and heat treatments, made their systematic study a complex challenge.

The application of quantum mechanics to the study of solids, through the theory of electronic level bands, due to A. H. Wilson in 1931, provided the background rules for understanding of the principles which regulate both electrical and optical properties of semiconductor materials [3]. Important work conducted at the Bell Laboratory in

Murray Hill (USA), by J. Bardeen, W. H. Brattain and W. B. Shockley in the mid-20th century, yielded to the definition of new criteria for classifying semiconductors, as well as to important technological inventions, such as the bipolar junction transistor in 1948, which ushered in the modern electronic era [4].

Formally, a semiconductor is defined as a material with electrical resistivity lying in the range of 10^{-2} - 10^{9} Ω cm^{-1} or, equivalently, with an energy bandgap between 0 and 4 electron volts (eV) [5]. In nature, semiconductors can occur with a large variety of crystal structures forming *elemental*, *binary*, *ternary, quaternary, layered* and *organic* semiconductors [1].

The most renowned *elemental* semiconductor is undoubtedly silicon (Si), which exhibits excellent properties at room temperature for most common applications with minimal economic impact. In fact, 25% of the Earth's crust is made of Si in the form of silica and silicates, followed only by oxygen in term of abundance. Noteworthy, elemental semiconductors based on Ge, selenium (Se) and carbon (C) (in the form of C_{60} or nanotubes) as well as on other elements of the groups V and VI of the periodical table (i.e. phosphorus (P), sulphur (S) and tellurium (Te)), can be also found.

The combination of two elements from the periodic table results in *binary* compound semiconductors, *i.e.* gallium arsenide (GaAs, III–V compound), zinc sulphide (ZnS, II–VI compound), mercury telluride (HgTe), lead sulphide (PbS, IV–VI compound), lead tellurite (PbTe, IV–VI compound), tin sulphide (SnS, IV–VI compound) and gallium nitride (GaN, III–V compound). The specific combination of elements determines the properties of the resulting semiconductor compound, making them suitable for different applications in electronics, optoelectronics, and power devices [6].

In addition to *binary* compounds, *ternary* semiconductors, such as $Al_xGa_{1-x}As$, and *quaternary* semiconductors of the $A_xB_{1-x}C_yD_{1-y}$ type, can be also obtained starting from a combination of *elemental-binary-ternary* species (*i.e.* GaP, InP, InAs, and GaAs to form the $Ga_xIn_{1-x}As_yP_{1-y}$ alloy semiconductor). However, in contrast to *elemental* semiconductors, the production in single-crystals of the aforementioned *ternary* and *quaternary* compounds often entails significantly more intricate and involved procedures [7–9].

Going on, *layered* semiconductors gained considerable attention due to the quasi-two-dimensional behaviour exhibited by electrons within the layers, particularly appealing in the view of the realization of high-speed logic electronics and high-performance IR detectors [10–12]. Lead iodide (PbI_2), molybdenum disulfide (MoS_2) and gallium selenide (GaSe), characterized by a layered crystal structure, represent some of the most promising narrow bandgaps and high mobility layered materials of this class [13,14]. Interestingly, the addition of foreign elements allows the possibility to control and modulate the strength of the interactions between different layers (known as *intercalation* process), opening to a new set of advantages and potential applications [15,16].

Finally, *organic* compounds, including polyacetylene $(CH_2)_n$ and polydiacetylene, despite not currently employed in electronic devices, offer promising solutions for different electronic devices such as OLED displays [17–19], organic transistors [20–23] and memory devices [24,25]. By selective functionalization of specific functional groups of such organic semiconductors, especially those with conjugate bonds like –C=C–C=, significant optical nonlinearity can be achieved, making them highly relevant for optoelectronic applications. Noteworthy, new forms of carbon, such as C_{60} (fullerene), have been identified as semiconductors. Carbon nanotubes (CN), formed by rolling graphite sheets into nanometer-scale tubes, have also emerged as a promising variation, offering versatility and adaptability in designing electronic circuits [26–30].

1.2 **Energy-Momentum Diagram**

Let's consider a silicon crystal composed of *N* Si atoms interacting with each other. With the decrease of the interatomic distance, the electronic *3s* (*i.e.*, for n = 3 and ℓ = 0) and *3p* (*i.e.*, n = 3 and ℓ = 1) subshells of each Si atom, holding the relatively weakly bounded 4 valence electrons (of a total of 14) which can be involved in chemical reactions, underwent to a significant overlap, yielding to the onset of a single band of 8 *N* states.

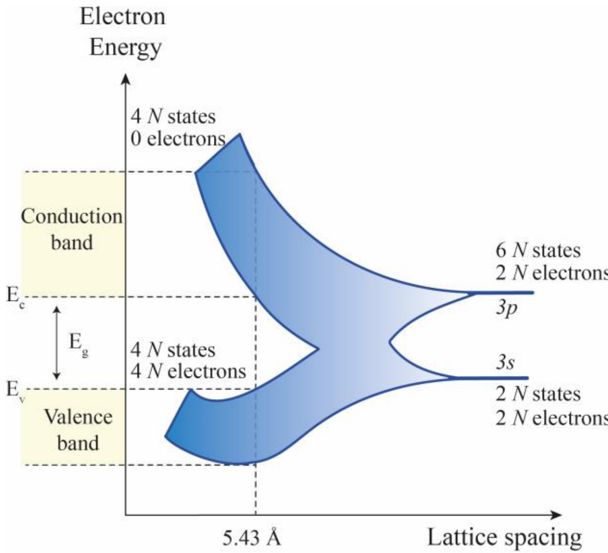


Figure 1: *Formation of energy bands as a diamond lattice crystal is formed by bringing isolated silicon atoms together.*

The minimum of the total energy imposes equilibrium interatomic distances, and the bands split again into two different bands, known as *valence* (lower, VB) and *conduction* (upper, CB) bands, each consisting of 4 *N* states. At T = 0 K, electrons naturally tend to occupy all the lowest energy states thus filling completely the VB. In such condition, the CB will be empty. The *bandgap* energy E_g, accounting for the width of the forbidden energy gap between the two bands, is then E_c–E_v, respectively associated to the bottom and the top of the CB and VB (Figure 1). In particular, E_c corresponds to the potential energy of an electron, *i.e.* the energy of a conducting electron when it is at *rest*, while E_v corresponds to the potential energy of a *hole*. Both the electrons in the conduction band and holes in the valence band contribute to the

electrical conductivity. Intrinsic conductivity and intrinsic carrier concentrations are largely controlled by the E_g/k_BT factor, *i.e.* the ratio between the *bandgap* energy and temperature. It is worth of note that the higher the E_g/k_BT factor is, the lower the intrinsic carrier concentration and conductivity will be.

In the case of electrons affected by the periodic potential of the nuclei, their energy E can be written as:

$$E = \frac{p^2}{2m_e} \tag{1}$$

where p is the momentum and m_e is the electron effective mass. The E *vs.* p plot thus provides a simple convex parabola. For silicon, the energy-momentum diagram assumes a much complex behaviour, which strongly depends on the chosen crystal direction (see Figure 2).

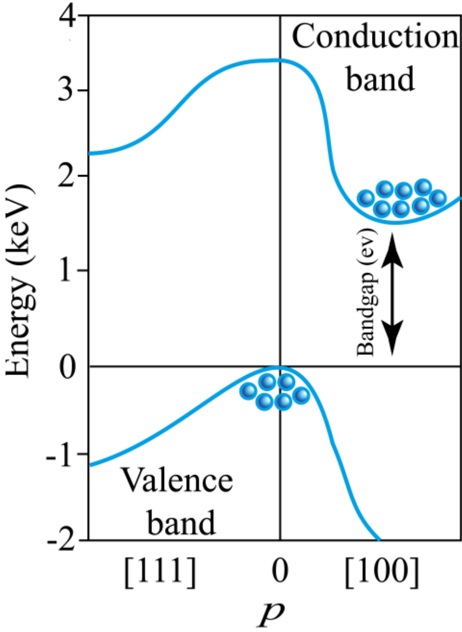


Figure 2: *Energy band structure of Si.*

Generally, when the conduction band's minimum point is located at $p = 0$ (typical of semiconductors exhibiting partial ionic bonding, especially those with polar characteristics), it implies, in some cases, not only a uniform effective mass for electrons in all crystal directions, but also that electron motion remains uninfluenced

by the crystal's orientation. Conversely, minimum of the conduction band at $p \neq 0$ yields to a directional-like behaviour of such electrons. In the case of silicon, an electron transition from the VB to the CB always requires an energy ($\geq E_g$) and momentum ($\geq p_c$) changes, and for this reason it is known as *indirect semiconductor*. Other examples of *indirect semiconductor* are germanium (Ge), silicon carbide (SiC) and aluminium antimonide (AlSb). When the top of the VB and the bottom of CB occur at $p=0$, an electron transition only requires an energy change, forming the so-called *direct semiconductor, i.e.* gallium arsenide (GaAs) and gallium nitride (GaN).

1.3 ***Intrinsic semiconductors*** **(I-SCs)**

The impurities naturally present in crystals generate localised states within the gap, often closely to the VB or CB. At a given temperature, the thermal activity yields to the "ionization" of such localized states resulting in an increase in conductivity. An *intrinsic semiconductor* (I-SC) is characterized by minor amount of impurity compared to the thermally generated electrons and holes. In I-SC, the electron density *n(E)*, accounting for the number of electrons per unit volume, is determined by the multiplication of the density of states, *N(E)* $(cm^3 \cdot eV)^{-1}$, which represents the count of permissible energy states (considering electron spin) within a given energy interval per unit volume, and the probability of occupying that energy range *F(E)*, modulated by the Fermi-Dirac distribution function (Eqn. 2)

$$F(E) = \frac{1}{1 + e^{\frac{E-E_f}{kT}}}, \tag{2}$$

Where k, T and E_f are the Boltzmann constant, absolute temperature (K) and the energy of the *Fermi level*, respectively.

For $E \geq E_f \pm 3kT$, Eqn. 2 can be simplified as:

$$F(E) \cong e^{-\left(\frac{E-E_f}{kT}\right)}, \qquad \text{for } E - E_f > 3kT \tag{3}$$

$$F(E) \cong 1 - e^{+\left(\frac{E-E_f}{kT}\right)}, \qquad \text{for } E - E_f < 3kT \tag{4}$$

Thus, the electron concentration n (cm^{-3}) existing in the CB can be achieved by integrating $N(E)F(E)dE$ from the bottom (assumed as $E=0$) to the top (E_{top}) of the CB (Eqn. 5).

$$n = \int_0^{E_{top}} n(E)dE = \int_0^{E_{top}} N(E)F(E)dE. \quad (5)$$

In Figure 3, a schematical representation of the band diagram, $N(E)$, Fermi-Dirac distribution function (Eqn. 2) and the carrier concentrations for an intrinsic semiconductor, is displayed.

By substituting Eqn. 3 into Eqn. 5, and considering the behaviour of the $N(E)$ as a function of energy, the electron concentration n became:

$$n = \frac{2}{\sqrt{\pi}} N_C (kT)^{\frac{3}{2}} \int_0^{\infty} \sqrt{E} e^{-\left(\frac{E-E_f}{kT}\right)} dE, \quad (6)$$

with N_C *effective density of states* in the CB, equal to 2.86×10^{19} cm^{-3} and 1.2×10^{18} cm^{-3} in the case of Si and GaN SCs (at room temperature), respectively.

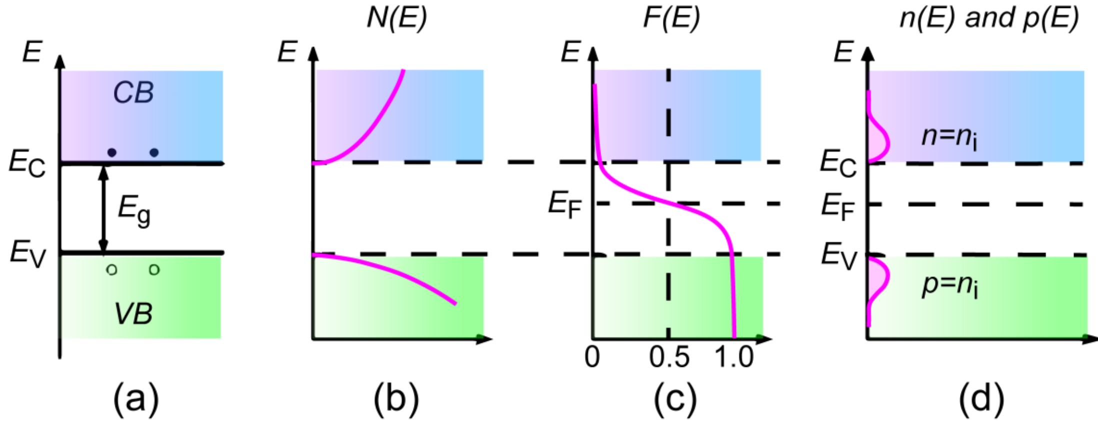


Figure 3: *(a) schematic band diagram, (b) density of state, (c) Fermi distribution function and (d) carrier concentration for a I-SC.*

By defying the bottom of the CB as E_c instead of 0, the electron density in the CB turns out to be:

$$n = N_c \, e^{-\left(\frac{E_c - E_f}{kT}\right)}. \tag{7}$$

In a similar way, the hole density p in the VB can be obtained as:

$$p = N_v \, e^{-\left(\frac{E_f - E_v}{kT}\right)}, \tag{8}$$

Where N_V *is effective density of states* in the VB, equal to 2.66×10^{19} cm^{-3} and 4.01×10^{19} cm^{-3} in the case of Si and GaN SCs (at room temperature), respectively.

For I-SCs, the density of electrons in the CB corresponds to the density of holes in the VB, which means that $n = p = n_i$, with n_i equal to the *intrinsic carrier density* (as can also be noted by the extension of the shaded areas in Figure 3d). Starting from Eqns. 7 and 8, the Fermi level can be written as:

$$E_f = E_i = \frac{E_C + E_V}{2} + \left(\frac{kT}{2}\right) \ln\left(\frac{N_V}{N_C}\right), \tag{9}$$

At T = 300 K, the second term is negligible with respect to the bandgap and hence the intrinsic Fermi level E_i typically lies close to the middle of the bandgap. Accordingly, the intrinsic carrier density became:

$$np = n_i^2 = N_C N_V e^{-\left(\frac{E_g}{kT}\right)}, \tag{10}$$

with $E_g \equiv E_C - E_V$.

1.4 ***Extrinsic semiconductors*** **(E-SCs)**

Extrinsic semiconductors (E-SCs), also known as *doped* SCs, are materials containing impurity atoms, intentionally introduced into the SC crystal lattice, which are able to deeply modify the SC's electrical properties due to the introduction of new energy levels (EL) lying within the bandgap. Depending on the nature of the

impurities, E-SCs can be divided in two classes, negative-type (n-type) and positive-type (p-type).

Replacing a Si-atom with an As-atom (having five valence electrons), four covalent bonds are preserved with its four neighbouring Si-atoms, while the fifth external electron has a sufficiently low binding energy with its As-atom, and hence it can be “ionised”. Since the impurities belonging to the V group of the periodic table "donate" additional electrons, which become *conduction electrons* at moderate temperatures, they are called *donors*. Simultaneously, silicon becomes n-type *SCs* due to the addition of negative charges. Elements such as P (phosphorus) and Sb (antimony) are also commonly used as donor impurities. Vice versa, if a Si-atom is substituted by a B-atom, characterized by three valence electrons, a *hole* is created in the VB so that an additional electron is accepted to form the fourth covalent bonds with neighbouring Si-atoms. In this case, the B-atom is defined as *acceptor*, and the material become of the p-type due to an excess of positive charge carriers populating the VB. Common acceptor impurities are B (boron), Ga (gallium), and In (indium) belonging to the III group of the periodic table.

The *ionization energy,* defined as the minimum energy required to remove the external electron form an atom, for the donor E_D can be expressed as:

$$E_D = \left(\frac{\varepsilon_0}{\varepsilon_s}\right)^2 \left(\frac{m_n}{m_0}\right) E_H, \tag{11}$$

Where ε_0, ε_s, m_n, m_0 and E_H are free-space permittivity, semiconductor permittivity, effective mass, free-electron mass and energy levels for an isolated hydrogen atom (given by the Bohr model), respectively.

In the case of n-type SCs, the thermal energy at room temperature exceeds E_D, ionising all donor impurities, thus delivering the same number of electrons within the CB. Under such circumstance, a *complete ionisation* is achieved, and the electron density becomes equal to the donor concentration N_D:

$$n = N_D, \tag{12}$$

Considering Eqns. 7 and 12, the Fermi level for n-type SCs became:

$$E_C - E_f = kT \ln\left(\frac{N_C}{N_D}\right), \tag{13}$$

with N_C effective density of states and N_D donor concentration. Eqn. 13 reveals that the enhancement in donor concentration leads to the reduction of the E_C-E_f term, which means that the Fermi level shift towards the bottom of the CB. In Figure 4 the carrier concertation for n-type SCs is displayed, in this case the electron concentration n (upper shaded area) is much greater than the hole concentration p (lower shaded area).

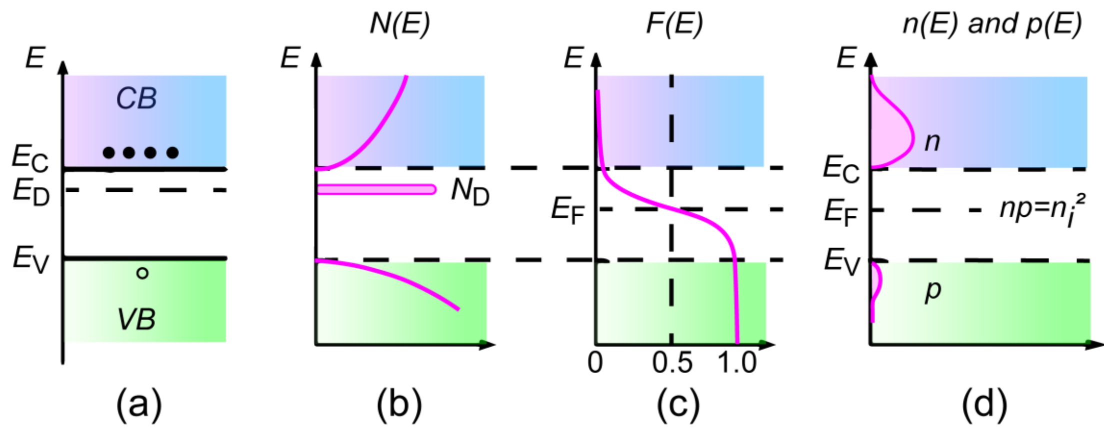


Figure 4: *(a) schematic band diagram, (b) density of state, (c) Fermi distribution function and (d) carrier concentration for a n-Type SC.*

In the same way, it is possible to write, for p-type SCs, the holes concentration, equal to acceptor concentration N_A, and the Fermi levels, starting from Eqns. 8 and 12:

$$p = N_A, \tag{14}$$

$$E_f - E_V = kT \ln\left(\frac{N_V}{N_A}\right), \tag{15}$$

In contrast with the previous case, when the acceptor concentration is high, the Fermi level will shift towards the top of the VB.

It is worth of note that the simultaneous occurrence of both *donor* and *acceptor* impurities within the SC crystal yields, owing to the change neutrality condition, to an

equal concentration of the total negative and positive charges arising from electrons and ionized acceptors, and holes and ionized donors, respectively.

At high temperature and/or $E_A \ll E_f \ll E_D$:

$$n + N_A = p + N_D. \tag{16}$$

By equating Eqn. 10 and 16 and the electron (n_n) and hole (p_n) concentration for *n*-type SCs can be written as:

$$n_n = \frac{1}{2}\left[N_D - N_A + \sqrt{(N_D - N_A)^2 + 4n_i^2}\right] \tag{17}$$

$$p_n = \frac{n_i^2}{n_n}. \tag{18}$$

With electrons and holes representing the *majority* and *minority* carriers, respectively. Similarly, the hole (p_p) and electron (n_p) concentration for *p*-type SCs can be obtained as:

$$p_p = \frac{1}{2}\left[N_A - N_D + \sqrt{(N_A - N_D)^2 + 4n_i^2}\right] \tag{19}$$

$$n_p = \frac{n_i^2}{n_p}. \tag{20}$$

In the case in which the impurity concentration $|N_D - N_A| \gg n_i$, Eqns. 17 and 19 can be simplified:

$$n_n \approx N_D - N_A, \qquad \text{if} \qquad N_D > N_A \tag{21}$$

$$p_p \approx N_A - N_D \qquad \text{if} \qquad N_A > N_D. \tag{22}$$

In Figure 5, as example, the trend of the computed electron density for Si and 2H-GaN structures as a function of temperature (*T*), at two different donor concentration [31]. At low temperature, the electron density (*n*) is less than the donor concentration due to the fact that the thermal energy is not sufficient to ionize all donors therefore some

electrons are locked at the donor level. At higher temperatures, the ionisation process is completed and remains stable for a wide range of *T*, in this case the *extrinsic region* is reached.

By further increasing the temperature over specific point (depends on both impurities concentration and bandgap value) the *intrinsic region* is also achieved, here the intrinsic carrier concentration is comparable to the donor concentration.

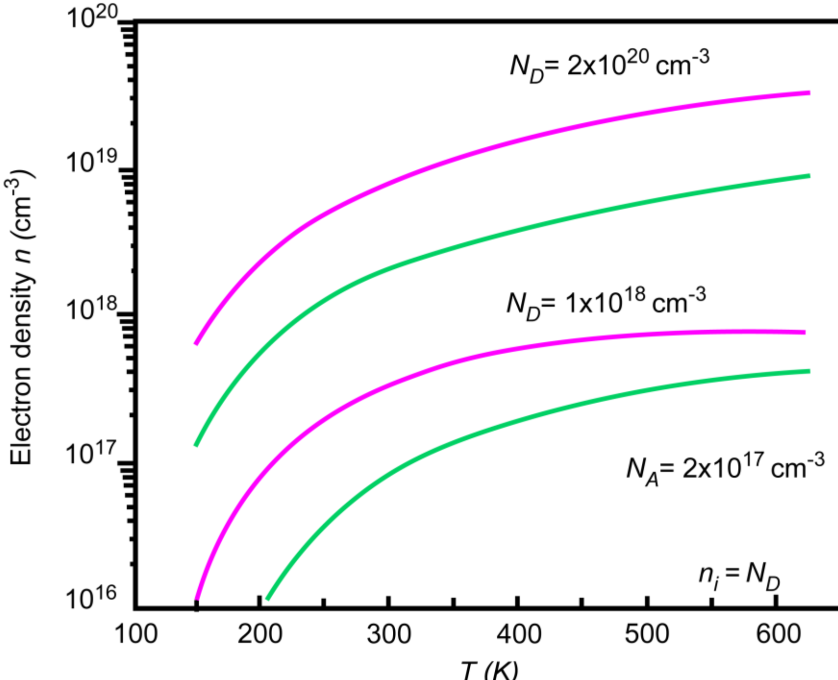


Figure 5: *Computed electron density (n) as a function of temperature for Si (purple line) and 2H-GaN (green line) at different donor concentrations.*

CHAPTER 2
SEMICONDUCTOR SUBSTRATES AND TECHNOLOGY

Over the past four decades, Silicon (Si) has emerged as the predominant technology in power electronics. Currently, silicon-based power transistors and diodes have become an integral part of our daily existence. This widespread acceptance has paved the way for consistent technological advancements and process refinements based on Si, complemented by inventive packaging (PG) and interconnection techniques. These developments have boosted thermal control while reducing unwanted parasite side effects, thereby facilitating operation at higher frequencies. It is worth noting that the relentless strive for improvement is leading the silicon technology to reach a theoretical limit in terms of quality, reliability, and yield of some related products. In this sense, new cutting-edge silicon-based technologies are being developed with critical process issues to be analysed to reduce reliability risk.

Even though silicon maintains its market supremacy, the rise of GaN and SiC, known as wide bandgap semiconductors (WBSs), is poised to steer technology toward novel and highly efficient power solutions. In particular, such new semiconductor materials, thanks to their enhanced electrical properties, allow to overcame several limitations typical of the Si-based technology, being able to sustain even higher specific requirements in terms of voltage, temperature and mechanical stress for specific applications [32]. More in details, WBS-based power electronic components are more efficient and faster with respect to Si-based products [33–35], thus ensuring high life-cycle costs while maintaining reduced size [36,37]. These capabilities encompass the potential for the development of technologies and topologies capable of improving the energy conversion efficiency in both industrial applications and everyday consumer devices.

For a more comprehensive grasp of the possible performance advantages, Table 1 reports the key characteristics of silicon in comparison to SiC (4H polytype) and GaN.

Table 1: *Si, 4H-SiC and GaN main characteristics.*

Property	**Si**	**4H-SiC**	**GaN**
Bandgap E_g (eV)	1.1	3.26	3.45
Dielectric Constant, ε_r	11.9	10.1	9
Breakdown Field, E_c (kV/cm)	300	2200	2000
Electron mobility, μ_n (cm^2/V s)	1500	1000	1250
Hole mobility, μ_p (cm^2/V s)	600	115	850
Thermal Conductivity, λ (W/cm K)	1.5	4.9	1.3
Thermal Expansion ($\times 10^{-6}$)/°K	2.6	4.2	5.6
Saturated E-Drift Velocity V_{sat} ($\times 10^7$ cm/s)	1	2	2.2

In the following sections, two macro technologies of interest for this thesis work will be discussed, namely Bipolar-Cmos-Dmos (BCD) and High electron mobility transistors (HEMTs), based on silicon and GaN, respectively.

2.1 **Si-based technology: Bipolar-Cmos-Dmos (BCD)**

Power devices (PDs) have been studied since the birth of the first bipolar transistor in the late ’40s. PDs are components designed to handle high levels of power through the use of a large number of transistors incorporated within a single device. An example of PD is the Bipolar-Cmos-Dmos (BCD) technology, which includes three different sections that operate simultaneously to ensure the proper device function: a *bipolar transistor* to realize complex analogical functions, a *CMOS transistor* for a fast and good digital switch, and a *DMOS transistor* for the power section (Figure 6). BCD technology has introduced several innovative aspects including the removal of interconnections between different dies that occurred through the package. Such improvement increases the performance thus enhancing the overall reliability of the device. In the last thirty-five years a large number of BCD versions have been

developed, from the first BCD1 characterized by a minimum spacing (MS) of 4 µm, to the BCD10 version with MS equal to 90 nm [38].

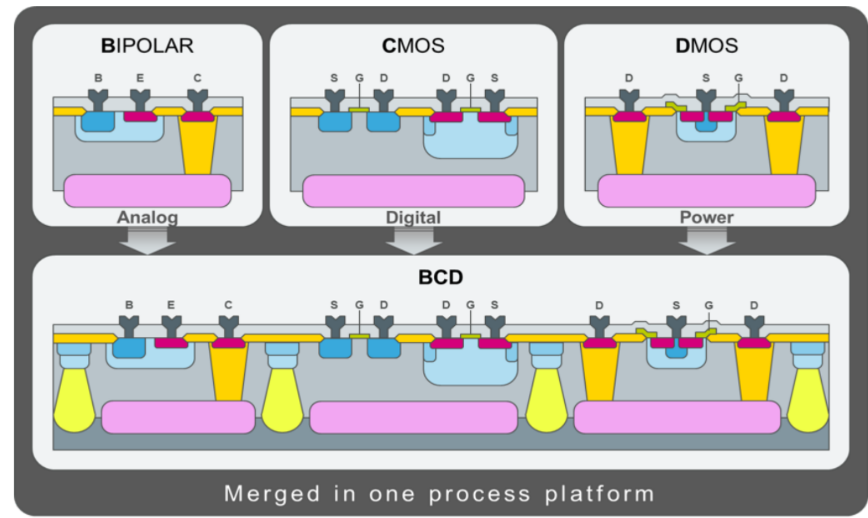


Figure 6: *Schematic representation of BCD technology.*

Thus, when a new BCD product is required, it is possible to design a complex system consisting of CMOS, bipolar transistors, DMOS optimised for low voltage classes (< 40 V), intermediate voltage classes and high voltage classes (> 600 V), passive components such as resistors, capacitors and transformers, and non-volatile memories. The assembly of a BCD device follows a well-defined process flow characterised by several production steps [39]. In particular, process engineers classify such process in two main modules: the *Front End of Line* (FEoL), that includes all the process steps related to the individual component production (i.e. transistors, resistors, capacitors), and the *Back End of Line* (BEoL), that covers the deposition of metal interconnections.

In the case of FEoL, an initial *epitaxy growth* step in order to create a thin and slightly *p*-doped layer is carried out starting from a thick substrate of highly *p*-doped silicon. The substrate doping level ensures good crystal electrical properties while maintaining low substrate resistance, resulting in high electrical stability and low noise. Then, a highly *n*-doped region, named as *buried layer* (BL), is created with the aim to provide the vertical isolation, thus preventing current propagation to or from the substrate when the bipolar transistors are activated. In this way the BL becomes the collector of NPNs parasitic. An additional thin *epitaxial* (EPI) layer is grown above

the BL. Depending on the specific device application, the doping, in terms of impurities (*n* or *p*- type) and depth, can be significantly different. Typically, the lower the working voltages, the thinner and more heavily doped EPI layer are achieved, and vice versa [40].

Considering that in BCD technology the bipolar or CMOS transistors are integrated close to power devices, a good lateral isolation between different die sections, or simply between neighbouring transistors, is of paramount relevance. One of the most innovative techniques to ensure a good latera isolation between the components is called *Deep Trench Isolation* (DTI) (see Figure 7), where the silicon is dug down to the substrate (achieving depths ~20 µm) to form a trench up to ~20 µm deep, then the resulting structure is filled with oxide or polysilicon to realize a substrate contact [41]. This approach offers a number of advantages, including minimised space requirements, no lateral parasitic NPNs and almost absent leakage [42].

For both digital and power sections, the *active area* (AA) of the *integrated circuit* (IC) must be defined for a single or multiple devices depending on the design

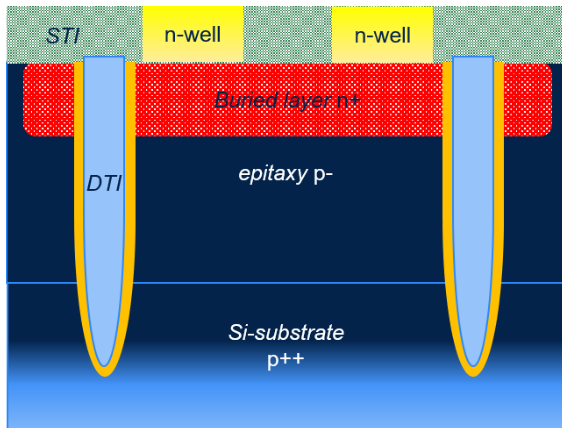


Figure 7: *Representation of both deep (DTI) and shallow (STI) trench isolation for a bipolar transistor, filled with poly and oxide, respectively. Si-substrate p++ doped, epitaxy p, buried layer and n-well region are also shown.*

requirements. In this case, the lateral isolation of AAs is provided by oxide regions that can be realised through local silicon oxidation (LOCOS) or adopting the *Shallow Trench Isolation* (STI) method [43]. Then, a series of *implantation* steps are carried

out in sequence to realize high- and low-voltage (HV and LV, respectively) wells, respectively with high and low thermal budget. The former will be used for LD-MOSFET, *n*-MOS and *p*-MOS, the latter for CMOS. A *polysilicon* layer is deposed after the Gate Oxide (*GATOX),* a dielectric layer separating the gate from the underlying source and drain terminals, growth and etch in order to leave an oxide layer only where needed. The *spacers* structures, that consist of a thin SiO_2 and a thicker Si_3N_4 layers, are used to controls the current flow between drain and source. The last step of the FEoL module involves growing of a *silicide* layer onto the silicon surface, which, thanks to its metal-like behaviour (act as a metal-metal junction), is capable to short-circuiting specific zones where contacts must be made. In addition, *silicide* can also be used to optimise the conduction properties of some poly strips used as conductors. The protection of specific areas from the formation of the *silicide* is guaranteed by the covering of the silicon surface with a patterned oxide/nitride layer commonly called *siprot.*

The BEoL module start with the *Pre-Metal Dielectric* (PMD) deposition and planarization by means of *Chemical-Mechanical Polishing* (CMP) process. The PMD function is to isolate the silicon and polysilicon from the metal that will be deposited subsequently. PMD and metal are placed in communication by means of *contacts* which are sputtered with a thin *barrier* layer and filled with *tungsten* (W). In order to achieve the proper W flatness, a CMP process is also required. The Aluminium (Al) deposition and etch is needed to complete the first *metallisation*. The same process is repeated twice, by replacing the PMD oxide with *Inter-Metal Dielectric* (IMD), and replacing the contacts with the *vias*. The metallic lines described above are thin lines dedicated to fast digital operations, while the top metallisation is much thicker and involves the application of the *damascene* process [44] that uses copper instead of aluminium. This process, designed for power operations, guarantees better electrical performance in terms of lower resistance, excellent robustness to thermal stresses and electromigration.

2.1.1 *Metal-oxide-metal (MOM) capacitors*

In this thesis, the thermal characterization of a specific component named as Metal-Oxide-Metal (MOM), belonging to the BEoL module of the BCD8 family (the "8"

number indicates the technology's specific version) and characterised by a MS equal to 160 nm, will be addressed.

Nowadays, analogue integrated circuits (AICs) employ three different types of capacitors based on MOS (p-n junction), MIM (metal-insulator-metal) and MOM (metal-oxide-metal) structures. Although characterized by high capacitance density per unit area, MOS junctions are not suitable for all ICs applications, due to their low breakdown voltage and non-linear response. Hence, many efforts have been devoted to the optimization of MOM and MIM structures, with the aim to overcome the aforementioned MOS issues [45,46]. However, due to lower production costs and higher capacitance density with respect to MIM components, MOM capacitors became popular for the manufacturing of power semiconductor devices. In this work we report the state-of-art about MOM capacitors, together with a description of some of their known applications in Bipolar-Cmos-Dmos (BCD) technology. MOM capacitor consists of multiple lateral capacitive units made up of metal layers (MT) separated from each other by oxide layers (OL). Each MTs are put in contact through tungsten vias, forming the so-called strips (see Figure 8).

The lateral intra-layer coupling furnishes better matching properties than vertical geometries, thanks to the enhanced processing control of lateral dimensions. In order to optimize the capacitance per unit area, a minimum spacing between each conductive layer must be achieved. In this sense, different types of MOM architectures have been developed (parallel stacked wires, interdigitated parallel wires, woven and vertical bars MOMs, see Figure 9 for details) in order to obtain high capacitance density (up to ~2 $fF/\mu m^2$) and low parasitic capacitance with a moderately low production cost [47,48].

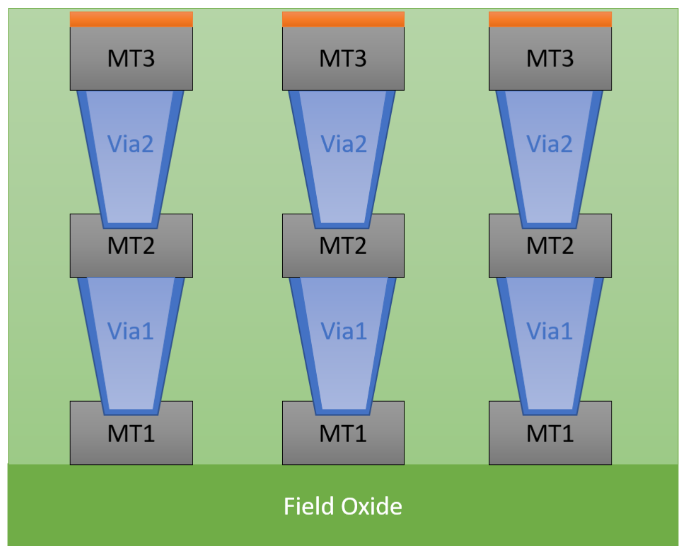


Figure 8: *Frontal view of a MOM capacitor. Dark grey boxes (MT1, MT2,...) account for metal layers separated from each other by oxide layers (green area). Metal layers are contacted by means of tungsten vias (Via1, Via2,...).*

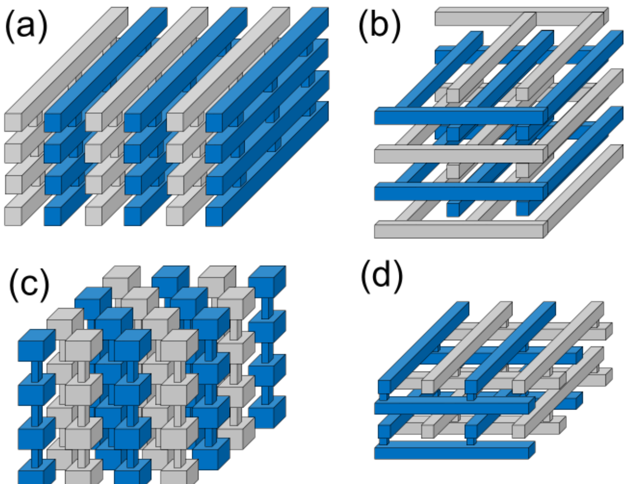


Figure 9: *Schematic representation of the parallel stacked wires (a), interdigitated parallel wires (b), woven (c) and vertical bars (d) MOM architecture. Blue and grey strips account for positive and negative conductors, respectively.*

In the emerging field of ICs, MOM structures represent a fundamental building-block for the engineering of devices built on silicon substrates. However, because of their extremely small size, the presence of defects included during a specific step of the production flow can lead to electric failures. Generally, although most of them can be properly screened through electrical wafer sorting (EWS) and burn in (BI), some of

these elude such standard electrical tests, causing unwanted reliability failures. In this framework, the development of novel approaches (based on electrical, optical, and spectroscopic techniques) able to properly detect the presence of impurities such us metal flakes, polymeric residues and structural inhomogeneities, represents a key point for the enhancing of the final de vice reliability.

2.1.2 *Si-based material applications*

Silicon-based devices have been part of our society for decades and have achieved very high levels of performance considering the theoretical limits of the material. Even if to date they represent the building blocks of modern electronics, thanks to their versatility and reliability, they are used for a wide range of electronic, communication, automotive, manufacturing, healthcare, aerospace, renewable energy and power electronics applications, including:

- Microprocessors for PCs, smartphones and tablets;
- Telecommunication equipment such as routers, switches and base station;
- Sensors for touchscreen, accelerometers and gyroscopes in mobile device;
- Chips for TVs, gaming consoles, audio equipment;
- Microcontrollers and sensors for automotive vehicle control and safety systems (i.e. airbags and ABS);
- Microcontrollers for convolutional neural network (CNC) machine;
- Advanced Driver Assistance Systems (ADAS) for radar, lidar and camera sensors;
- Radar systems;
- Sensors and control systems for automation, robotics and process control;
- Inverters and energy storage systems in renewable energy application;
- Solar cells for photovoltaic energy used to convert sunlight into solar panels;
- Power devices in power electronics for motor drives, inverter, and power distribution systems.

In particular, this is supported by the continuous development of diodes, thyristors, IGBTs, MOSFETs, BCD and other devices that can handle high voltages and currents in power conversion, transmission, distribution, and control systems. As well as is used

to make bipolar junction transistors (BJTs) and metal-oxide-semiconductor field-effect transistors (MOSFETs), which can amplify or switch electrical signals in various circuits and systems.

2.2 **Gallium nitride (GaN)-based technology**

In the last thirty years, gallium nitride (GaN) is emerging as the latest breakthrough in the development of novel energy-efficient power electronic devices and optoelectronic components. In fact, it allows the achievement of better efficiency/performances of the resulting electronic device while maintaining reduced power consumption [49], thus boosting the overall nitride-based device market with respect to that related to other semiconductors.

The development of such substrates met serious challenges mainly originating from the intrinsic difficulty to grown and process nitrides. The first polycrystalline GaN material was produced in 1932 by flowing, at high temperature, ammonia (NH_3) over liquid gallium (Ga) [50]. The crystal structure of the resulting material was first investigated in 1938 on GaN powders [51]. Between 1969 and 1971, Maruska and Tietjen [52] employed hydride vapor-phase epitaxy (HVPE) on sapphire substrates to grow thin GaN layers, which, however, exhibited poor crystallographic quality due to a significant reticular mismatch existing between the used initial materials. Despite such unfavourable condition, the aforementioned GaN layers permitted the quantification of the energy band gap, equal to 3.39 eV (direct gap) [53]. After that, a forward step was undertaken by Manasevit *et al.* [54,55] in 1972, with the development of the first metal–organic vapor-phase epitaxy (MOVPE) GaN layers, providing one of the most popular synthetization methods utilized till today in nitride technology. These layers appeared still opaque and rough, with a high percentage of crystallographic defects mainly originating from the sapphire/GaN lattice mismatch. In 1986, Hiroshi Amano achieved a significant milestone in GaN epitaxy by pioneering the use of a low-temperature AlN nucleation layer [56], paving the way for Amano and Akasaki to produce GaN materials with remarkable smoothness and transparency, as well as with excellent crystallographic properties.

The employment of MOVPE allowed Asif Khan et al. [57] to develop the first Aluminium Gallium Nitride/Gallium Nitride (AlGaN/GaN) heterojunction, characterized by a mobility of the two-dimensional electron gas (2DEG) at the AlGaN/GaN interface of 600 $cm^2/V \cdot s$. Such innovation can be considered as the beginning of the nitride high electron mobility transistor (HEMTs) technology [58]. The analytical model used to describe the 2DEG features in AlGaN/GaN heterojunction was first introduced by Ambacher *et al.* [59] in 1999, and is today widely accepted by the scientific community working in the field, although the nature of the 2DEG was properly clarified by Ibbetson *et al.* [60], attributing to the surface states present in nitride materials the primary source of electrons.

More recently, thanks to the harvesting of innovative device scaling technologies [61], high-frequency (HF) performances of GaN-based HEMTs, with ultrahigh cut-off frequency > 450 GHz, were achieved, while recessed gate Al_2O_3/AlGaN/GaN HEMTs with high threshold and blocking voltage (2.4 V and 825 V, respectively) and reduced leakage current, were verified on 200 mm silicon substrates [62]. In 2015 *Transphorm* [63] first released the first high-voltage (600 V) normally-off GaN HEMT solution, working in "*cascode*" configuration [64].

The exceptional characteristics of nitride-based devices must be attributed to the unique nitride microstructure, including its main crystallographic form and high built-in electric fields.

In particular, GaN possess a crystallographic arrangement typical of wurtzite, which consists of Gallium (Ga) and Nitrogen (N) atoms spatially arranged to form a superimposed hexagonal packed lattice (Figure 10).

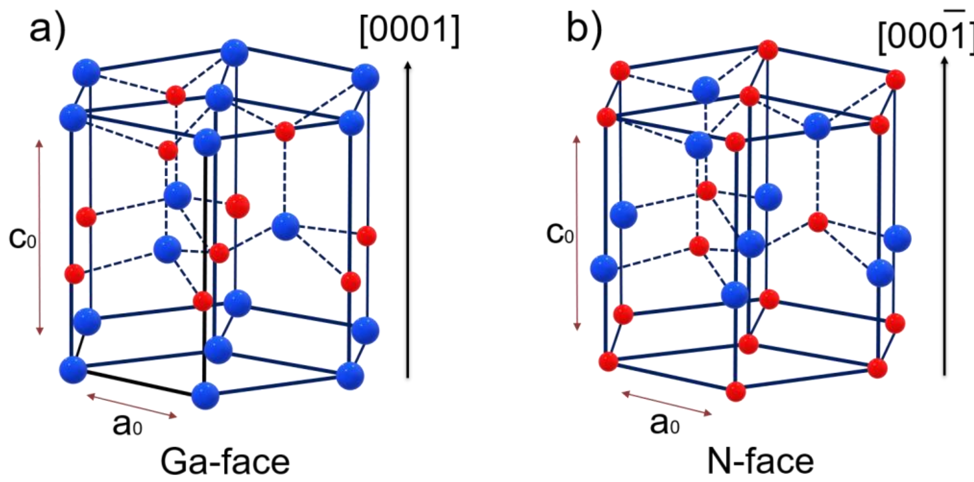


Figure 10: *Representation of a typical GaN crystal structure (wurtzite), with the blue and red dots representing Ga and N atoms, respectively. Detail of the structure as seen from the Ga-face (a) and N-face (b). The unit cell is depicted using solid lines, whereas the Ga-N bonds are represented by dashed lines. In particular, the Ga-face easily incorporates acceptors and is more chemically inert than the N-face, which, instead, easily incorporates donors. Ga atoms are tetrahedrally covalent bonded with four surrounding N atoms of the lattice, although the ionic contribution, due to the remarkable difference in electronegativity between the Ga and N atoms, plays also a key role in the formation of the structure. Taking into account all these forces, the lattice parameters of the GaN hexagonal structure turns out to be 5.18Å (c_0) and 3.19Å (a_0).*

Such spatial atom distribution has no inversion symmetry in the [0001] direction [65], which means that two different types of orientation in GaN crystals can be distinguished, namely the Ga-face (Figure 10a) and the N-face (Figure 10b), each characterized by different chemical properties [66–68].

In the field of power electronic and optoelectronic devices based on GaN technology, the increasing demand for the next generation of high-efficiency power converters led to the development of AlGaN/GaN high electron mobility transistors (HEMTs) [69,70], capable of operating at high temperatures, frequencies, voltages, and currents, hence appropriate for power conversion applications in electric vehicles, phone chargers, renewable energies [71], and so on. However, due to the limited commercial availability of bulk-GaN substrates [72], GaN-based electronics are

typically developed through the employment of mismatched substrates, such as sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si) [73]. In the case of Al_2O_3 and SiC, high number of crystallographic defects are introduced within the GaN crystal lattice during the epitaxy process [74]. This aspect, together with the high costs and possibility to produce only small-sized wafers, led to a massive use of Si-based substrates in the electronic industrial production.

2.2.1 *Electrical Properties*

GaN is a wide bandgap material characterized by a value of E_g = 3.4 eV, which provides a high critical electric field (E_c) ranging from 3 to 3.75 MV/cm. Such high E_c values turn out to be extremely useful in the view of the realization of high efficiency electronic devices, based on GaN substrates, operating under high voltages.

The influence of temperature must always be taken into account as it has a strong impact on the carrier generation. In fact, even if intentional doping agents are absent, all semiconductors possess a given amount of intrinsic thermal carriers n_i within the crystal whose behaviour, as a function of temperature, follows the exponential trend reported in Eqn. 10. In Figure 11, the calculated n_i trend as a function of the inverse of T in GaN and Si, adapted from [75,76], is reported for comparison.

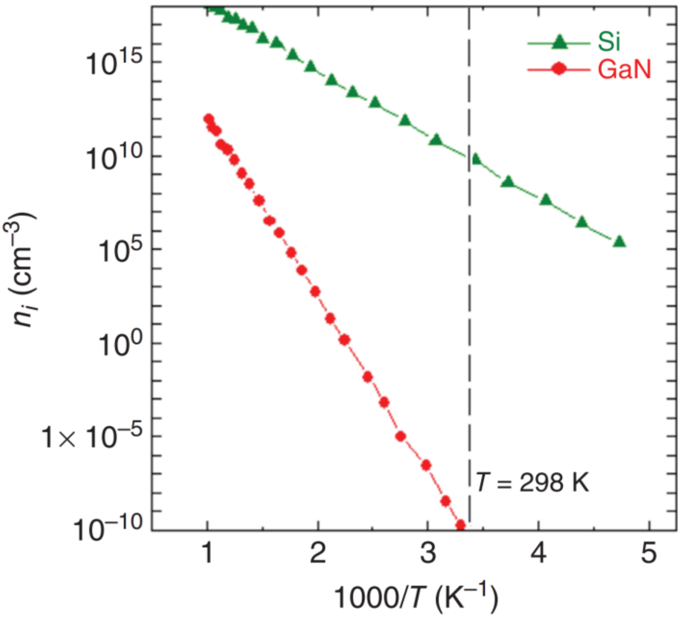


Figure 11: *Calculated* $\mathbf{n_i}$ *as a function of reverse of the temperature (1000/T) for GaN and Si. The dashed line indicates the room temperature (T = 298 K).*

As can be noted, the intrinsic carrier concentration in GaN at room temperature is about 19 orders of magnitude lower with respect to that of Si. This means that GaN electronic devices should theoretically exhibit lower leakage current, thus permitting their functioning upon high temperature operating conditions (in the case of perfect GaN crystals). However, the presence of the GaN/substrate reticular mismatch, in conjunction with the existence of dislocation defects within the structure, offers preferential leakage routes which negatively affect the optimal electrical performance of the resulting device.

Based on the work of [77,78], Figure 12 reports the comparison of the calculated electron velocity *vs.* the applied electrical field for GaN and Si semiconductors, as example.

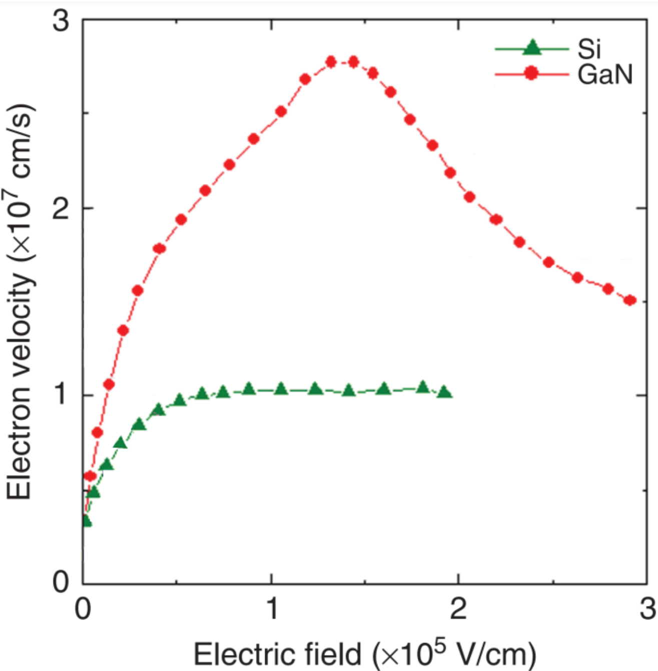


Figure 12: *Calculated electron velocity vs. applied electric field in GaN and Si semiconductors.*

An inspection of the figure reveals, in the case of GaN, a maximum and a saturation electron velocity higher with respect to those exhibited by Si, with values around 3×10^7 cm/s and 1.5×10^7 cm/s, respectively. In particular, the high saturation velocity experienced by carriers leads to a diminishing of the transit time characteristic of all

GaN-based power devices, which allow them to sustain remarkable high-frequency operation cycles.

Finally, also the defect density shows a tangible impact on the thermal conductivity of GaN-based materials, which were found to varies between 1.3 and 2.1 W/cm ·K. Such values are considerably lower with respect to those exhibited, for example, by SiC, and for this reason much attention must be paid in using GaN devices for applications involving high temperature stresses.

Based on all the aforementioned properties, GaN-based devices offers significant advantages in terms of high-voltage, high-frequency, and high-temperature operation. The electron properties of GaN are summarized in the radar chart reported in Figure 13, in comparison with those of Si.

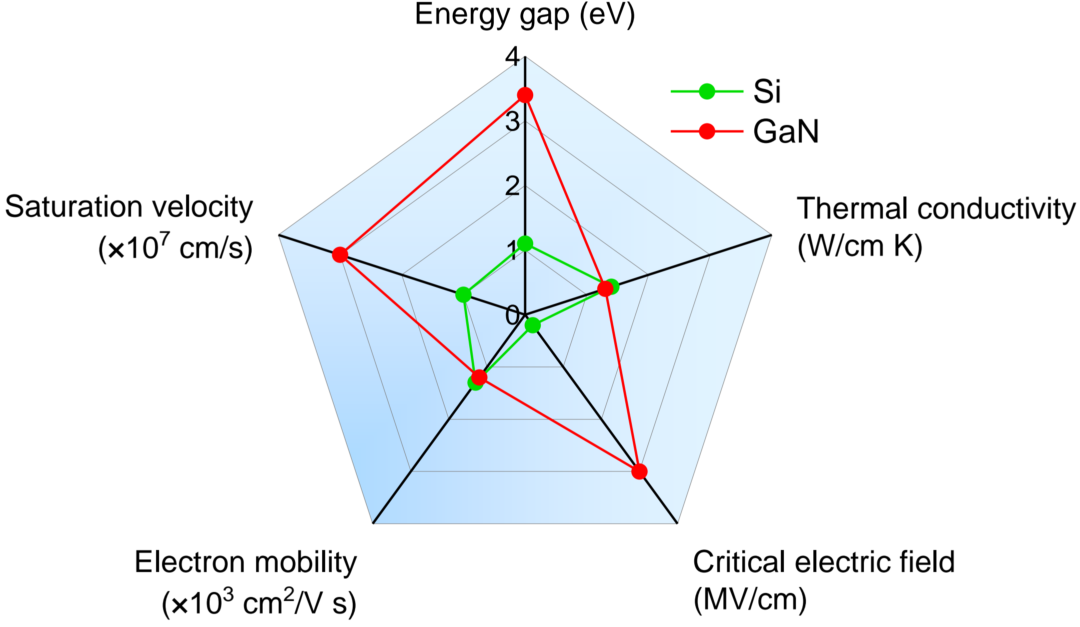


Figure 13: *"Radar chart" of physical and electronic properties of GaN compared with those of Si.*

2.2.2 *GaN-based High electron mobility transistors (HEMTs)*

The High electron mobility transistor (HEMT) is a device whose working principle is based on the presence of the two-dimensional electron gas (2DEG) in AlGaN/GaN heterostructures. A 3D schematic cross-sectional illustration of an AlGaN/GaN HEMT is reported in Figure 14.

In conventional AlGaN/GaN HEMT, the current that moves within the 2DEG channel, connects the source and the drain ohmic contacts and experiences modulation when a negative bias is applied to a Schottky contact, which acts as the gate electrode of the transistor. It is worth noting that the channel carriers have very high mobility, and this allows the devices to work at very high frequencies.

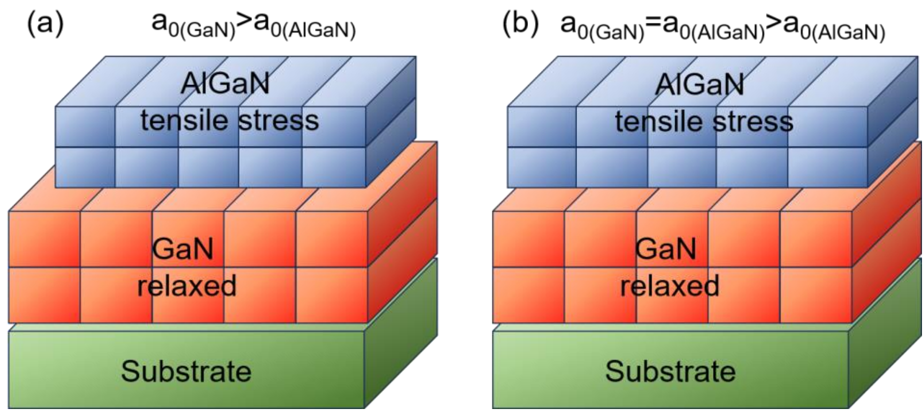


Figure 14: *Representation of isolated AlGan and GaN crystals (a); heterostructure formed by AlGaN/GaN (b) where the compensation of lattice mismatch between the two materials is visible.*

Typically, AlGaN/GaN heterostructures can be produced by growing a thin layer of $Al_xGa_{1-x}N$ onto a GaN substrate towards a specify crystallographic direction, namely the [0001]. The difference in the energy gap between $Al_xGa_{1-x}N$ and GaN provides an energy discontinuity visible in the corresponding band diagram. Moreover, the significant lattice mismatch between $Al_xGa_{1-x}N$ and GaN ($a_0^{GaN}>a_0^{AlGaN}$) originates tensile strain along the $Al_xGa_{1-x}N$ layer, which tends to reduce the in-plane reticular mismatch (see Figure 14).

In a strained AlGaN/GaN heterostructure, a not-negligible *piezoelectric polarization* $\mathbf{P}_{PE}$ develop pointing towards the c-axis direction [59] given by:

$$P_{PE} = e_{33}\varepsilon_z + e_{31}\left(\varepsilon_x + \varepsilon_y\right), \quad (23)$$

with e_{33} and e_{31} the piezoelectric coefficients, ε_z the strain along the c-axis and ε_x = ε_y = are the in-plane strains (in an isotropic condition). It can be demonstrated that

$\mathbf{P}_{PE}$ will be positive or negative for *compressive* ($a^{AlGaN} > a_0^{AlGaN}$) and *tensile* ($a^{AlGaN} < a_0^{AlGaN}$) strain, respectively [59]. Accordingly, considering the Ga-plane of a AlGaN/GaN heterojunction, upon the application of a tensile strain onto the AlGaN layer $\mathbf{P}_{PE}$ will be negative and directed towards the GaN substrate, thus parallel to *the spontaneous polarization* $\mathbf{P}_{SP}$.

A polarization gradient at the $Al_xGa_{1-x}N$ and GaN interface induces the onset of a charge density whose extent varies according to the concentration of Al through the following relation:

$$|\sigma(x)| = |P_{SP}(Al_xGa_{1-x}N) + P_{PE}(Al_xGa_{1-x}N) - P_{SP}(GaN)|, \qquad (24)$$

Hence, to guarantee the charge neutrality within the structure, free electrons will spontaneously tend to originate a two-dimensional electron gas which compensate the $|\sigma(x)|$ at the AlGaN/GaN interface. Such electron gas, *i.e.* 2DEG, yields to a potential well insisting along the AlGaN/GaN interface and can be regarded as an electron transfer process occurring between donor-rich surface state and lower energy empty states of GaN.

Since in real devices the surface is not free, deviation from the theoretical predictions can be observed. In fact, a Schottky electrode is typically shaped at the AlGaN surface, which thank to the application of a bias allows the modulation of the sheet carrier density existing within the 2DEG. More in details, the maximum sheet carrier density $n_s(x)$ of the 2DEG, in presence of a Schottky electrode can be written as:

$$n_s(x) = \frac{\sigma(x)}{q} - \left[\frac{\varepsilon_0 \varepsilon_{AlGaN}(x)}{d_{AlGaN} q^2}\right] \cdot [q\Phi_B(x) + E_F(x) - \Delta E_C(x)], \qquad (25)$$

With d_{AlGaN}, $\varepsilon_{AlGaN}(x)$, $q\Phi_B$, E_F and ΔE_C equal to the $Al_xGa_{1-x}N$ barrier thickness, $Al_xGa_{1-x}N$ permittivity, Schottky barrier height, Fermi level position calculated with respect to the GaN conduction band edge energy and AlGaN/GaN interface conduction band offset (see Figure 15).

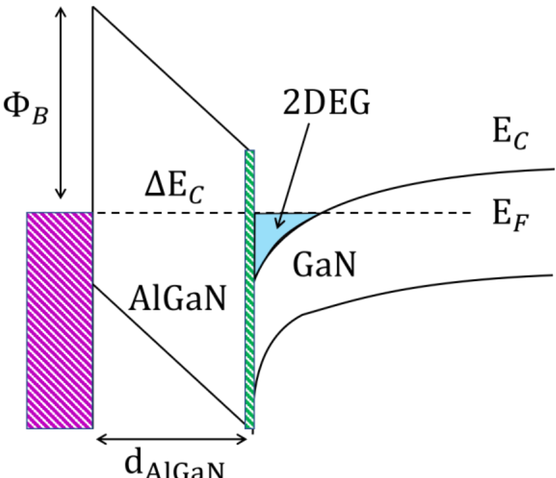


Figure 15: *Band diagram of an AlGaN/GaN heterostructure. [Source:* [79]*].*

Considering that the Fermi level is located above the conduction band at the interface, a current flow between source and drain can be measured even if the gate bias is set to 0. For this reason, AlGAN/GaN HEMTs are considered as "normally-on" devices. Typical values of d_{AlGaN} are 20 – 25 nm, which yield to 2DEG sheet carrier density at the AlGaN/GaN interface of 0.7 – 1 $\times 10^{13}$ per square centimetre.

It is worth of note that for power electronic applications, "normally-off" HEMTs are strongly demanded. Also, the employment of Schottky metal acting as a gate electrode can induce to high leakage current thus representing a limitation in terms of off-state characteristic. To overcome such issue, the addition of an insulator layer lying below the gate represents a widely-accepted solution in GaN-based HEMT technology, often called metal–insulator–semiconductor high-electron mobility transistors (MISHEMTs).

2.2.3 *GaN-based material applications*

Due to their unique properties and versatility, GaN-based semiconductors have found extensive applications in a wide range of industries. This section provides an overview of the main applications of the GaN-based material in the field of power electronics, taking into account the most relevant physical and technological open issues. Up to now, silicon (Si) has been the most popular semiconductor for PD due to its natural abundance, low cost and excellent crystalline quality reaching its

operational limits linked to its intrinsic properties. Specifically, a significant power dissipation in Si-base practical applications must to be overcome in order to reduce global energy consumption. This challenge is entrusted to the new semiconductor substrates, among them, GaN and related alloys are very promising although they still suffer from a lot of problems.

The potential applications of GaN devices compared with another WBG semiconductors, *i.e.* silicon carbide (SiC), are shown in Figure 16.

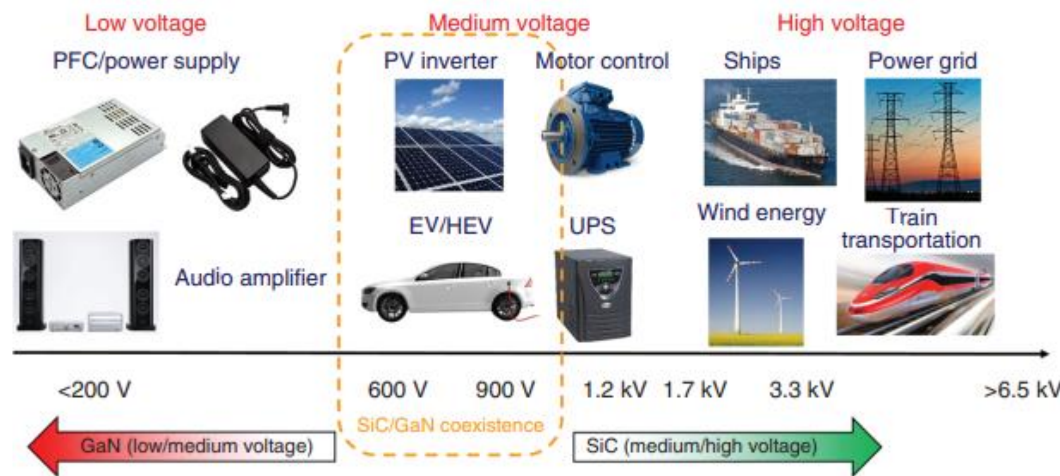


Figure 16:*Potential application of GaN power device as a function of Voltage. The application area of SiC is also indicated. [Source:* [80]*].*

In particular, devices operating in the low-medium voltage range, i.e. 200-600V, have a broad field of applications ranging from audio amplifiers to PC power supplies, and could replace existing Si-based devices. Furthermore, the development of devices operating in the medium voltage range, *i.e.* 600-900 V, would lead to an overlap with SiC-based technology, in fact, the upcoming GaN-based devices would be used as converters for electric vehicles (EVs) and hybrid electric vehicles (HEV), as well as inverters for renewable energies such as photovoltaics. For industrial applications, such as power distribution networks or heavy transport, voltages >1.2kV are required. GaN technology is not yet mature for this type of application since the substrate quality and device reliability are not sufficient enough to guarantee good performances. For the aforementioned applications, devices grown on 4H-SiC substrates are much more robust in terms of performance and reliability due to the fact that their development has drastically accelerated over the last decade.

Considering the on-resistance R_{ON} of a unipolar power device, the following relationship can be written:

$$R_{ON} \cong \frac{4B_V^2}{\varepsilon_0 \varepsilon_{GaN} \mu_n E_{CR}^3}, \quad (26)$$

where, R_{ON} is expressed in $\Omega{\cdot}cm^2$, B_V is the breakdown voltage, ε_{GaN} is the GaN permittivity, μ_n is the electron mobility and E_{CR} is the material's critical electric field.

Typically, power devices, such as diodes, consist of a heavily *n-* doped anode and cathode and a weakly *p+* doped *drift layer*. The width of the drift layer determines the breakdown voltage of the diode. From Eqn. 26, it can be deduced that the size of the drift layer can be compensated with a high electric field E_{CR} that allows to support high breakdown voltages while maintaining thin drift layers. By reducing this value, the R_{ON} of the device is also reduced, therefore it is possible to obtain devices with lower thermal dissipation and better energy efficiency.

As mentioned in the previous section, a key element for the optimization of these devices consists of the metal/semiconductor contacts. Considering the GaN-based HEMTs, the aim is to create, on the one hand, ohmic contacts with a low specific contact resistance ρ_c (in the range between 10^{-4} and 10^{-6} $\Omega{\cdot}cm^2$), and on the other hand, Schottky contacts with an correct barrier while maintaining low leakage [81]. The aforementioned characteristics are difficult to be obtained and different metallization schemes have been proposed, among which, the sequence of titanium (Ti), deposited on GaN, with low work function, aluminium (Al), barrier layer inserted to limit the interdiffusion between metals during annealing (Ni, Ti, Pt, Pd, Mo, etc.) and gold (Au) top cap layer in order to prevent oxidation, is the widely used protocol.

In the case of p-type GaN in Ohmic contacts, Ni, Pt and Pd elements are preferred because they are expected to form a low Schottky barrier on the p-type semiconductor. Meanwhile, from a production point of view, the use of Au for the growth of the top cap is incompatible with the standards of the Si-based line since this element is a contaminant.

To ensure the compatibility of Gan technology with current silicon production, the development of Au-free metallization schemes becomes mandatory. In the context of

GaN HEMTs, Schottly contacts are used as gate metallization to modulate the 2DEG concentration where Ni, Pt and Au are the prevailing choices among metals. Due to the non-ideal behaviour of Schottky barriers on (Al)GaN, it is necessary to use dielectric materials to isolate the gate and reduce the leakage current. In addition, the dielectric layer (SiN_x, SiO_2, Al_2O_3, etc.) [82,83] plays a critical role in surface passivation, preventing the trapping of electrons at the device surface/buffer (phenomena known as "current collapse"), which is widespread in GaN HEMTs [84–86]. It is worth noting that the GaN electronics predominantly relied on lateral transistors accomplished from AlGaN/Gan heterostructures raised on foreign substrate. However, the quest for improved performance in power electronics has led to the search for vertical devices based on bulk GaN. This vertical configuration offers a fundamental advantage, which is the increased breakdown voltage achieved by increasing the thickness of the drift region while maintaining the same chip size. Furthermore, the strategic positioning of the maximum electric field deeper in the bulk in vertical GaN devices effectively mitigates trapping phenomena and eradicates the risk of current collapse. Vertical devices engineered from high-quality bulk GaN crystals exhibit a higher power density attributable to their lower on-resistance (R_{ON}), increased current-carrying capacity, and the superior thermal conductivity intrinsic to bulk material.

CHAPTER 3
QUALITY AND RELIABILITY ISSUES OF SEMICONDUCTOR DEVICES

3.1 **Introduction**

Semiconductor devices are the fundamental building block for the modern electronic objects. Nowadays, ever-smaller size and ever-increasing computing power are continuously demanded while maintaining high standard of quality and reliability.

Quality is typically defined as the reduction of variability around a target in order to achieve customer requirements and expectations. More specifically, referring to electronic components, it accounts for the probability that a given device will perform a specific function under defined conditions for a determined period.

On the other side, reliability is defined as the ability of a device to conform to its electrical specifications over a specified period of time under specified conditions at a specified confidence level [87], and it is a measure of the probability that a given component does not exhibit deviation from the behaviour described in the specification over a given period of time. Figure 17 reports the failure rate, measured in defects per million (DPM) or parts per million (PPM), of an electronic component as a function of time. An inspection of the Figure 17 revealed the existence of three domains characterized by different failure classes, namely *infant, random* and *wear out* failures. In particular, *infant* failures originate from the presence of defects within the device, such as contaminant particles, crystallographic defects, film oxide integrity, static electricity, due to the manufacturing process, and typically occurs in the very first phase of the device's operational life. The second region describes a constant failure rate due to *random* failures which has a constant level over time, while the last region describes the failure rate which occurs due to the inherent lifetime of the device due to wear and fatigue, such as mechanical and thermal stresses, induced corrosion, age, etc... This contribution increase moving towards the maximum limit of stresses that

can be sustained by each component. Therefore, the failure rate can be represented as the mixture of three curves (shown in Figure 17) resulting in the so-called *bathtub curve*, which shows a low failure rate due to wear in the initial phases of the device's life, which proportionally increase with age.

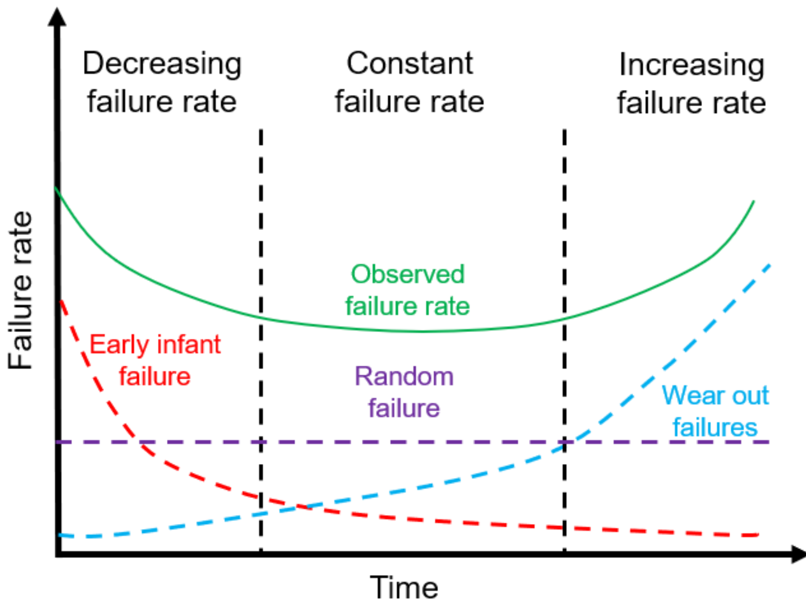


Figure 17: *Bathtub curve representing the device failure rate as a function of time.*

The improvement of the semiconductor reliability, together with the even increasing number of stressed samples, is leading to an easier and faster detection of electrical issues yet in the early stages of device life.

Generally, one of the weakest aspects of modern energy-efficient architectures is related to the reliability of power electronic components [88–90], and, in order to be able to estimate the time-to-failure associated with wear mechanisms, deterministic models calibrated with data extracted from accelerated ageing cycle experiments must be taken into account. The lifetime of semiconductor devices is strongly related to the existence of thermomechanical failure mechanisms naturally originating upon normal operation cycles. The understanding of failure mechanisms is the first prerequisite to formulate the time-to-failure relationship and, therefore, be able to predict the operating state of the device.

In the early failure period, the number of defects or failures against the total number of samples, irrespective of the time parameter, is generally expressed in (%) or ppm.

In the random failure period, it is necessary to consider the time parameter as well as the reliability, unreliability, probability density and conditional failure rate functions. The reliability function (*R(t)*) is the proportion of components (devices, parts, and elements) which keep performing their designed functions normally after time (t). This can be expressed by the equation:

$$R(t) = \frac{n - c(t)}{n}, \qquad (27)$$

with *n* equal to the total number of tested components, and *c(t)* the total number of failures to develop up to time (*t*). On the other side, the unreliability function (*F(t)*), also known as the cumulative failure distribution function, is defined as the distribution function when the failure time is considered as the probability function, equal to the total number of failures (the cumulative number of failures) which lose their designed functions after any particular device, part, or component is being used for a period of time expressed as "*t*".

$$F(t) = \frac{c(t)}{n}, \qquad (28)$$

With $R(t) + F(t) = 1$ (see Figure 18).

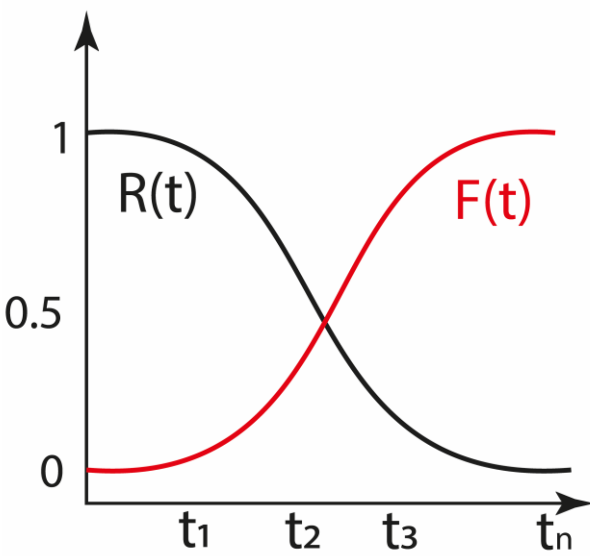


Figure 18: *Relation of R(t) and F(t).*

Another criterium widely used in the reliability assessment is the probability density function (*f(t)*), defined as the probability of failure of a particular device or component after being used for a period of time (t):

$$f(t) = \frac{dF(t)}{dt} = -\frac{dR(t)}{dt}. \tag{29}$$

From the equation above, both $F(t)$ and $R(t)$ can be calculated by taking the integral of the *f(t)* (see Figure 19), as:

$$F(t) = \int_0^t f(t)dt\,; \tag{30}$$

$$R(t) = 1 - F(t) = 1 - \int_0^t f(t)dt = \int_t^\infty f(t)dt. \tag{31}$$

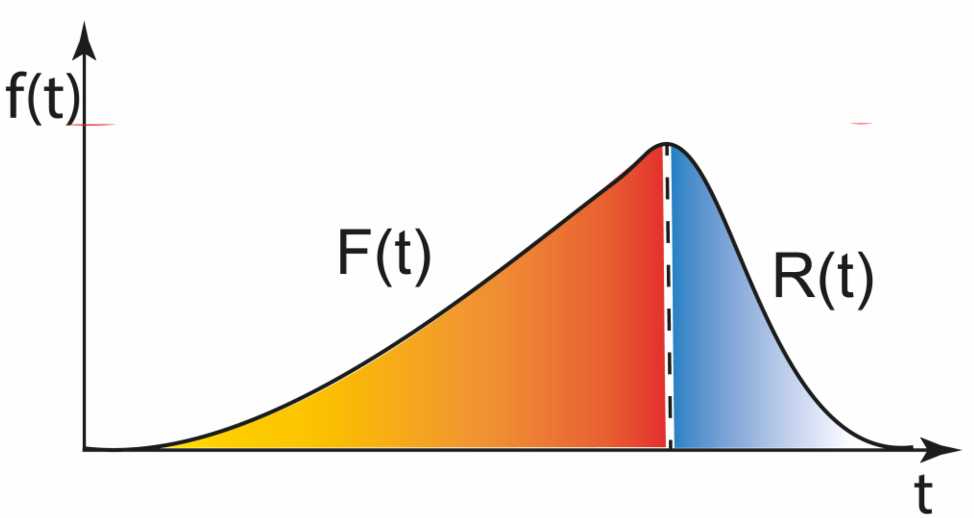


Figure 19: *Schematic of f(t), R(t), F(t).*

Going on, the *failure rate function* (λ(t)), also known as *hazard function*, accounts for the rate of failures over time, with respect to all device running for longer than the defined time. Such function can be express as:

$$\lambda(t) = \frac{f(t)}{R(t)}. \tag{32}$$

It is wort of note that the behaviour of λ(t) is often used to achieved information about the reliability of semiconductor devices and other components. However, despite the instant values of λ(t) are theoretically very accurate, it is practically impossible to quantify at a point of time in a short period. Hence, a period of time of 1000 hours, one month or one year, is usually considered for the assessment of the mean failure rate, defined as:

Mean failure rate = Total failures in the period / Total operating time in the period

Its values are expressed in unit of % per 1000 hours or ppm/1000 hours. The more common term Failure in Time (FIT) is widely used as a unit to express the failure rate:

1 FIT = 1 x 10^{-9} 1/h = 1 ppm/1000 h

Number of failures / (actual number of devices tested x actual operation time)

It is worth underline that the total operating hours are not obtained by focusing on one single component. In fact, for a failure in time value of 100, the probability that a failure occurs in an operating time period of 10^7 h become 1 (100%).

Finally, The Reliability Function R(t) and Failure Rate Function λ(t) can be determined by expanding (32) from equation (29) to produce the following relation shown in equation (33).

$$R(t) = \exp\left(-\int_0^t \lambda(t)dt\right) \tag{33}$$

Further if the cumulative hazard function H(t) is defined as:

$$H(t) = -\int_0^t \lambda(t)dt \tag{34}$$

Where the λ(t) expresses a Weibull distribution; the following relation holds:

$$R(t) = \exp\left(-\frac{t}{\eta}\right)^{m} \tag{35}$$

Therefore,

$$H(t) = \left(\frac{t}{\eta}\right)^{m} \tag{36}$$

Further

$$R(t) = \exp[-H(t)]. \tag{37}$$

Generally, semiconductor devices cannot be repaired, maintained, and reused once a component fails. Therefore, they can be referred to as non-repairable (non-maintainable) products. The average time for non-repairable components (devices, parts, elements) to fail is defined as the Mean Time to Failure (MTTF) and can be expressed by the equation:

$$MTTF = \frac{1}{\lambda(t)}\,. \tag{38}$$

It is important to underline that both λ(t) and MTTF are time-dependent functions which can be used to describe the life expectancy and working conditions of the investigated device.

In Figure 20, reports the changes in the semiconductor failure rate results in a bathtub curve. At the start of device operation, there may be semiconductors with latent defects included in the set. These will fail under operating stress and are removed from the set.

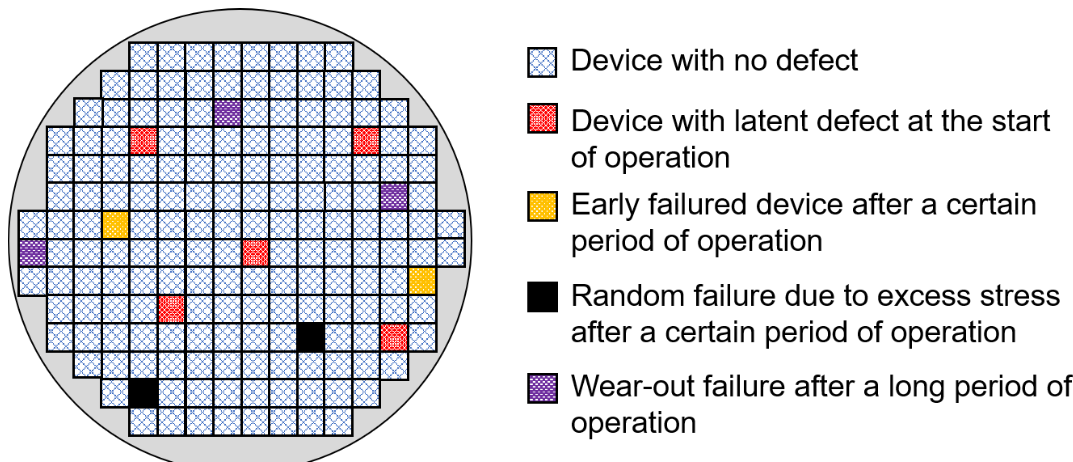


Figure 20: *Image shows the resulting good dice excluding early and wear-out failures described in the Bathtub Curve.*

In the integrated circuit (IC) industry, power semiconductor devices are the most vulnerable components of the whole IC, with almost 31% of respondents, as shown in Figure 21. The harsh environmental and thermal operating conditions can potentially trigger die and package-related degradation in power semiconductor devices [91,92], of which 60% of failures are caused by thermal stress [78]. Within the working temperature range of power semiconductor devices, temperature jumps of 10 °C yield to a doubling of the failure probability [93], mainly attributed to the dissimilar coefficients of thermal expansion of the different layers used to realize the dice and packaging of the PD.

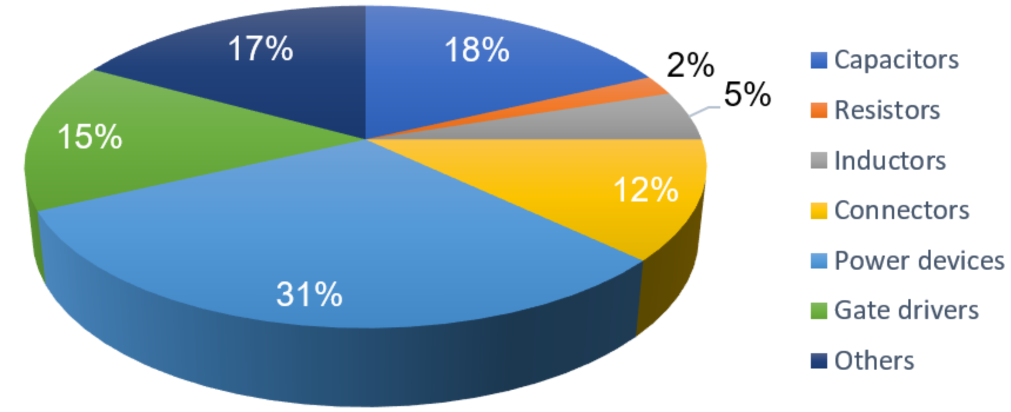


Figure 21: *Survey of fragile components in an IC.*

3.2 **Electrical Analysis**

In semiconductor technology, ensuring the reliability and functionality of semiconductor devices is of paramount relevance. Reliability testing consists of a series of laboratory tests carried out under known stress conditions to evaluate the lifetime of a device or system. Reliability tests are performed to ensure that semiconductor devices maintain the performance and functions throughout their life. These reliability tests, as reported in Table 2, aim to simulate or accelerate by the stresses that the semiconductor device may encounter during all phases of its life, including mounting, aging, field installation and operation. The typical stress conditions are defined in the testing procedure described later in this document. Reliability tests are performed at various stages from development to mass-production. The purpose and contents differ in each stage.

Table 2: *Examples of reliability testing conduced when new products are developed.*

Phase	Purpose	Contents
Development of new device	To verify that the reliability target and the customer's reliability requirements are satisfied.	The following and other tests are carried out as required: **1.** Accelerated tests **2**. Marginal checks **3**. Physical structural analysis
Development or change of design, processes and materials	To verify that the reliability target and the customer's reliability requirements are satisfied regarding the materials and processes. To understand the quality characteristics and limits as influenced by materials and processes.	Test Elements Group (TEGs) (used to evaluate the structural elements of the semiconductor device) or products are used to perform acceleration tests and other analyses as required with focusing on the characteristics and changes of materials and processes.
Trial run before mass production	To verify that the production quality is at the specified level	**1**. Early warning system is performed focusing on the device parameters and characteristics. **2**. Reliability tests are carried out to confirm the fluctuations and stability of the device parameters and characteristics in the initial stage of mass-production.

A range of electrical tests and techniques can be used to intercept critical device, including electrical wafer sorting (EWS) and burn-in (BI). These tests play a crucial role in assessing the performance and quality of semiconductor devices, both at wafer level as well as during the packaging phase. While, in case of custom incident (CI) different technique needs to be applied to get down to the breaking point, such as Fault Isolation (FI) and physical analysis. This section covers the main electrical test and CI analysis methods.

3.2.1 *Electrical Wafer Sorting (EWS)*

The device production usually takes place in the clean rooms that must obey to very high-quality standards in terms of amount airborne particulates, humidity, and temperature. Despite this, the introduction of defects is mainly due to particle contamination, process equipment drift or handling errors. Design errors can also lead to non-compliance with the circuit specifications. These defects result in functional problems in the chip: the circuit may not work at all or only partially, or it may fail after a few weeks. The EWS test is performed directly on the silicon wafer before it is diced and packaged, in order to have quick indication about the in-line quality and process variation, discriminate faulty devices before packaging, protecting the customer from damaged pieces [94,95].

More in details, the EWS test allows the detection of non-functional or at-risk devices through the application of an electrical stress by verifying the power consumption with a power supply between 80% and 120% of the nominal voltage. Generally, electrical tests are customised according to the specific use of the device, trying to simulate a test environment as close as possible to that of the target one, so test temperatures can vary from -40°C to 100°C. To perform such test, silicon wafers at the end of their manufacture are placed within a probe station that is connected to a tester. The probe is a key element in the measurement chain as it allows electrical contact between the device and the test. The test is typically made up of a printed circuit with tungsten-rhenium “tips” which is placed in contact with the device upmost surface thus ensuring the electrical contact. Tips are metal rods with a diameter ranging from 15 µm to 20 µm. Such printed circuit can have from a few to several hundred

tips, and can be very complex and expensive. The prober is a robot that manipulates wafers with μm-precision. It regulates the position of each device is such a way to place them in contact with the tip card through optical alignment. The test is a kind of program (controlled by dedicated software) that regulated a series of electrical parameters. The test program (controlled by a dedicated software) regulates the electrical parameters and defines the sequence of electrical signals, and the chip acceptance or rejection conditions. The tester is not dedicated to a particular circuit, only the test program is specific for each product. At the end of the test, one or more wafer maps are generated, and to each chip a 'bin' code indicating the type of defect is assigned. This electronic mapping is used to separate functional chips from defective (or potentially defective) devices. The wafer mapping also provides information on the cause of the defect, i.e. type of defect and geometric location. Numerous statistical tools are used to analyse these maps with the aim to minimise the risk of rejection for the customer.

3.2.2 *Burn-In (BI)*

The burn-in process consists in the application of marginal or accelerated thermal and electrical stresses to semiconductor components upon an extended period of time. The aim of such process is to recognise devices that would fail due to the infant mortality or during the early part of the "bathtub" curve of the device reliability (see Figure 17 in section 3.1). If the burn-in period is long enough and, at the same time, the operating conditions are sufficient to stress the devices, it is possible to assume that all infant mortality has been identified. Typically, stress conditions are temperature and voltage, applied for a time interval long enough to guarantee the screening of infant mortality (extrinsic defects) without affecting the intrinsic lifetime of the device. More generally, the conditions in the field are the set of very complex factors [96]. The semiconductor components may be subjected to real time or at the end of the burn-in process. Currently, components are burn-in at the "package level", which means that the individually packaged devices are typically tested after being derived from a wafer. Each device is tested and placed in sockets to be burn-in either as a packaged unit or as a bare die, i.e. prior to packaging. Both die-level and package-level burn-in can be expensive for manufacturers because of cycle time and chip management, equipment,

yield, and human resource. The reliability of the whole package is shown to be highly dependent on the reliability of each individual die. The usual method of achieving high reliability parts is to burn-in to eliminate extrinsic defects. However, there are very few alternatives to burn-in of unpackaged (bare) dies. These few alternatives are compared in terms of cost per burn-in die versus wafer volume. Recently, a number of improvements have been introduced that significantly reduce the cost per die.

3.2.3 *Fault Isolation (FI)*

In failure analysis, the position of the failure is achieved thanks to the use of fault isolation techniques [97]. FI tests typically employs electron beam testing, LASER Voltage Probing (LVP), emission/thermal analysis, Optical Beam Induced Current (OBIC) [98], and Optical Beam Induced Resistance Change (OBIRCH) [99–101] techniques, that relies on the generation of electron-hole pairs within the sample, induced by the raster scanning of a focused laser beam possessing energy equal to or greater than the band gap energy. Simultaneously, synchronized detection of the resulting current profile in relation to the positions of the laser beam is carried out. The aforementioned techniques are used to localize defect sites arising from metal semiconductor interdiffusion, electrostatic discharge, cavities in both metal wires and vias, short and current leak. Moreover, the conjugation of OBIC configurations, together with reflected confocal and optical beam-induced resistance change imaging, helped in observing nonuniformities at diffraction-limited resolution (~2.1 μm). Therefore, the device must be exposed without the package, which require some pre-processing including the disassembly of the package and the subsequent removal of the device top coating.

According to the type of failure, different fault isolation techniques are typically used. In particular, in the case of functional failures due to erroneous outputs directly generated from the logic, Electron beam testing or LVP are used, while Emission analysis or OBIRCH are deployed for leakage failures with an increased power current. More recently, the direct measure of the electrical characteristics in minute circuits, thanks to the use of a *nanoprobe* method, have made it possible to locate a failure with a significant high precision.

3.2.4 *Physical Analysis*

Physical analysis allows the assessment of the elemental/molecular composition of the failed point on the device with the aim to clarify the cause of failure. It provides final information that is fed back to the design and manufacturing processes. The defect, which is the cause of failure, sometimes exists between the surface and lower layers. In such a case, the dielectric film and metallic wiring must be removed. This procedure is performed while observing the spot using an optical microscope or SEM. It is sometimes necessary to observe the cross section of the chip with Focused Ion Beam (FIB). If any discoloration or particle is found at the failed location, composition analysis is carried out to clarify how it happened.

3.3 **Packaging process**

In the integrated circuit (IC) industry, steps ranging from the wafer lapping to the dice shipping are part of the back-end (BE) processes. In particular, the BE phase begins with the thinning of the wafer, followed by its electrical testing. Then, the process involves the cutting of the wafer in single dice and their encapsulation in packages. Finally, each package is placed in contact with an IC by means of metal interconnections. As the electrical performance of ready-to-use devices improves, and the size of devices shrinks, ever more sophisticated packaging techniques and materials are needed, since packaging plays a key role in ensuring the correct and long-lasting functioning of the entire electronic circuit. Device encapsulation within the package involves the use of bonding techniques through thin layers of metal. This process is called *die-attach*, and consists of a mechanical coupling of the die to its substrate. Unfortunately, metals used for bonding have much higher thermal expansion coefficients with respect to those of packaging materials. This originates significant residual stresses within the device and the onset of new interconnections which can lead to a change in the operating characteristics of the device or, more generally, to device failure due to package, die or solder bump crack, wire break and delamination. Furthermore, this process is critical in terms of both thermal and electrical performances. In order to minimize the thermo-mechanical stresses of the device and

thus improve its mechanical strength and resistance, it is necessary to use materials with a low thermal expansion coefficient.

The device package has several functions, including protecting the electronic devices from the external environment preventing the contact with chemical solutions, light exposure or mechanical impact. In general, it is necessary for the packaging to be dark and airtight to prevent the creation of humidity which favors the development of corrosion responsible of failures. Furthermore, the device package must be able to properly dissipate the heat generated by the device, and for this reason different materials are typically employed, such as plastics (siloxane polyimide, polyxylylene, silicones, polyepoxides and bisbenzocyclo-butene), metal, glass and ceramics. It must also provide a connection between the device (made up of one or more dies) and the external environment, such as an integrated circuit board provided by conductors for the distribution of electrical and power signals.

Wire bonding is an electrical interconnection technique that uses a combination of heat, pressure and ultrasonic energy to join two metallic materials (wire and pad surface). In the wire bonding process, the adhesive force can cause deformation of the material, and the application of ultrasonic energy amplifies these effects. Heat can accelerate interatomic diffusion and hence bond formation. Ultimately [102], wire bonding processes result in the formation of an irregular intermetallic compound (IMC) between the wires and their substrate, with voids or cracks within them, which have a significant effect on the reliability of the bond. An adequate amount of IMC formed in a metallic bond will increase the bond strength, but excessive growth can lead to a reduction in bond performance. Increased IMC growth can also result in increased brittleness and increased contact resistance, leading to increased heat generation during operation, which in turn accelerates IMC growth, ultimately leading to bond failure [103]. The wires are soldered using a specific tool (capillary or wedge). Depending on the bonding agent (heat and ultrasonic energy), the bonding process can be divided into three processes:

- Thermo-compression bonding (T/C);
- ultrasonic bonding (U / S);
- thermosonic bonding (T / S).

There are two basic forms of wire bonding: ball-bonding and wedge-bonding, as shown in Figure 22.

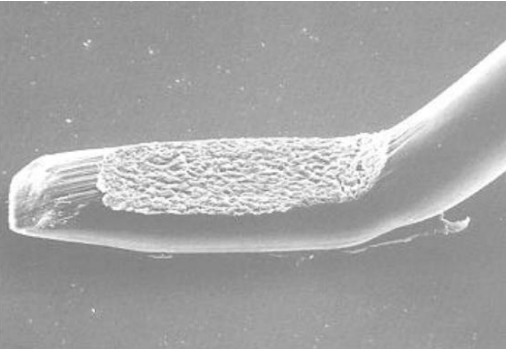


Figure 22: *Ball- and wedge-bonding.*

Ball-bonding, despite its widespread use, is not the best solution for high power devices, as the size of the wire provides a limit to its conductivity. In addition, to avoid short circuits, it is necessary to provide bonding in the peripheral regions of the chip. This makes wire bonding not feasible for devices with high pin densities (e.g. over 500 pins). At present, ball-bonding with thermosonic bonding for gold is the most widely used wire bonding technique, mainly because it is faster than ultrasonic bonding for aluminium. Once ball-bonding has been performed on the machine, the wire can be moved in any direction without stressing the wire, which greatly facilitates automated bonding, since the movement only needs to be in the x and y directions.

CHAPTER 4
EXPERIMENTAL

4.1 **Standard microscopy combined with Thermal Emission Camera**

Thermal emission (THe) refers to the release of energy in the form of electromagnetic waves from any object with a temperature exceeding absolute zero. The THe originating from a blackbody (an ideal thermal emitter) is regulated by the Planck's law [104] and only depends on its temperature. THe in a non-ideal thermal emitter, also depends on how effectively the emitter can radiate, and is quantified by its *emissivity*. In the case of an object in thermal equilibrium, Kirchhoff's law demonstrates that the object *emissivity* exactly matches its *absorptivity,* which can be indirectly obtained by measuring the absorption via a combination of reflection, transmission, and scattering measurements.

The assessment of the thermal emission from a sample can be challenging because almost every component of the object and the surrounding environment thermally radiates light, resulting in a background signal that may be difficult to isolate.

The monitoring and controlling of thermal radiation find applications especially in all those technological platforms where regulating a temperature is relevant, including thermal camouflaging [105–107], circuitry [108–111], spectroscopy [112], sensing and thermal photonics [113].

4.1.1 *Planck's law of thermal radiation*

Planck's law regulates the correlation between a body's temperature and the characteristics of its thermal emission, encompassing both amplitude and spectrum. In particular, it defines the *spectral emissive power* (energy per unit volume), denoted as $M_{\omega}(\omega, T)$, for an emitter at temperature T and frequency ω.

In the case of a blackbody (an indented box (cavity) lined internally with highly reflecting surfaces) radiation consists of a superposition of non-interacting

monochromatic waves due to the linearity of the equations of Maxwell's equations. Keeping the cavity at a constant temperature, and tacking into account the quantization of the electromagnetic field, the radiation can be interpreted as a gas of massless bosons (photons) that reaches thermal equilibrium with the cavity.

Classically, the confinement within a cubic cavity of volume V of electromagnetic waves is equivalent to the imposition of boundary conditions for the wavefield $\boldsymbol{\Psi}(x, y, z, t; \omega)$ [114], *i.e.*:

$$\begin{cases} \boldsymbol{\Psi}(0, y, z, t; \omega) = \boldsymbol{\Psi}\left(V^{\frac{1}{3}}, y, z, t; \omega\right) = 0 \\ \boldsymbol{\Psi}(x, 0, z, t; \omega) = \boldsymbol{\Psi}\left(x, V^{\frac{1}{3}}, z, t; \omega\right) = 0 \\ \boldsymbol{\Psi}(x, y, 0, t; \omega) = \boldsymbol{\Psi}\left(x, y, V^{\frac{1}{3}}, t; \omega\right) = 0 \end{cases} \tag{39}$$

corresponding to the following resonance conditions:

$$\omega^2 = \frac{\pi^2 c^2 \left(n_x^2 + n_y^2 + n_z^2\right)}{4V^{\frac{2}{3}}} = \frac{\pi^2 c^2 n^2}{4V^{\frac{2}{3}}}, \tag{40}$$

where n_x, n_y and n_z are non-negative integers and c is the speed of light in vacuum. The number N of oscillators (photons) with pulsation in $[\omega, \omega + \Delta\omega]$ is given, due to the non-negativity of n_i, by the volume between the radii $\frac{\omega V^{\frac{1}{3}}}{\pi c}$ and $\frac{(\omega+\Delta\omega) V^{\frac{1}{3}}}{\pi c}$ of a spherical octant, as:

$$\begin{aligned} N &= 2 \cdot \frac{1}{8} \iiint_{\frac{\omega V^{\frac{1}{3}}}{\pi c} < n < \frac{(\omega+\Delta\omega) V^{\frac{1}{3}}}{\pi c}} dn_x\, dn_y\, dn_z = 2 \cdot \frac{1}{8} \cdot \frac{1}{4} \cdot \pi \cdot \frac{V}{\pi^3 c^3} \left((\omega + \Delta\omega)^3 - \omega^3\right) \\ &= 2 \cdot \frac{1}{8} \cdot \frac{4}{3} \cdot \pi \cdot \frac{V}{\pi^3 c^3} (3\omega^2 \Delta\omega) = \frac{V \omega^2 \Delta\omega}{\pi^2 c^3} \end{aligned} \tag{41}$$

where factor 2 takes into account the two independent polarization states of the electromagnetic waves.

The contribution of oscillators pulsating in [ω, ω + Δω] to the free energy of Helmholtz A can be written as:

$$A = -Nk_bT \ln Z = \frac{V\omega^2 \Delta\omega}{\pi^2 c^3} k_B T \ln Z, \tag{42}$$

with k_B equal to the Boltzmann constant (k_b = 1,3806488 10^{-23} JK^{-1}), T is the temperature and Z is the *boson partition function*.

Then, the internal energy E_{int} of the blackbody radiation is therefore:

$$E_{int} = -T^2 \left(\frac{\partial}{\partial T}\frac{A}{T}\right)_V = \frac{V\omega^2 \Delta\omega}{\pi^2 c^3} k_B T^2 \left(\frac{\partial}{\partial T} \ln Z\right)_V. \tag{43}$$

The elemental *emissive power* in the interval [ω, ω + Δω] (ΔM_ω) radiated by the surface $\Delta\Sigma$ of the blackbody in the time Δt in the solid angle $\Delta\Omega$ around the direction of the versor $\mathbf{e}_\varepsilon$, can be written as the *density of spectral energy* U_ω in the same interval, contained in the volume ΔV of the cylinder of base $\Delta\Sigma$ and height $c\Delta t$ coincident with the direction of the versor $\mathbf{e}_\varepsilon$, multiplied by the fraction of solid angle $\Delta\Omega/4\pi$ (see Figure 23):

$$\Delta M_\omega \Delta\omega \Delta\Sigma \Delta t = \frac{U_\omega \Delta\omega \Delta V \Delta\Omega}{4\pi} \tag{44}$$

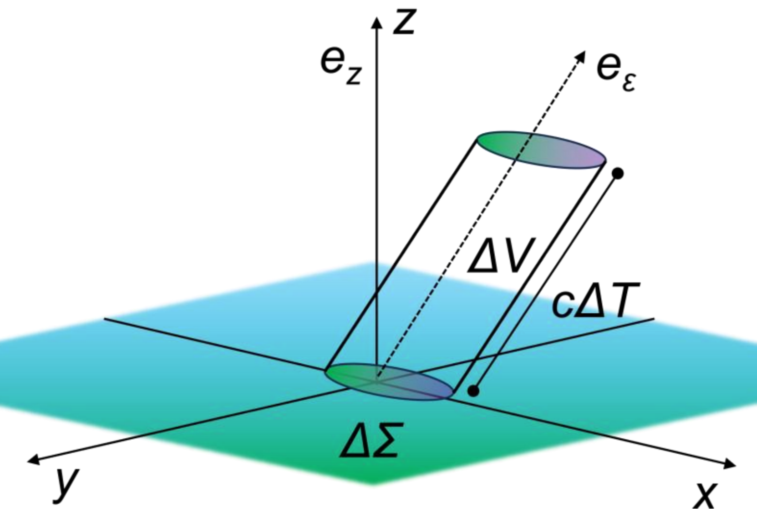


Figure 23: *Black body emitting surface.*

For the volume element, $\Delta V = \Delta\Sigma \mathbf{e_z} \cdot c\Delta t \mathbf{e_\varepsilon}$, where $\mathbf{e_z}$ is the z-axis direction Eqn. 44 yields to:

$$\Delta M_\omega = U_\omega \Delta V \frac{\Delta\Omega}{4\pi\Delta\Sigma\Delta t} = \frac{cU_\omega}{4\pi}\Delta\Omega\,(\boldsymbol{e_z}\cdot\boldsymbol{e_\varepsilon}). \qquad (45)$$

In polar coordinates:

$$\begin{cases} \Delta\Omega = \sin\theta d\theta\, d\varphi \\ \boldsymbol{e_z}\cdot\boldsymbol{e_\varepsilon} = cos\theta \end{cases}$$

The *spectral emissive power* M_ω is therefore given by the integral of the elemental emissive power ΔM_ω as:

$$M_\omega = \int_\Omega \frac{\Delta M\omega}{\Delta\Omega} d\Omega = \frac{cU_\omega}{4\pi}\int_0^{2\pi} d\varphi \int_0^{\frac{\pi}{2}} \sin\theta\cos\theta\, d\theta = \frac{cU_\omega}{4}. \qquad (46)$$

As can be seen from Eqn. 46, the assessment of the *spectral emissive power* requires the derivation *density of spectral energy* U_ω. To this purpose, starting from Eqn. 43,

the energy density ΔU, defined as $\Delta U_\omega = E_{int}/V$, in the interval [ω, ω + Δω], can be written as:

$$\Delta U = \frac{\omega^2 \Delta\omega}{\pi^2 c^3} k_b T^2 \left(\frac{\partial}{\partial T} \ln Z\right)_V, \tag{47}$$

and hence the *density of spectral energy* U_ω, calculated as $\Delta U / \Delta\omega$, now became:

$$U_\omega = \frac{\omega^2}{\pi^2 c^3} k_B T^2 \left(\frac{\partial}{\partial T} \ln Z\right)_V. \tag{48}$$

The *boson partition function Z* is given by the geometric serie:

$$Z = \sum_{n=0}^{\infty} \exp\left(-\frac{n\hbar\omega}{k_B T}\right) = \frac{1}{1 - \exp\left(-\frac{\hbar\omega}{k_B T}\right)}, \tag{49}$$

where $\hbar$ is the reduced Planck constant. Substituting the Eqn. 49 into Eqn. 48 we obtain the final expression of the *density of spectral energy* of the blackbody:

$$U_\omega = \frac{\omega^2}{\pi^2 c^3} k_b T^2 \left(\frac{\partial \ln\left(\frac{1}{1 - \exp\left(\frac{-\hbar\omega}{k_B T}\right)} \right)}{\partial T} \right) = \frac{\hbar}{\pi^2 c^3} \cdot \frac{\omega^3}{\exp\left(\frac{\hbar\omega}{k_B T}\right) - 1}, \tag{50}$$

which allows the derivation of the *spectral emissive power* M_ω, according to Eqn. 46:

$$M_\omega(\omega, T) = \frac{c U_\omega}{4} = \frac{\hbar}{4\pi^2 c^2} \cdot \frac{\omega^3}{\exp\left(\frac{\hbar\omega}{k_B T}\right) - 1}, \tag{51}$$

Also known as *Planck's law (*Figure 24*).*

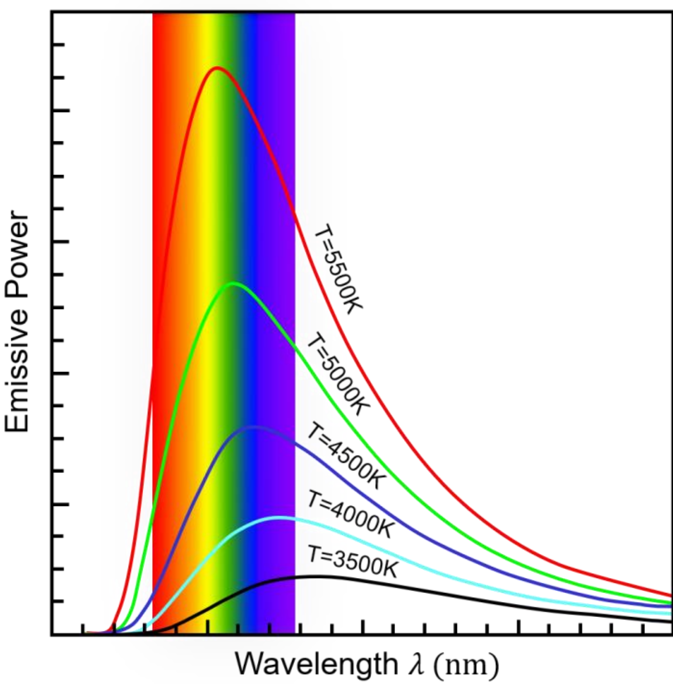


Figure 24: *Blackbody spectral power distribution.*

The thermal emission outcome is thus solely dependent by the modulation of a blackbody emitter's temperature. In fact, the manipulation of temperature in Eqn. 51 results in significant alterations to both the central frequency and the amplitude of the the *spectral emissive power* of a blackbody emitter.

It is possible to evaluate the *bolometric emittance* of a blackbody (M_{BB}) by integrating the emissive power (Eqn. 51) over the whole spectrum:

$$M_{BB} = \int_0^\infty M_\omega d\omega = \int_0^\infty \frac{\hbar}{4\pi^2 c^2} \cdot \frac{\omega^3}{\exp\left(\frac{\hbar\omega}{k_B T}\right) - 1}. \tag{52}$$

By substituting $\delta = \frac{\hbar\omega}{k_B T}$, there is:

$$M_{BB} = \frac{\hbar}{4\pi^2 c^2} ({k_B}^3 T^3/\hbar^3) \int_0^\infty \frac{\delta^3}{\exp(\delta) - 1} (k_B T/\hbar) d\delta. \tag{53}$$

Considering that the result of the integral is $\pi^4/15$, Eqn. 53 yields to:

$$M_{BB} = \frac{\hbar}{4\pi^2 c^2} ({k_B}^3 T^3/\hbar^3\ ) \ (k_B T/\hbar) \ (\pi^4/15) = \frac{\pi^2 {k_B}^4}{60 c^2 \hbar^3} \ T^4, \qquad (54)$$

known as *Stefan-Boltzmann's law*, with $\frac{\pi^2 {k_B}^4}{60c^2\hbar^3} = \sigma$ *Stefan-Boltzmann constant* equal to $5.670373 \cdot 10^{-8}$ W/m^2K^4.

It is worth of note that all real bodies have intermediate emitting properties between those characteristics of *blackbodies* (BB, ideal absorbers) already described, and those related to *whitebodies* (WB, i.e. an ideal body that reflects all incident radiation with no absorption).

Is this case, it is common to refers to such materials as *greybodies* (GB).

More in details, the *spectral emissive power* M_ω of a grey body is obtained by taking into account a quantity called *emissivity* (ε_ω), which serves as a metric of the efficiency of an emitting body as a thermal emitter. Emissivity is defined as the ratio between the *spectral emissive power* of a *greybody* $M_{\omega,\mathrm{GB}}$ and that of a *blackbody* $M_{\omega,\mathrm{BB}}$, under the same conditions of temperature T and frequency ω:

$$\varepsilon_\omega = \frac{M_{\omega,\mathrm{GB}}}{M_{\omega,\mathrm{BB}}}. \qquad (55)$$

Thus, the *emissive power* of a *greybody* $M_{\omega,\mathrm{GB}}$, can be derived by multiplying its spectral *emissivity* with the *spectral emissive power* of the BB, which yields to:

$$M_{\omega,\mathrm{GB}} = \varepsilon_\omega M_{\omega,\mathrm{BB}} = \varepsilon_\omega \frac{\hbar}{4\pi^2 c^2} \cdot \frac{\omega^3}{\exp\left(\frac{\hbar\omega}{k_B T}\right) - 1}. \qquad (56)$$

With similar mathematical manipulations already carried out into Eqns. 14,16, the *bolometric emittance* of a greybody M_{GB} can be written as:

$$M_{GB} = \varepsilon_{\omega}\sigma T^4, \tag{57}$$

which generalizes the *Stefan-Boltzmann law*.

It is worth of note that the Planck's law intrinsically assumes that the dimension of the emitting body as well as the distance d at which the spectral flux is collected, are much larger with respect to the typical dimension of the thermal wavelength [115], given by:

$$\lambda_t = \pi^{\frac{3}{2}} \frac{\hbar c}{k_B T}, \tag{58}$$

With respect to λ_t, it is possible to distinguish two different regions, termed *far-field* (FF) and *near-field* (NF), according to the value of the d/λ_t ratio. In particular, for $d \gg \lambda_t$, (i.e. far away from a thermal emitter) the FF radiative heat transfer occurs, while for $d \ll \lambda_t$, describing regions very close to the thermal emitter, the NF must be considered. To properly highlight the difference between the aforementioned regions, let us consider a monochromatic thermal emitter positioned at a point $\boldsymbol{r} = \boldsymbol{r_0}$ within an isotropic and homogeneous medium. The amplitude of the electric field $\mathrm{E}(\boldsymbol{r}, \omega)$ measured at a point $\boldsymbol{r}$ can be assessed considering the plane wave:

$$E(\boldsymbol{r}, \omega) = E_0 e^{i[\boldsymbol{k}(\boldsymbol{r}-\boldsymbol{r_0})-\omega t]},$$

With E_0 equal to the electric field amplitude measured at $\boldsymbol{r_0}$, **k** is the wavevector, ω is the angular frequency, and t is the time. In the case in which the wavevector **k** assumes real values, then at a distance **r** from the source the field $E(\boldsymbol{r}, \omega)$ gains a phase $e^{i[\boldsymbol{k}(\boldsymbol{r}-\boldsymbol{r_0})]}$ while maintaining the amplitude, which yields to a *propagating wave*. The FF domain exclusively consists, by definition, of propagating waves. In the Fourier space these waves are constrained within the region enclosed by the light cone, outlined by $k_0 = n\,\omega/c$, with n equal to the refractive index of the surrounding medium, and c is the speed of light in vacuum (Figure 25a). A different behaviour is achieved when the transverse component of the wavevector extends to values of k beyond the light cone. This leads to complex wavevector in $\mathrm{E}(\boldsymbol{r}, \omega)$, resulting in an

exponentially decaying wave away from its source known as *evanescent wave* (Figure 25b). A representation of two objects engaged in radiative heat exchange in FF and NF is illustrated in Figure 25c,d.

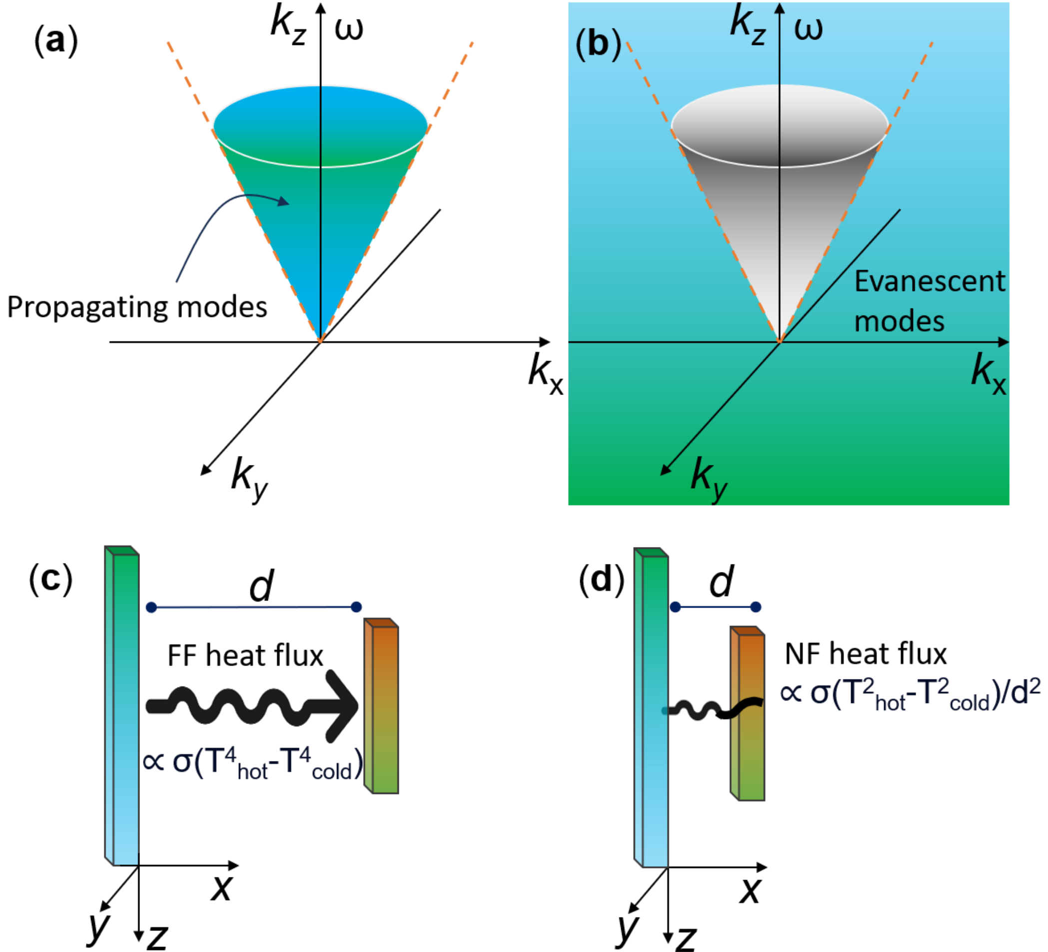


Figure 25: *Schematic representation of the (a) FF and (b) NF waves in the Fourier space. Panels (c) and (d) displays, respectively, the thermal radiation exchange in (c) FF and (d) NF between two plan surfaces at different temperatures.*

4.1.2 *Infrared thermography*

Matter at temperatures above of absolute zero emits thermal radiation. The amount of radiation emitted, measured by the bolometric emittance, is proportional to the fourth power of the temperature of the source (*Stefan-Boltzmann law* – Eqn. 57).

The temperature of a body can therefore be measured by measuring *its bolometric emittance* and applying the Stefan-Boltzmann law.

Materials at room temperature (around 300 K) emit most of their radiation in the infrared (IR) region of the electromagnetic spectrum. Thus, their temperature can be measured by assessing their infrared emission. This technique is referred to as infrared thermography (IRT). IRT exploits the ability of certain devices, the so-called thermal cameras, to detect the intensity of thermal radiation emitted in the infrared region of the electromagnetic spectrum. These devices produce thermal maps, in greyscale or false colours, of the intensity of thermal radiation emitted in which the signal coming from each point of the image (pixel) is associated to a temperature value. These images are also called *thermograms*.

The ensemble of phenomena accompanying the emission of radiation from a source up to absorption by a detector is referred to as the *radiometric chain*. The electromagnetic signal detected by the thermal camera is not simply the radiation coming from the observed device, but also includes the radiation reflected and transmitted by bodies. Therefore, the distance from the source, humidity and ambient temperature also needs to be taken into account. The angle of observation is not negligible when the body is not in thermal equilibrium, as thermal radiation is generally not isotropic, or when diffracted radiation is observed, the intensity of which is modulated by an obliquity factor. Eqn. 57 points out that the *emissivity* of the body is of fundamental relevance since it is crucial in the emittance-temperature conversion. All these parameters can be achieved directly into the thermal imaging camera or thanks to post-acquisition processing software.

4.2 **Experimental setup**

One of the targets of this thesis is to define a possible experimental protocol to identifying failure in the MOM component by analysing wafer coming from the *STMicroelectronics S.r.l.* farm. Various techniques have been explored to accomplish this purpose, but failure detection has proven to be a challenging task. For instance, the assessment of the leakage current in a potential DC configuration was found to be ineffective due to insufficient repeatability, often resulting in disruptive tests. The

accurate identification and analysis of a non-functioning device before it is shipped to the customer is of paramount importance as it has a direct impact on quality issues. Moreover, the ability to discriminate between functional and non-functional devices without inducing physical damage, such as avoiding burns, is of crucial importance if the aim is to examine the extraneous element responsible for the faulty device. By applying an electrical signal to a capacitor, the dielectric undergoes a displacement current, resulting in energy dissipation and temperature increase. Specifically, thermal variations are more pronounced in the presence of defects, resulting in a non-uniform thermal map in terms of temperature distribution, i.e. the thermal emission. Therefore, it is possible to detect the presence of a faulty component by observing the thermal maps. Taking into consideration the aforementioned aspects, it was decided to apply an alternating signal to the MOM component and acquire thermal maps to assess the temperature variations caused by defects. Since tests were performed on bare wafers, the setup had to be configured as a probe station. This setup includes two tungsten tips and two micrometric positioning stages capable of movement in the X, Y and Z directions (Thorlabs PT3A/M). These stages provide sub-micron precision over 1" of travel (see Figure 26).

Figure 26: *Thorlabs Probe stations image.*

To complete the bench the following elements have been used:

- Hewlett Packard E3632A DC Power Supply (see Figure 27) that is a high-performance supply optimized for manual and basic automated testing; and,

with a combination of benchtop capabilities and system features, it is designed to help improve measurement quality and reduce test time.

Figure 27: *Hewlett Packard E3632A DC Power Supply picture.*

- DS345 Function Generator that is a full-featured 30 MHz synthesized function generator (see Figure 28). It uses a Direct Digital Synthesis (DDS) architecture and generates many standard waveforms with excellent frequency resolution (1 μHz), and has versatile modulation capabilities including AM, FM, Burst, PM and frequency sweeps. The amplitude of all function outputs is adjustable from 10 mVpp to 10 Vpp with 3-digit resolution, and can be displayed in Vp, Vpp, Vrms or dBm. In addition, standard TTL and ECL output levels can be selected. The DS345 Function Generator offers a wide variety of modulation options. It contains an internal modulation generator which can modulate any of its standard waveforms except noise. The modulation waveform can be a sine, square, triangle, ramp or an arbitrary waveform. Modulation rates from 1 mHz to 10 kHz can be selected. The modulation generator can provide amplitude modulation (AM), frequency modulation (FM), and phase modulation (PM). In addition to the internal modulation generator, the output waveform can be amplitude modulated by an external signal applied to the rear-panel AM input. This input is always active—even when other modulation types are turned on.

Figure 28: *DS345 Function Generator picture.*

- The output of the signal generator was delivered to a solid-state amplifier chain. In particular, two broadband amplifiers were used, the first of those is a dual-stage amplifier and has a bandwidth ranging from 1 to 900 MHz with a maximum power of 2W. The second is a single-stage amplifier based on a PD 55008 power MOSFET that can deliver a maximum of 8W with 17dB gain @ 500 MHz/12.5 V. The last mentioned device is a common source N-channel, enhancement-mode lateral field-effect RF power transistor. It is designed for high gain, broad band commercial and industrial applications. It operates at 12 V in common source mode at frequencies up to 1 GHz. A 3dB attenuator was used to connect the two amplifiers, in order to reduce the output power of the first amplifier and prevent the self-oscillation of the chain.

- to accurately contact the device pads (see Figure 29), an optical microscope with up to 50x magnification was used.

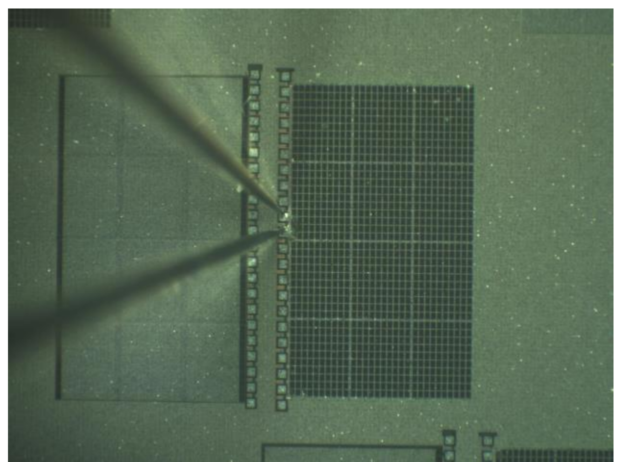


Figure 29: *The image represents the giant 3 of the DUT contacted through the tungsten tips. The image was captured using the optical microscope at 20x magnification.*

- Longwave Infrared Thermal Camera Module Tau® 2 was used to catch the thermal images (see Figure 30). This camera offers an unmatched combination of features and reliability, making them well-suited for several applications. Improved electronics provide powerful image processing modes that dramatically improve detail and contrast through continuous histogram equalization. Radiometry is available in every pixel for both 640 × 512 and 336 × 256 resolutions and all three camera grade levels. All Tau 2 configurations share electrical, mechanical, and optical interfaces allowing integrations to be designed that work seamlessly with all formats. The main features of the thermal camera are:
    - Pixel Size: 17 µm;
    - Frame Rate Options: 30/60 Hz (NTSC) 25/50 Hz (PAL)
    - Thermal Sensitivity/NETD Commercial: <60mK
    - Scene Temperature Range: -40°C to +550°C

Figure 30: *Longwave Infrared Thermal Camera Module Tau® 2.*

Before to proceed with a thermal measurement, a camera calibration was required. This was possible through the use of FLIR Camera Controller GUI software linked to the thermal camera. The principal step for the calibration procedure involves the use of wo black bodies, one of it needs to be approximately 20 °C apart from the other. It was recommended to wait about 30 minutes for black body source to reach operating temperature and stabilize. At this point, the camera will monitor its internal temperature and verify stability. Through the GUI was possible to acquire the hot source in front of the camera. After this, a cold black body was placed in front of the camera. Then, it will calculate the gain and perform an FFC. The correction term will then be enabled, and the quality of the image must be assessed. The gain is stored in the camera's DRAM. To proceed correctly during calibration, the following points must be observed:

- The camera should be left focused as it is to be used;
- The delay between taking the warm and cold sample should be as short as possible;
- The black-bodies should be approximately 20 °C apart;
- When required by the procedure, the camera should be positioned close to the black-body so the entire camera field of view is covered;
- The black-bodies should not be allowed to heat the end of the camera lens. Shield the camera from the hot black body when not in use;

A scheme of the electrical circuit used to send a power signal to the DUT is shown in Figure 31b, where A1, -3dB and A2 represents the dual-stage amplifier, the signal attenuator and the single-stage amplifier based on a PD 55008 power mosfet, respectively. Also, the coaxial cable is represented to highlight the connection with the two tips. The wafer placement has been included as example. Finally, the optical microscope and thermal camera are mutually exchangeable and placed on above the sample to carry out the measurements, see Figure 31a,b.

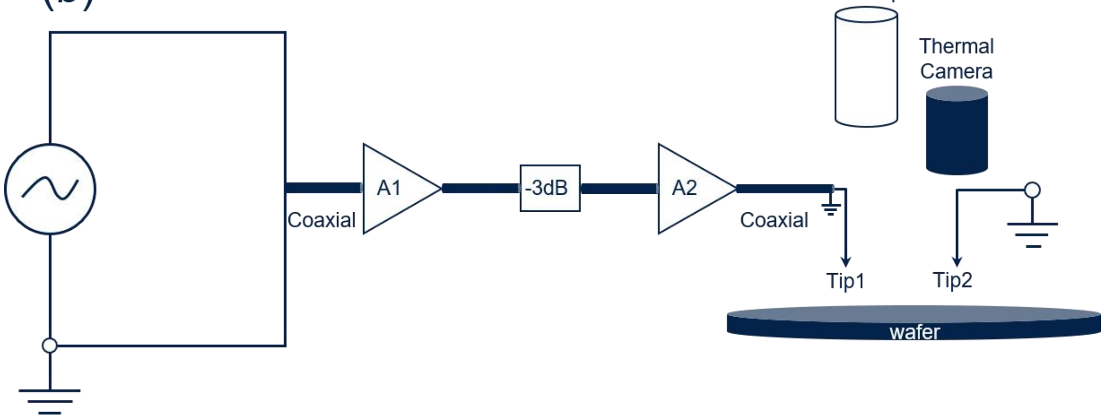


Figure 31: *(a) photograph of the home-made setup employed; (b) schematic representation of the used setup where A1, -3dB and A2 represents the dual-stage amplifier, the signal attenuator and the single-stage amplifier respectively. The wafer placement has been included as example. the optical microscope and thermal camera are mutually exchangeable and placed on above the sample.*

4.3 **Raman spectroscopy**

In this thesis, Raman spectroscopy has been used to assess residual stress in power devices, as it has a significant impact on performance and reliability. This analysis involves the investigation and evaluation of the frequency shift of specific spectral components of the DUT under different conditions, such as applied stress, temperature, humidity, encapsulation, etc.

The Raman spectroscopy is a powerful tool that allows for the simple, non-invasive, fast, and efficient understanding of the structural, chemical, and electronic properties of a wide range of materials. The phenomenon of Raman scattering was first observed experimentally in neat solvents by 1928 by Raman and Krishnan and defined as a "*feeble fluorescence*". Raman scattering involves a frequency change in a small percentage of the intensity of a monochromatic beam as the result of coupling between the incident radiation and vibrational energy levels of molecules. The theory of the Raman effect was developed between 1930 and 1934 by the Czechoslovakian physicist George Placzek.

The basic principle behind the frequency changes detected in Raman scattering lays in the exchange of energy between the scattering system and the incoming radiation and can be explained through both a classical and quantum approach.

4.3.1 *Classical approach*

According to the classical theory of electromagnetic radiation, the dipole moment induced by the electric field **E** could be expressed by the power series:

$$\mu = \alpha \cdot \boldsymbol{E} + \beta \cdot \boldsymbol{EE} + \gamma \cdot \boldsymbol{EEE} + \cdots + \delta \cdot \boldsymbol{E^n}, \tag{59}$$

where α, β and γ second-rank polarization tensors of the molecule at first, second and third order. Typical order of magnitude of α, β and γ are 10^{-40} Cm^2V^{-1}, 10^{-50} Cm^3V^{-2} and 10^{-61} Cm^4V^{-3}, respectively. The first term is associated with Rayleigh and Raman scattering processes while the second-order term describe the Hyper-Rayleigh and Hyper-Raman scattering processes. Even under high electric field, high-order terms of

Eqn. 59 are almost negligible, and for this reason and one can reasonably consider explaining Raman scattering in terms of $\mu = \alpha \cdot \boldsymbol{E}$ only.

Let's consider a simple interaction of a molecular system with a harmonically oscillating electric field at the frequency ν_0. For simplicity, we will momentarily neglect rotational effects and focus solely on the vibrational aspect. Under such circumstances the polarizability will fluctuate in response to changes in the nuclear coordinates. This alteration is articulated through a Taylor series, highlighting the nuanced interplay between the polarizability tensor components and the vibrational coordinates. In particular, the dependence of α on the position of the nuclei can be considered, in the case of small vibrations, by expanding the Taylor series polarizability tensor close to equilibrium positions of the nuclei:

$$\alpha_{ij} = \left(\alpha_{ij}\right)_0 + \sum_k \left(\frac{\partial \alpha_{ij}}{\partial Q_k}\right)_0 Q_k + \frac{1}{2}\sum_{k,l} \left(\frac{\partial^2 \alpha_{ij}}{\partial Q_k \partial Q_l}\right)_0 Q_k Q_l + \cdots , \qquad (60)$$

where $\left(\alpha_{ij}\right)_0$ is the ij-element of the polarization tensor at the equilibrium condition, while Q_k and Q_l are the normal vibration coordinates at frequencies ν_k and ν_l, respectively.

Under harmonic approximation, terms which involve powers of Q higher than first can be ignored and Eqn. 60 became:

$$\alpha_{ij} = \left(\alpha_{ij}\right)_0 + \sum_k \left(\frac{\partial \alpha_{ij}}{\partial Q_k}\right)_0 Q_k. \qquad (61)$$

For a harmonic vibration (normal mode) of the $Q_k = Q_{0k} \cos(2\pi\nu_k t + \delta_k)$ type, the expression of the α tensor resulting from k-th vibration can be written as:

$$\alpha_k = \alpha_0 + \left(\frac{\partial \alpha_k}{\partial Q_k}\right)_0 Q_{k0} \cos(2\pi\nu_k t + \delta_k). \qquad (62)$$

In the light of the aforementioned considerations, the first-order dipole moment induced by the electric field $\boldsymbol{E} = \boldsymbol{E}_0 \cos(2\pi\nu_0 t)$ can now be rewritten as:

$$\mu = \alpha_k \boldsymbol{E} = \alpha_0 \boldsymbol{E}_0 \cos(2\pi\nu_0 t) + \left(\frac{\partial \alpha_k}{\partial Q_k}\right)_0 Q_{k0}\, \boldsymbol{E}_0 \cos(2\pi\nu_k t + \delta_k) \cdot \cos(2\pi\nu_0 t) =$$

$$\alpha_0 \boldsymbol{E}_0 \cos(2\pi\nu_0 t) + \frac{1}{2}\left(\frac{\partial \alpha_k}{\partial Q_k}\right)_0 Q_{k0}\, \boldsymbol{E}_0 \cos(2\pi\nu_k t + 2\pi\nu_0 t + \delta_k) +$$

$$\frac{1}{2}\left(\frac{\partial \alpha_k}{\partial Q_k}\right)_0 Q_{k0}\, \boldsymbol{E}_0 \cos(2\pi\nu_k t - 2\pi\nu_0 t - \delta_k). \quad (63)$$

From Eqn. 63, the linear induced dipole moment turns out to be composed of three components with different frequencies, i.e. $\alpha_0 \boldsymbol{E}_0 \cos(2\pi\nu_0 t)$, which yields to radiation at ν_0 and accounts for the *Rayleigh* scattering, and the two terms $\frac{1}{2}\left(\frac{\partial \alpha_k}{\partial Q_k}\right)_0 Q_{k0}\, \boldsymbol{E}_0 \cos(2\pi\nu_k t \pm 2\pi\nu_0 t \pm \delta_k)$ which give rise to radiation at $\nu_0 - \nu_k$ and $\nu_0 + \nu_k$ accounting, respectively, for the *Stokes* and *Anti-Stokes* Raman scattering phenomena (see Figure 32 [116]).

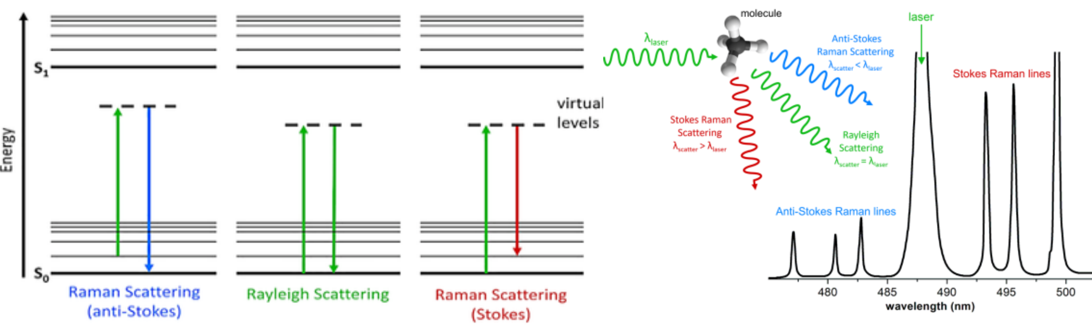


Figure 32: *Jablonski diagram showing the origin of Rayleigh, Stokes and Anti-Stokes Raman Scattering.*

4.3.2 *Quantum mechanical approach*

The classical theory, however, fails to clearly explain neither the differences in intensity between Stokes and anti-Stokes emission lines nor their temperature dependence. For the description of all these aspects there is a need for a comprehensive quantum theory which makes use of Fermi's *golden rule* to derive the emission rate of the process:

$$W_{mn} = \frac{2\pi}{\hbar} \left| \langle \Psi_m | \tilde{V} | \Psi_n \rangle \right|^2. \quad (64)$$

Here, W_{mn} describes the probability per unit time that the total system composed of the probe and the reservoir changes from the initial state *m* to the final state *n*, described by the Ψ_m and Ψ_n wavefunctions. The computation of the interaction Hamiltonian for scattering processes requires the employment of a complete second-order expression for both the interaction (considering the quadratic term in the field) and the perturbation (the development of the perturbative series):

$$W_{mn} = \frac{2\pi}{\hbar} |\mathrm{K}_1^2 + \mathrm{K}_2^1|^2, \tag{65}$$

with:

$$\mathrm{K}_2^1 = \frac{e^2}{mc^2} \frac{2\pi\hbar c}{L^3} \frac{1}{\sqrt{kk'}} (\epsilon_{\boldsymbol{k}\lambda} . \epsilon_{\boldsymbol{k}'\lambda'}) \times \langle \Psi_m | [\hat{a}_{k\lambda} \hat{a}^{\dagger}{}_{k'\lambda'} + \hat{a}^{\dagger}{}_{k'\lambda'} \hat{a}_{k\lambda}] e^{i(\boldsymbol{k}-\boldsymbol{k}')\cdot \boldsymbol{r}} | \Psi_n \rangle$$
$$= 2 \left(\frac{e^2}{2mc^2} \right) \left(\frac{2\pi\hbar c}{L^3} \right) \frac{1}{\sqrt{kk'}} (\epsilon_{\boldsymbol{k}\lambda} . \epsilon_{\boldsymbol{k}'\lambda'}) e^{i\boldsymbol{Q}\cdot \boldsymbol{r}} \delta_{nm}, \tag{66}$$

with k, k’, $\epsilon_{\boldsymbol{k}\lambda}$ and $\epsilon_{\boldsymbol{k}'\lambda'}$ equal to the incident, scattered wavevector and polarization. In this case, we have assumed that the probe is made up of photons of momentum **k** and polarization $\boldsymbol{\epsilon}$. which carries a non-zero contribution only in the case where the initial state of the system coincides with the final state, thus in the case of elastic scattering (*Rayleigh* scattering).

The *inelastic* scattering contribution can be derived from the development of the term at first order in the field and second order of the perturbation which, using the approximation dipole approximation can be written:

$$\mathrm{K}_1^2 = \frac{m}{\hbar^2 e^2} r_0 \left(\frac{2\pi\hbar c}{L^3} \frac{1}{\sqrt{kk'}} \right) e^{i\boldsymbol{kR}} \sum\nolimits_L (E_l - E_m)(E_n - E_l)$$
$$\times \left[\frac{(\epsilon_{\boldsymbol{k}'\lambda'} \cdot \mu_{ml})(\epsilon_{\boldsymbol{k}\lambda} \cdot \mu_{ln})}{(E_l - E_m - \hbar\omega_k)} + \frac{(\epsilon_{\boldsymbol{k}\lambda} \cdot \mu_{ml})(\epsilon_{\boldsymbol{k}'\lambda'} \cdot \mu_{ln})}{(E_l - E_n - \hbar\omega'_k)} \right], \tag{67}$$

with E_m, E_n, E_l, equal to the energy of the initial, final and intermediate virtual state, while $\boldsymbol{\mu}_{m(n)l} = \langle \Psi_{m(n)} | e\widetilde{\boldsymbol{r}_i} | \Psi_l \rangle$ is the electric dipole calculated between the initial/final and an intermediate/virtual (*l*) state. So, the scattering process is due to the

sum of virtual transitions to intermediate states. Conservation of energy is valid only globally, not for transitions to intermediate virtual states. The terms in square brackets represent the Raman scattering contributions of the *Stokes* and *anti-Stokes* scattering phenomena. In both processes, the presence of the electric field induces the transition which involve the absorption of a photon, which takes the system from an initial state |m> an intermediate (virtual) state |l>, which is followed by the process of emission of a photon that brings the system to a final state |n>.

In the case in which $\omega_{mn} = 0$, the initial and final state energy coincide, and the scattered radiation has the same frequency as the incident one (*Rayleigh* scattering). When $\omega_{mn} < 0$, the final state has lower energy than the initial one, an *anti-Stokes* photons are then emitted with higher energy than the incident one. Finally, if $\omega_{mn} > 0$ a Stokes photon is emitted with lower energy than the incident one.

4.3.3 *Selection rules*

The primary selection rule for a Raman transition is that the molecular polarizability must change during the molecular vibration. In the case of vibrational Raman spectra of diatomic molecules in a vibrational state ν, the specific selection rule is:

$$\Delta\nu = \pm 1$$

We would expect Raman lines to appear at distances from the exciting line corresponding to each active fundamental vibration. Here, $\Delta v = 1$ corresponds to Stokes lines and the $\Delta v = -1$ corresponds to Anti-Stokes lines.

In the case of rotational Raman spectroscopy, the condition for observing a Raman spectrum is that the polarizability of the molecule should change as the molecule rotates in an electric field. The rotational energy levels of linear molecules, i.e. N_2, O_2, and CO_2, in the vibrational ground state can be written as [117–119]:

$$E_J = BhcJ(J + 1) - DhcJ^2(J + 1)^2, \quad (68)$$

With J corresponding to the vibrational quantum number, B the rotational constant for the vibrational ground state and D the centrifugal distortion constant, *i.e.*:

$$B = \frac{h}{8\pi^2 c}\langle\frac{1}{I_0}\rangle \; ; D = \frac{4B^3}{\omega^2}$$

where ω is the wavenumber of the harmonic vibrational frequency of the molecule's vibrational ground state.

The energy difference between two rotational energy levels E_J and $E_{J'}$ can be written in terms of the photon energy variation $\Delta\nu$ as:

$$E_{J'} - E_J = hc\Delta\nu = hc(\nu_i - \nu_{J\to J'}) \qquad (69)$$

With ν_i the energy of the incoming photon (laser), and $\nu_{J\to J'}$ the Raman shifted outgoing photon.

Noteworthy, not all transitions between two different rotational state are allowed. The selection rules for transitions the between initial state *J* and final state *J'* can be derived starting from the assessment of the transition moment for rotational Raman scattering within an infinitesimal volume element dV as:

$$[\boldsymbol{P}]^{-J'-J} = \int \Psi_{J'} \boldsymbol{P} \Psi_J dV \qquad (70)$$

With Ψ_J and $\Psi_{J'}$ wavefunctions of states *J* and *J'* and **P** is the induced electric dipole moment, which is dependent to the polarizability tensor and hence to the molecular structure. By solving Eqn. 70, the following selection rule for Δ*J* is obtained: 0, ±2. The Δ*J* = 0 corresponds to *Rayleigh* line and represents no change in the molecular energy (Q branch), while the Δ*J* = +2 (S branch) and Δ*J* = −2 (O branch) corresponds to the *Stokes* and *Anti-Stokes* line, respectively. Combining the obtained results with Eqns. 68 and 69, the rotational Raman shifted photon energies can be figured out:

$$\nu_{J\to J'=J+2} = \nu_i - 4B\left(J + \frac{3}{2}\right) + 6D\left(J + \frac{3}{2}\right)\left[1 + \frac{8}{6}\left(J + \frac{3}{2}\right)^2\right]\text{Stokes} \qquad (71)$$

$$\nu_{J\to J'=J-2} = \nu_i + 4B\left(J + \frac{3}{2}\right) - 6D\left(J + \frac{3}{2}\right)\left[1 + \frac{8}{6}\left(J + \frac{3}{2}\right)^2\right]\text{Anti-Stokes,} \qquad (72)$$

with J=0, 1, 2, 3, 4,…N. For small J values and neglecting the second-order term in J from both Eqns. 71 and 72, the wavenumbers of the Raman rotational scattered radiation can be written as:

$\nu_{J\to J'} = \nu_0 = \nu_i - 6B$ ($J = 0$) Stokes $\qquad \nu_{J\to J'} = \nu_2 = \nu_i + 6B$ Anti-Stokes

$\nu_{J\to J'} = \nu_1 = \nu_i - 10B$ ($J = 1$) Stokes $\qquad \nu_{J\to J'} = \nu_3 = \nu_i + 10B$ Anti-Stokes

$\nu_{J\to J'} = \nu_2 = \nu_i - 14B$ ($J = 2$) Stokes $\qquad \nu_{J\to J'} = \nu_4 = \nu_i + 14B$ Anti-Stokes

In particular, 4B is the spacing between the Stokes and anti-Stokes lines while the first lines from Stokes and Anti-Stokes branches are spaced with 6B relative to *Rayleigh* line (see Figure 33).

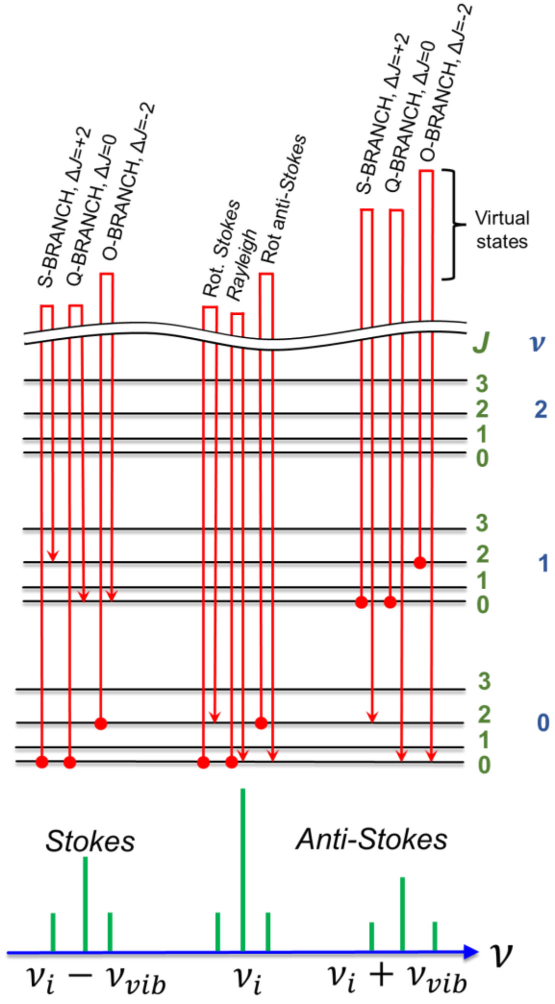


Figure 33: *Roto-vibrational Raman features with the S, Q and O branch indicated.*

4.3.4 *Raman experiment*

Micro-Raman spectra were collected through a confocal microscope NT-MDT NTEGRA Spectra working in reflection mode. We used a solid state DPSS laser working at 532 nm (Nd:YAG laser) as excitation source limiting the maximum power to ~ 400 μW to prevent any displacement of the Stokes peak due to the temperature increasing. An IDUS type Andor CCD camera cooled with a triple Peltier stage was used as detector. For the purpose of this study, the 500-600 cm^{-1} spectral range was investigated with a resolution < 1 cm^{-1}. A 100X objective with a working-distance of 6 mm and a numerical aperture of 0.75 was used to focalize the laser beam on the surface of the sample with a spot size of ~350 nm. All measurements were carried out in backscattering geometry, using the microscope objective to collect the scattered light.

CHAPTER 5
RESULTS AND DISCUSSION

5.1 **Defect identification in Metal-Oxide-Metal (MOM) Capacitors for Integrated Circuits (ICs) through thermal characterization**

In this chapter, the results achieved through the application of a novel approach based on thermal analysis for the identification of defects in Metal-Oxide-Metal (MOM) capacitors for integrated circuits (ICs) found through inline inspection are reported. The aim is to identify critical devices by means of electrical parameters starting from the analysis of those that showed an unusual defect during in-line optical inspections. In order to analyse the structural and reliability issues of the MOM component, a dedicated wafers specifically designed named as *test pattern,* were used, characterised by the unique presence of multiple MOM components that can be used to evaluate both defect and electrical issues.

Before discussing the obtained results, a preliminary multi-techniques analysis is required in order to properly correlate the possible "*fail*" or "*good*" device with the presence of specific defects of different nature found though the employment of the novel approach.

5.1.1 Methodologies for preliminary characterization

Generally speaking, optical and scanning electron microscopy (OM and SEM, respectively) represent well-established approaches for the evaluation of defect localization in semiconductor devices. In particular, OM allows to detect the defects on the metal surface. Buried defects can be observed too but only inside the oxide layers as they are almost transparent. In any case, the OM resolution is intrinsically limited due to the diffraction of visible light if no special tricks are used. Being defects of interest (DOI) in MOM capacitors of the order of 1-2 µm, shape and conformation cannot be easily determined through OM analyses, due to intrinsic limitations of the

used probe. High-resolution images can be obtained by using SEM, allowing the observation of defects/particles having dimensions down to tens of nanometres. A common SEM inspection system for ICs applications is developed in such a way to review and classify defects on a processed silicon wafer. Undesirable metallic or polymeric components are magnified thanks to a post-processing analysis which involves the use of at least two different images, one associated to the defect-containing die and one used as reference. This approach become mandatory since defect locations in semiconductor devices cannot always be accomplished by using the image position information alone, due to different errors affecting each measurement (see Figure 34).

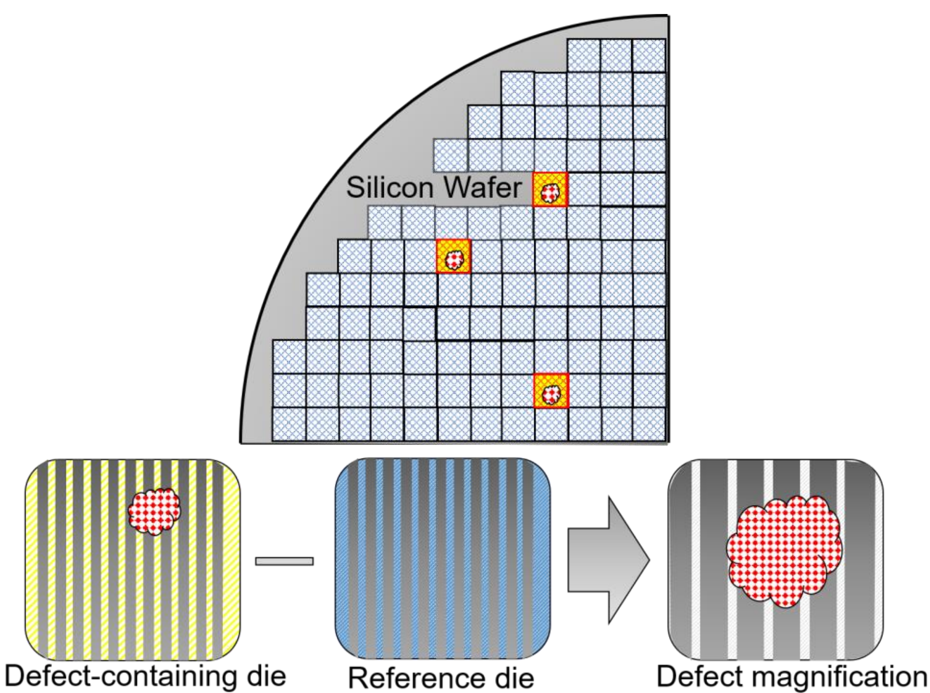


Figure 34: *Example of defect magnification obtained by post-processing analysis involving the use of two die with and without a defect.*

The main limitation of such technique relies in the fact that information is limited to the superficial layer of the investigated material. Hence, small impurities located at the bottom of the metal layer and/or embedded within the strips of the MOM capacitor are extremely difficult to detect/characterize. However, depending on their dimension, such in-depth impurities can affect the overlying surface, resulting in a detectable

superficial inhomogeneity. Moreover, underlying defects, having dimension less than the distance between two adjacent strips, and localized at different focal planes, do not provide sufficient optical signal to be revealed. In this case, such impurities can still be screened through electrical tests.

An example of the methodology used to identify a critical defect from a reliability point of view, involved the use of special devices, known as *test patterns*, which allow to enhance the impact of production processes on specific structures.

Such devices are characterized by the following features:

- they only execute partial steps of the production flow, thus the time required to produce wafer is significantly reduced;
- the only relevant sections of the device are designed;
- can be electrically stressed to study the presence of contaminants;
- correlations can be made between defects and electrical tests.

In the case of the MOM structure, a *test pattern* characterised by the presence of only MOM components can be used. In particular, each device consists of 4 regions called *giants* (G1, G2, G3 and G4), which means that the equivalent area of the MOM, with respect to standard device, is approximately 4 times greater (see Figure 35).

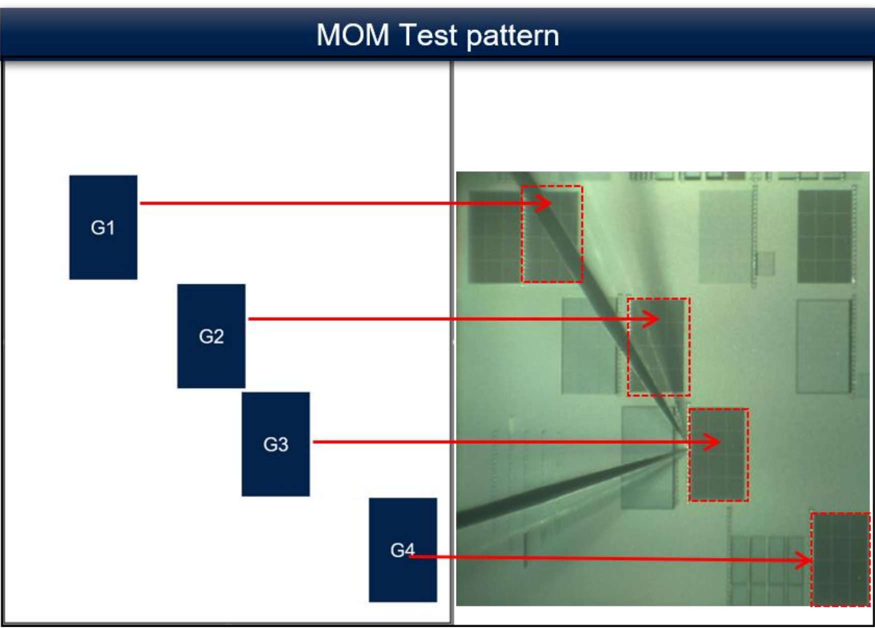


Figure 35: *Representation of a typical test pattern device for MOM component and corresponding image with the position of the giants indicated.*

Specifically, starting from the optical inspection at metal etch step of two "*test pattern*" wafers, called TP1 and TP2, all defects were highlighted (see Figure 36).

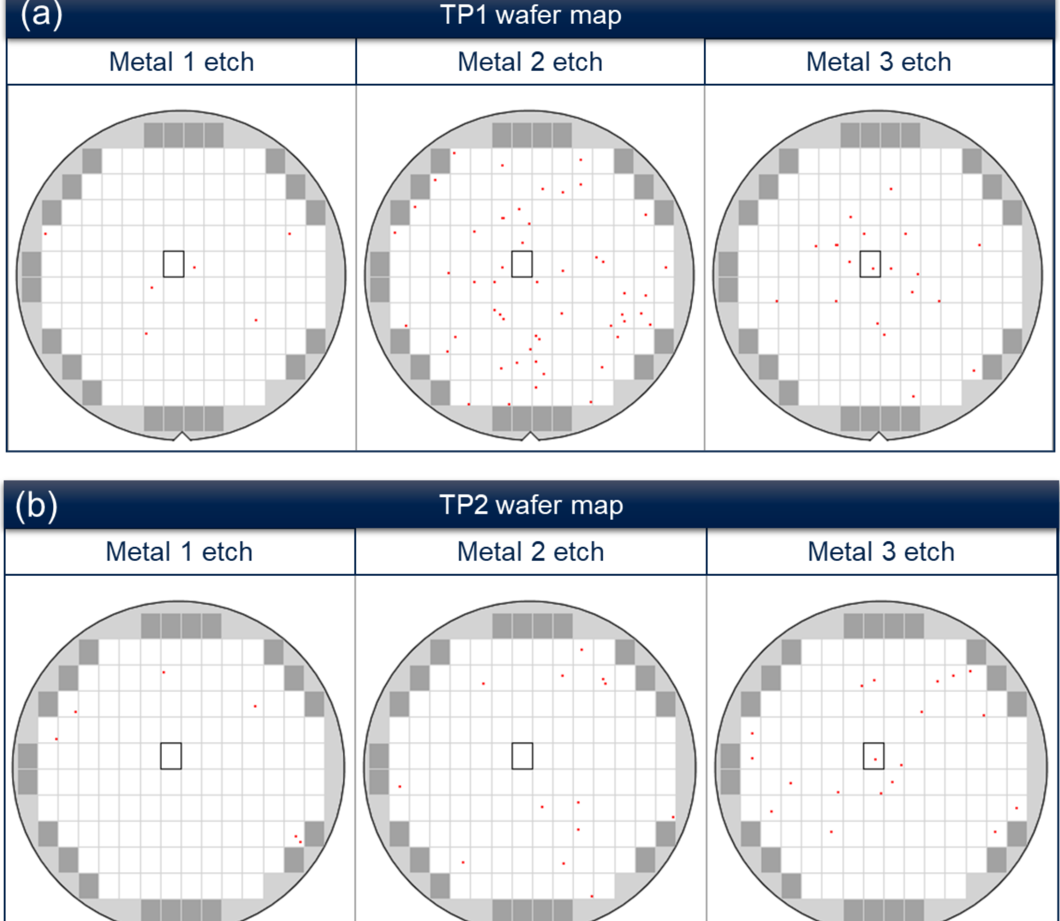


Figure 36: *Defects location (red dots) detected by optical microscopy in (a) TP1 and (b) TP2 wafers, respectively.*

Subsequently, a SEM review is required on the same locations to process the obtained images. In most wafer manufacturing plants, the defect classification process depends on manual human review. Operators generally separate defects into a few known and defined categories with a not negligible consumption of resources and time. The result is often inaccurate, and non-uniform, as it is influenced by the operator's own perception [120]. The evolution of automated analysis techniques, such as automatic defect classification (ADC), is an alternative solution to manual

classification, providing much more accurate, robust, uniform, and instantaneous data. In recent years, the development of deep learning algorithms has improved the computing power of the GPU and enabled the development of the convolutional neural network (CNN). Deep learning allows multi-layer neural networks to automatically extract and learn target features through layers of abstraction, and to properly detect target objects from images. The model is divided into 3 different parts, *i.e.* classification, detection, and segmentation network. The classification network extracts the characteristic information of the target object in the input image through a series of operations such as convolution [121] and pooling [122]. Then it passes through the fully connected layer capable to classify according to the preset label category settings. The network model is shown in Figure 37. The target detection network not only classifies the target object, but also identifies its location. Finally, the segmentation networks perform pixel-level segmentation of the regions of interest in the input images [123]. During the training phase, each of the labelled images is provided as input and the CNN is expected to provide the correct label. The entire training phase can take a long time, depending on the value set for the number of epochs or the convergence threshold.

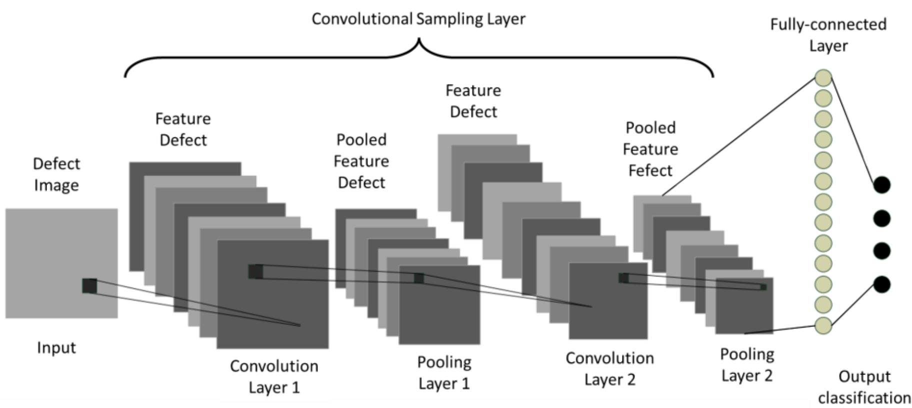
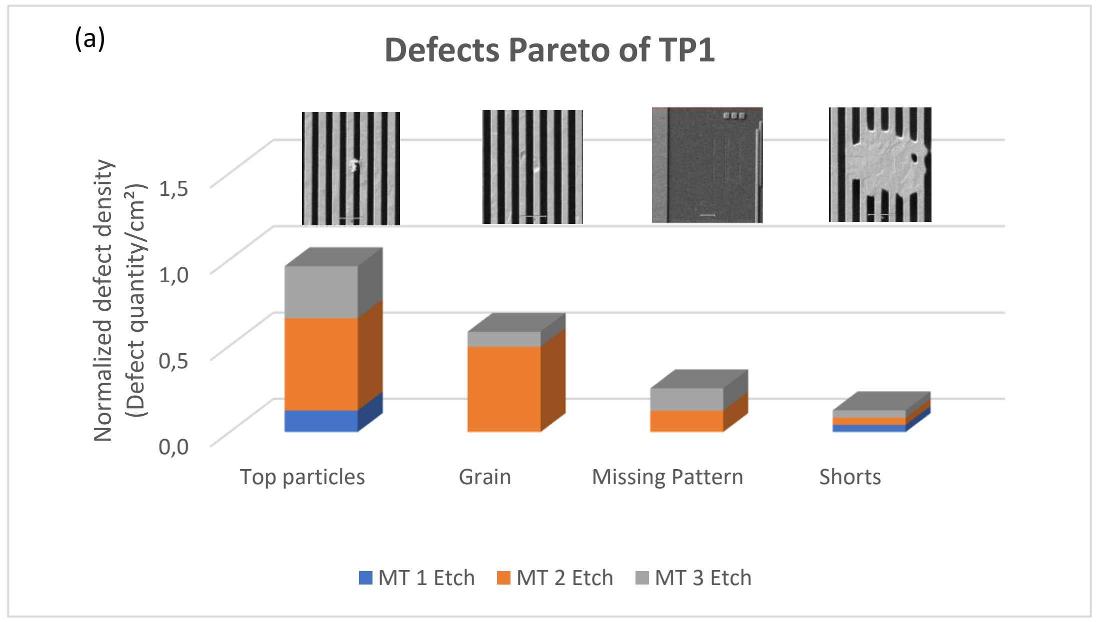


Figure 37: *Classification network model structure diagram.*

The methodology used to classify TP1 and TP2 wafers is based on the ADC, using machine learning algorithms based on the CNN architecture.

Taking advantage of this method, the detected defect types are shown in Figure 38. By looking at Figure 38, considerable difference between the Pareto of TP1 and TP2,

both in terms of quality (defect classes) and quantity, can be observed. Since both wafers underwent the same production processes and were processed with the same equipment, it can be assumed that the observed differences are caused by typical variations in the production process.



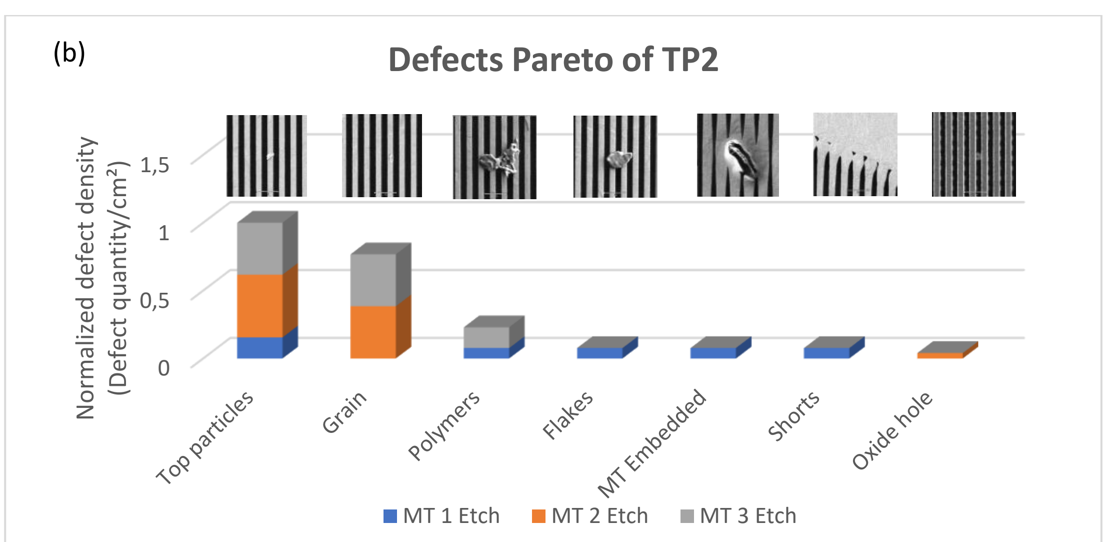


Figure 38: *Normalized defect density respect to defect classes for (a) TP1 and (b) TP2 wafers, respectively.*

In this work, "*top particles*" refers to defects that have a size ≤3 µm, conversely, particles that have a superior dimension are classified as "*flakes*". Both such classes

include different types of defects consisting of metallic and non-metallic elements such as aluminium, titanium, tungsten, silicon and oxide. The carbon defects fall into the "*polymers*" class and are generally originated by the coating removal. In both Figure 38a,b, the second bar accounts for the "*grain*" class, these defects are intrinsic to the metal growth process and are not electrically relevant. On the other hand, the defects that are generally intercepted by the standard electrical tests are: the "*MT embedded*" which are macroscopic defects embedded in the metallisation layer, "*shorts*" resulting from wrong metal pattern definition, "*missing patterns*" which means areas without the metallisation layer and "*oxide hole*", generally introduced during the pre/inter-metal oxide deposition process (PMD/IMD).

Considering the size and nature of the defects that fall into the *top particles* class, it can be concluded that such class is the most critical in terms of reliability.

To visualise the defects of interest and their wafer position regardless of the inspection (after MT1, MT2, MT3 etch) steps, a staked defectivity map is reported in Figure 39 referring to TP1 and TP2 wafers where the dice of interest are highlighted.

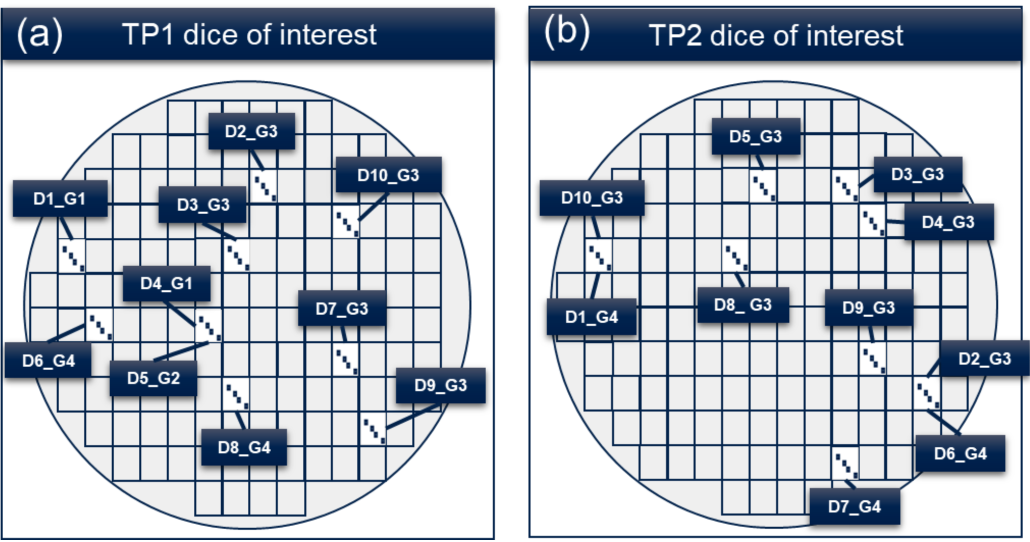


Figure 39: *Defective dice of interest is reported in figure for both TP1 (a) and TP2 (b), respectively.*

In the following table (Table 3) the position in the die and the relative defect image is reported for TP1 and TP2, respectively. The last listed sites represent the reference, which means that no defects were detected during in-line inspections in such locations.

Table 3: *Defect of interest are shown considering their position in the die and the relative defect image for both TP1 and TP2.*

TP1 defect location	TP1 Defect Image	TP2 defect location	TP2 Defect Image
TP1_D1_G1		TP2_D1_G4	
TP1_D2_G3		TP2_D2_G3	
TP1_D3_G3		TP2_D3_G3	
TP1_D4_G1		TP2_D4_G3	
TP1_D5_G2		TP2_D5_G3	
TP1_D6_G4		TP2_D6_G4	
TP1_D7_G3		TP2_D7_G4	
TP1_D8_G4		TP2_D8_G3	Reference
TP1_D9_G3		TP2_D9_G3	Reference
TP1_D10_G3	Reference	TP2_D10_G3	Reference

In this context, the most relevant defects are the "top particles" that can be more or less critical depending on the area of the die where they lie.

After knowing the location of the most interesting defects, preliminary electrical measurements were made in order to identify fail (already shorted), good and leakage devices. To study the performance and quality of a capacitor module, it needs to carry out specific tests suitable to measure some main electrical parameters. Among them, the current-voltage characteristic is of paramount importance, since it allows the main operating points of the device to be determined quickly and efficiently. The method used to trace the I-V curve involves the application of potentials ranging from 1 to 150 V for an extremely short period of time, in the order of 2 minutes. Such measurements were performed at the laboratories of *ST Microelectronics S.r.l.* in Catania site.

In Figure 40, the Current-voltage (I-V) plots for TP1 and TP2 for all the sites reported in Table 3, are shown.

Taking into account the results obtained from I-V measurements, the MOM component is considered non-critical if the current does not exceed 10 nA, for voltages that are in the range between 1 – 150 V.

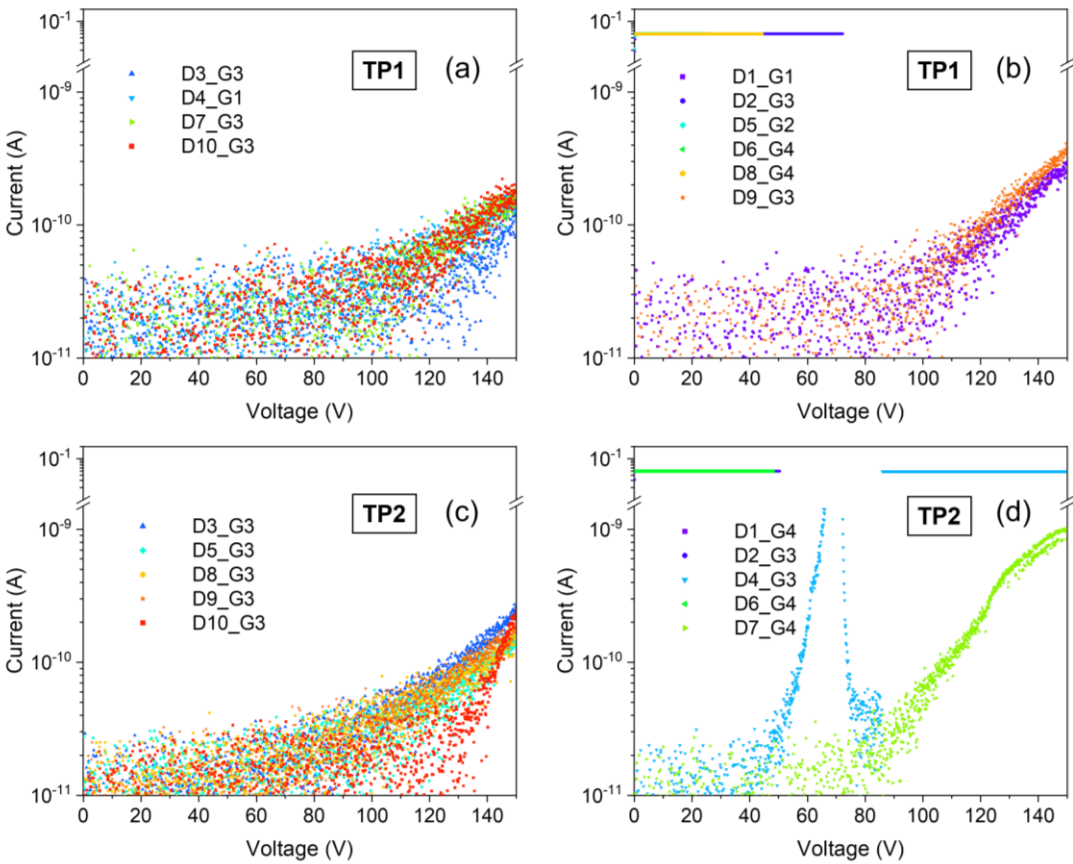


Figure 40: *Current-voltage (I-V) plots for (a, b) TP1 and (c, d) TP2 wafers, respectively. More in detail, panels (a, c) report the I-V plots related to working dice, while in panel (b, d) the I-V plots of leakage and fail ones.*

From a first inspection of the Figure 40, it is possible to gather the results into two different groups, i.e. devices that show a standard I-V trend, (Figure 40a and c), and devices that exhibit anomalous I-V behaviour, (Figure 40b and d).

The I-V plots observed in the case of working dice (Figure 40a, c) show current values which do not exceed the nominal product specification in terms of electrical characteristic (10 nA up to 150 V). In particular, the standard trends observed in the case of reference dice, *i.e.* D10_G3 for TP1 and D8_G3, D9_G3 and D10_G3 for TP2

were, in a way, expected considering that no physical defects were seen from the in-line inspection. Contrarily, for D3_G3, D4_G4 and D7_G3 within TP1 as well as for D3_G3 and D5_G3 within TP2, the I-V behaviour seems to be not affected by the presence of a physical defect since, even in these cases, the measured current values do not exceed the nominal threshold for voltages up 150 V. Such evidence constitutes the real limitation of the standard electrical tests in the assessment of faulty devices which could yield to serious reliability issues.

Going on, the I-V plots shown in Figure 40b,d, in the case of D2_G3, D5_G2, D6_G4, D8_G4 for TP1 and D1_G4, D2_G3, D6_G4 for TP2 exhibit a constant value of the current of 0,045 A, 9 order of magnitude higher than the current threshold set for working dice, as expected in the case of short-circuited state. In fact, defects seen during the in-line inspection for the aforementioned locations (see Table 3), are such that they 'join' (short-circuits) two metal strips of the MOM capacitor structure, thus preventing its correct operation. Finally, devices D1_G1 and D9_G3 for TP1 (Figure 40b) exhibit anomalous trends related to the leakage current passing through the device. Such signal can be the precursor of a reliability failure, even if the current is still below 10 nA. Indeed, reliability defects often pass electrical tests without showing any anomalous signals or, at most, by differing by small values from the threshold one. This is the case of D1_G1 and D9_G3, whose I-V plots revealed higher values of current of approximately ~ 80 % (relative variation at V = 150) with respect to those observed in Figure 40a, b. Meanwhile, devices D4_G3, D7_G4 for TP2 (Figure 40d) show, respectively, a current peak up to 2,8 x 10^{-8} A at 71 V followed by a constant trend of I (0,045 A) for $90 < V < 150$, while the D7_G4 sample reaches a maximum current of 10^{-9} A at 150 V, one order of magnitude higher than the threshold value.

5.1.2 *Thermal characterization measurements*

The thermal characterization was conducted on all devices reported in Table 3 with the aim to establish an alternative approach to evaluate the presence of defects in MOM-based devices. Results were then compared to those achieved by the I-V curves carried out at the laboratories of the *STMicroelectronics S.r.l.* in Catania site reported in the previous section.

The effectiveness of the home-made thermal characterization setup (see section 4.2) employed in this thesis was first verified through the collection of measurements on the reference dice, *i.e.* D10_G3 for TP1 and D8_G3, D9_G3 and D10_G3 for TP2, characterized by no physical defects as seen from the in-line inspection, and on some of the metal-short ones, i.e. D2_G3, D5_G2, D8_G4 for TP1 and D2_G3 for TP2. In particular, Figure 41 reports, as example, the thermal maps acquired for the D10_G3 reference sample taken, respectively, prior and after the application of a power signal. The obtained thermal maps revealed an almost comparable thermal signature, characterized by the absence of any hot-spots indicating that the current flow did not locally overheat the device, thus confirming the absence of any anomalous working condition, as expected. Same behaviour can be observed for the remaining reference sites (D8_G3, D9_G3 and D10_G3).

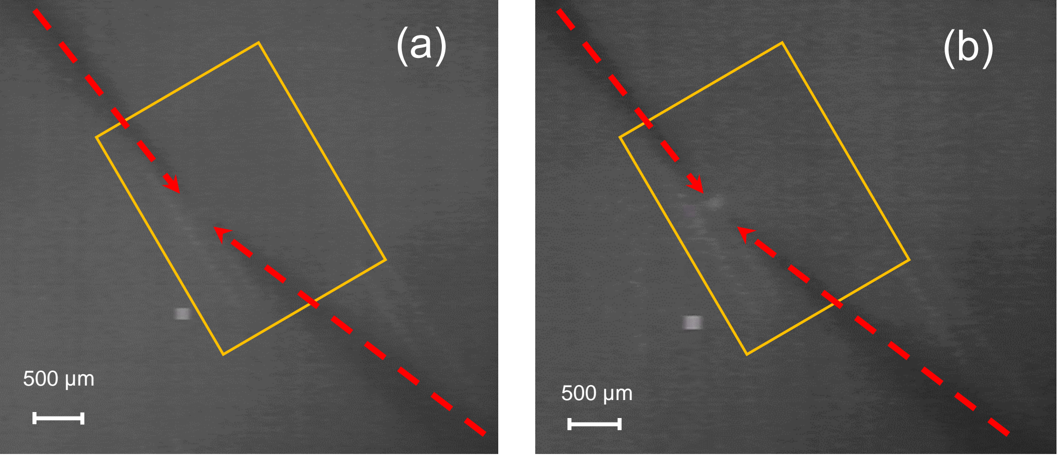


Figure 41: *Thermal maps acquired for D10_G3 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

Going on, with the aim to highlight the device thermal response in presence of a known defect, Figure 42, Figure 43, Figure 44, Figure 45 report the thermal maps acquired for metal-short sites taken, respectively, when the device is not subjected to any stress, on the left, and when a 30 MHz alternating power signal is applied, on the right. In all samples the local temperature increases, as highlighted by the "white" region indicating a higher infrared emission intensity along one or more specific "lines" of the device.

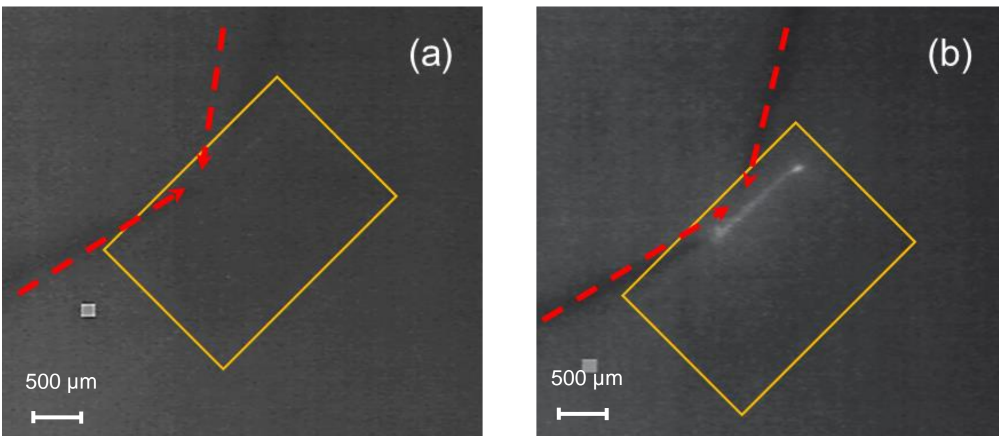


Figure 42: *Thermal maps acquired for D2_G3 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

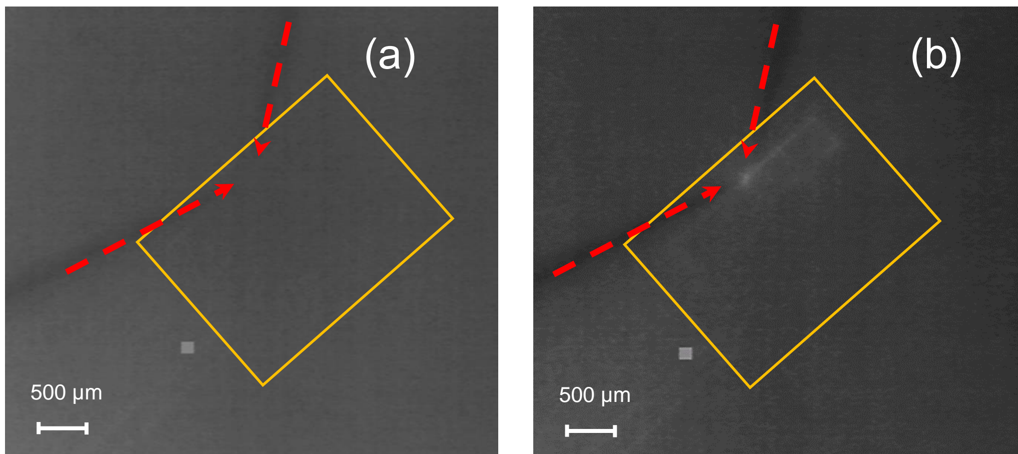


Figure 43: *Thermal maps acquired for D5_G2 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

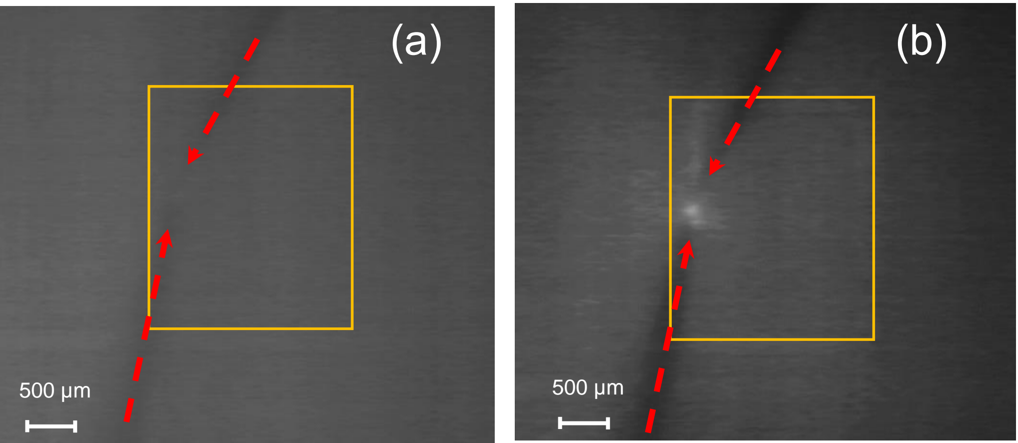


Figure 44: *Thermal maps acquired for D8_G4 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

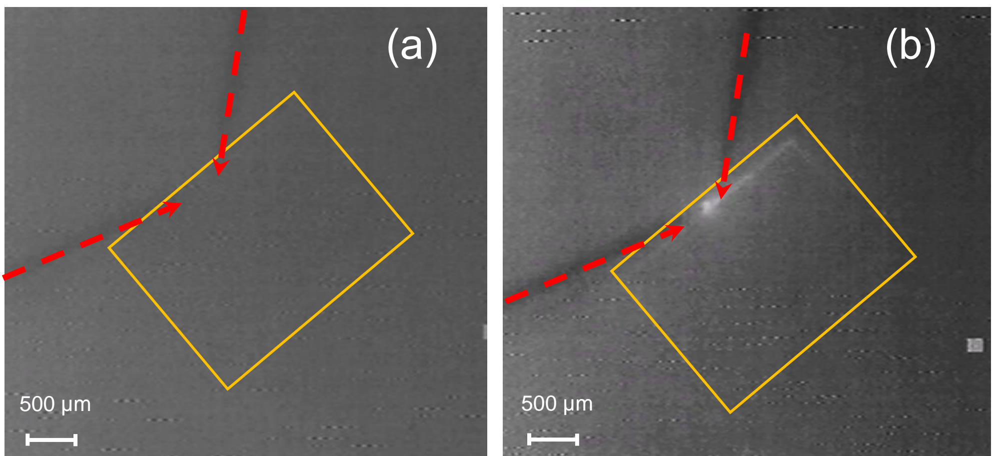


Figure 45: *Thermal maps acquired for D2_G3 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

After the thermal characterization of “good” and “fail” reference sites, the analysis involved the acquisition of thermal maps on the remaining 12 sites in both TP1 and TP2 (see Table 3). In the case of site D6_G4 for TP1 and D1_G4, D6_G4 for TP2 (Figure 46,Figure 47, Figure 48), which exhibited, through I-V analysis, a current value 9 orders of magnitude higher than the current threshold set for the working dice, thermal maps showed an increase in temperature quite similar to those observed for devices with a short metal, proving that physical defects can be considered as responsible of the onset of localized high thermal emission regions.

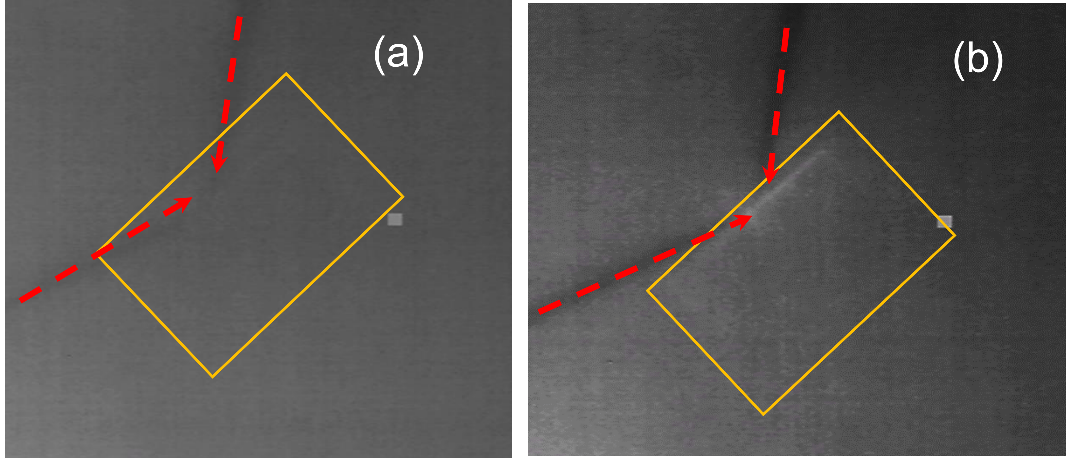


Figure 46: *Thermal maps acquired for D6_G4 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

It can therefore be concluded that the above devices are not working due to the presence of a defect that joining two metal strips thus producing an effect similar to the short.

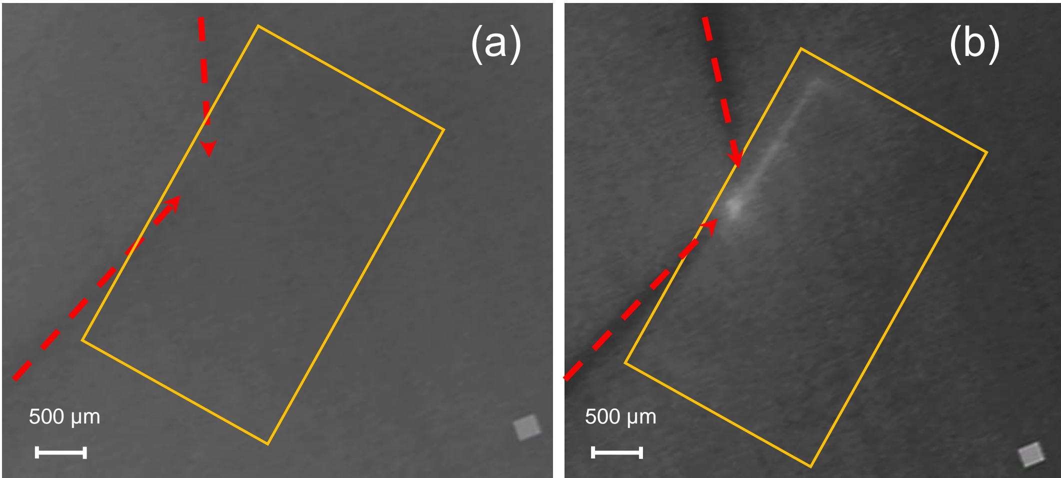


Figure 47: *Thermal maps acquired for D1_G4 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

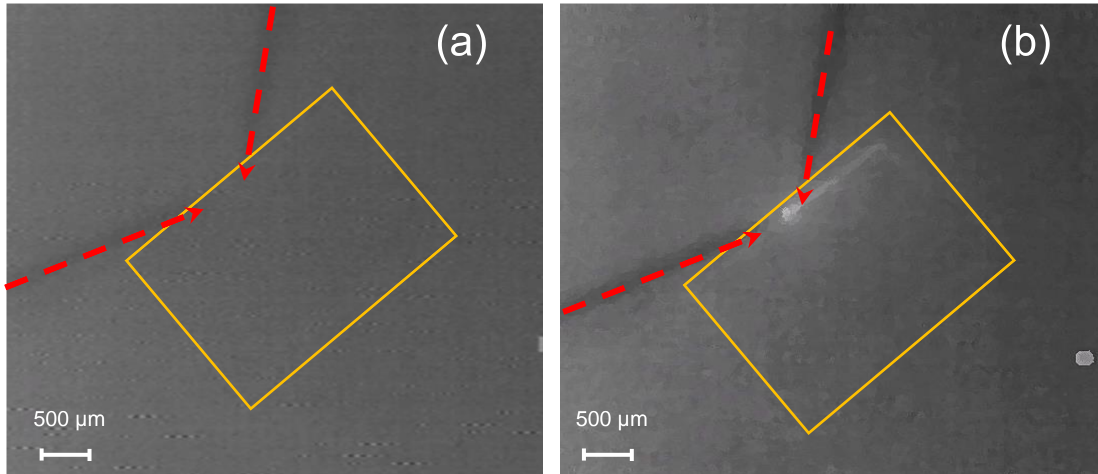


Figure 48: *Thermal maps acquired for D6_G4 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

A different discussion for the devices that showed an anomalous leakage during the I-V analysis, namely, D1_G1 and D9_G3 for TP1 and D4_G3, D7_G4 for TP2 is required. In particular, in the case of D1_G1 (Figure 49) and D9_G3 (Figure 49, Figure 50) for TP1, a weak temperature increase can be observed at the pad/tip contact (for D1_G1) and at the pads on the left perimeter (for D9_G3) of the dice. This behaviour is in agreement with what has been observed during the I-V analysis, since the

measured current values were found to slightly deviate from the nominal value; similarly, the local temperature variations observed are slightly prominent with respect to the almost negligible thermal activation characteristic of the good/reference samples.

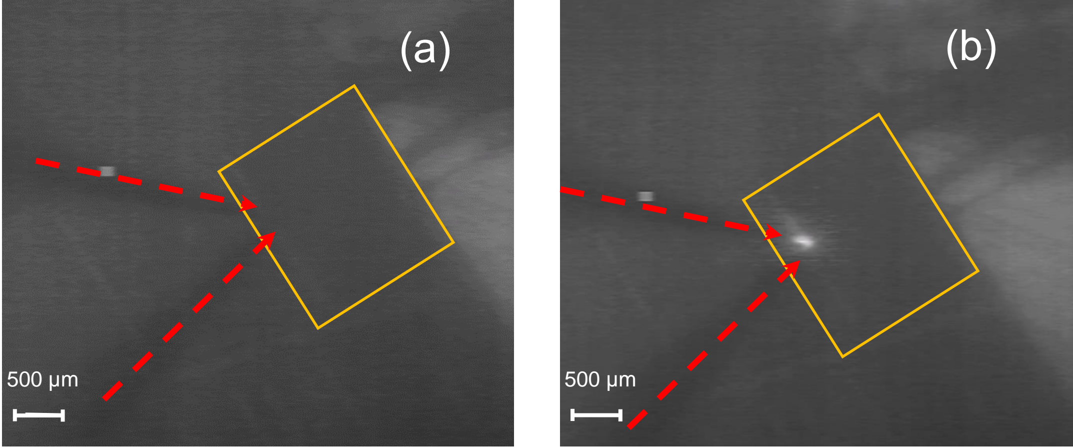


Figure 49: *Thermal maps acquired for D1_G1 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

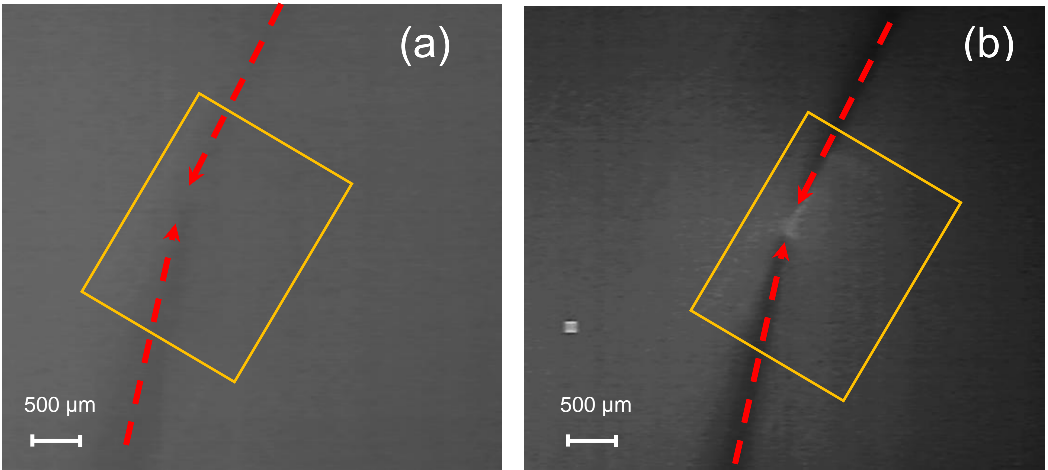


Figure 50: *Thermal maps acquired for D9_G3 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

More interesting results were achieved for site D4_G3 and D7_G4 for TP2, showing a significant temperature variation following alternative continuous wave (CW). In particular, Figure 51 reports, as example, the thermal map collected for D4_G3 which revealed a significant overheating along the entire device indicative, on one side, of the existence of defects which locally compromise the MOM functioning and, on the other side, of the activation of temperature-susceptible phenomena. The outcome of such processes can be more clearly visible in Figure 52, reporting a picture of the device after thermal characterisation, where several burns can be observed in different points of the die.

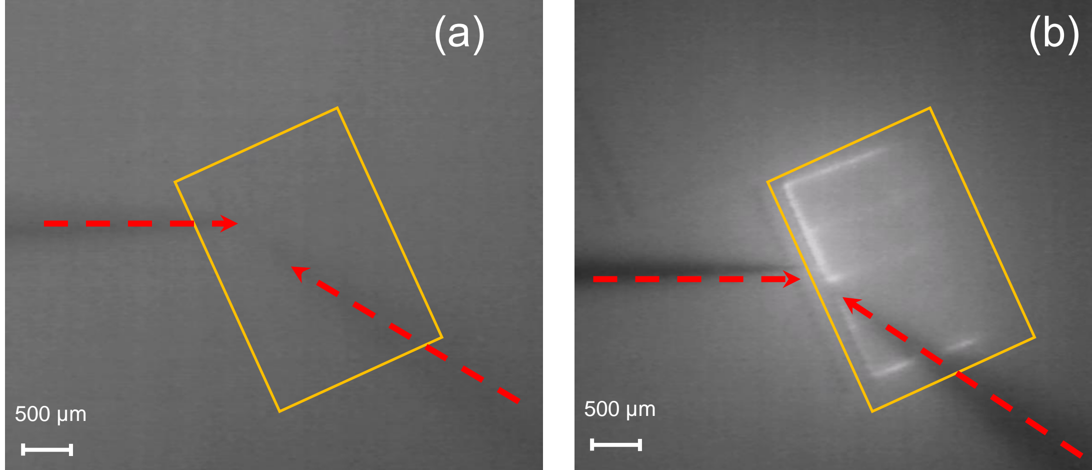


Figure 51: *Thermal maps acquired for D4_G3 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

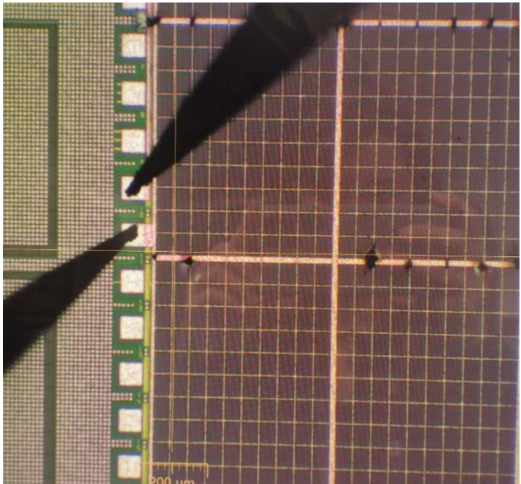


Figure 52: *Optical image of D4_G3 site for TP2 after thermal analysis.*

As can be seen from Figure 53 the D7_G4 for TP2 device also showed overheating in several points, so it is possible to conclude that the defect inside the device has compromised the operation of the entire die.

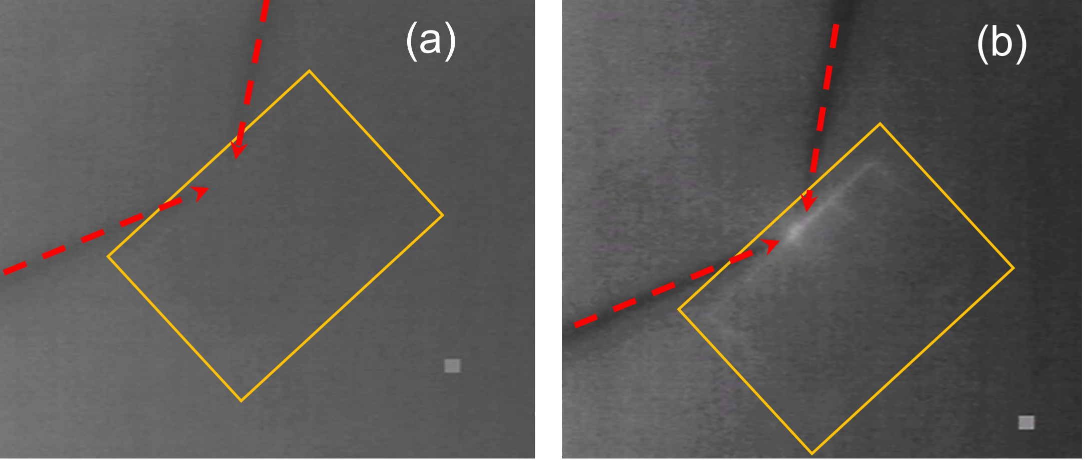


Figure 53: *Thermal maps acquired for D7_G4 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

Finally, a comment must be made for all devices that did not show any unusual signals during the I-V measurements but for which a physical defect during in-line inspections was found (D3_G3, D4_G1, D7_G3 for TP1 and in D3_G3, D5_G3 for TP2). Generally speaking, with the exception of D7_G3 for TP1, all the other sites did not register any local overheating upon the application of alternative continuous wave (CW). Figure 54, Figure 55, Figure 56, show the thermal images for each device examined taken, respectively, when the device is not subjected to any stress and when a 30 MHz alternating power signal is applied. By looking at the images of the defects (Table 3) seen in-line in D3_G3 and D4_G1 for TP1 and in D3_G3 for TP2, it can be seen that the particles place in contact two or more metal strips generating, in theory, a short. However, this phenomenon occurs if and only if these particles are conductive in nature. In the case of polymer defects, for example, no effect is expected from a

reliability point of view. It can therefore be concluded that the defects found during the in-line inspection are not failures.

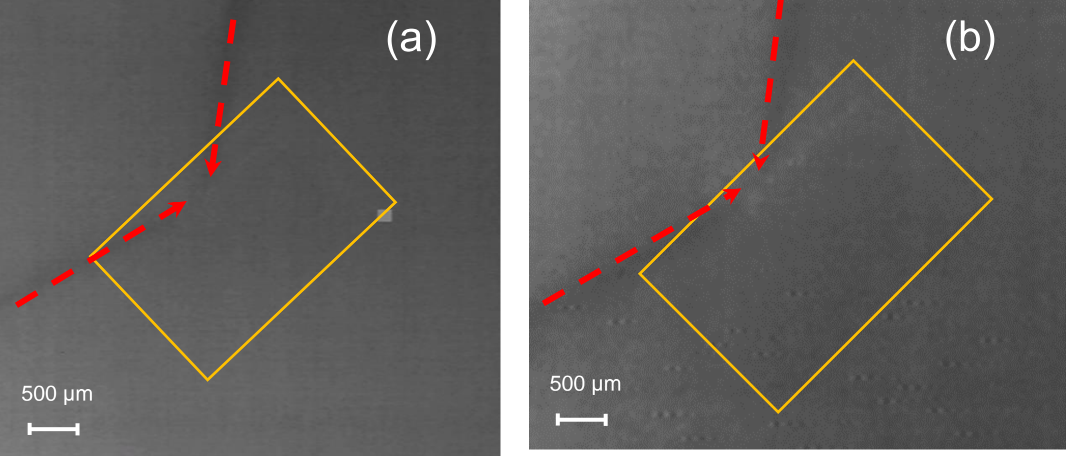


Figure 54: *Thermal maps acquired for D3_G3 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

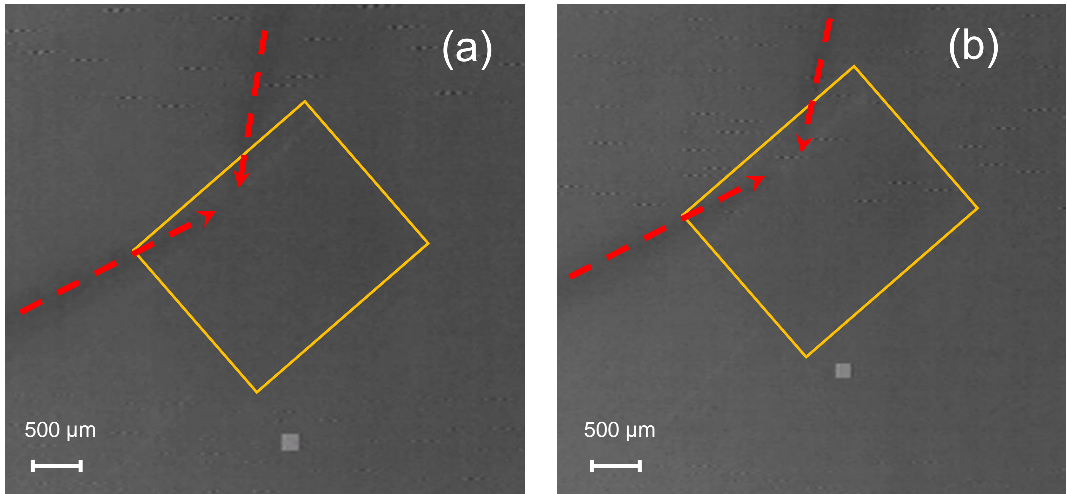


Figure 55: *Thermal maps acquired for D4_G1 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

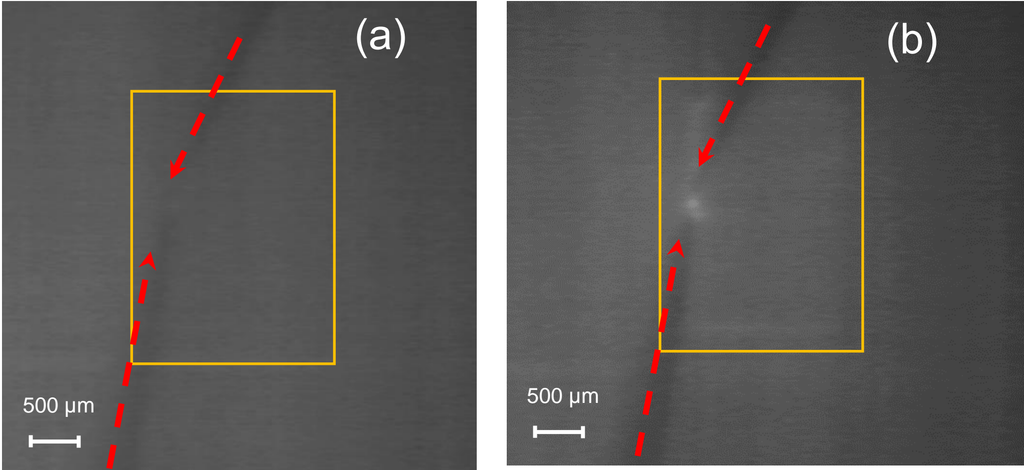


Figure 56: *Thermal maps acquired for D3_G3 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

Figure 57 shows the collected thermal map for D5_G3 site for TP2, respectively, prior and after the application of a power signal. In this case, no local temperature increase can be observed. In fact, by looking at the corresponding optical image reported in Table 3, an extremely small particle of about 0.28 µm is localized just above one metal strip, therefore, it does not constitute a reliability risk.

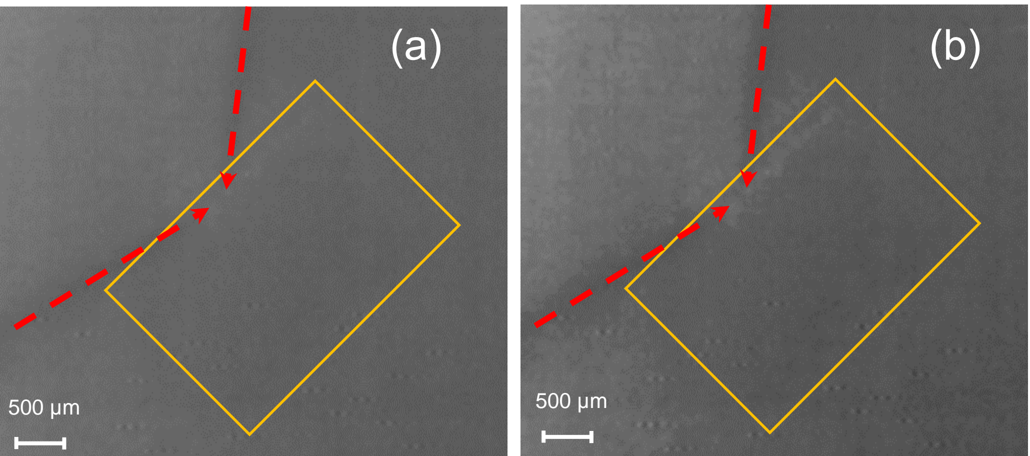


Figure 57: *Thermal maps acquired for D5_G3 in TP2 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

A different discussion must be made for D7_G3 site of TP1: while the defect characteristics observed during the in-line inspection (refer to Table 3) closely resemble those described for D5_G3 of TP2, a distinctive point arises during the thermal analyses. The device experienced overheating at multiple locations, exhibiting a behaviour strikingly similar to that observed in cases of metal shorts. According to the results obtained up to now, this behaviour cannot be explained by the presence of the defect observed during the optical inspections in MT1/2/3, but is to be found elsewhere. In fact, it is worth noting that the optical inspections performed are not fully exhaustive and do not reveal all the defects present on the wafers. In particular, it is not possible to detect little defects within the oxide or metal layers, so it is reasonable to assume that this device is affected by a defect of a different nature that was not intercepted by the optical inspections performed for this work and is not visible through the conventional I-V analysis. Therefore, such device constitutes an example of what happens when there is a reliability defect. In this case, however, the defect was intercepted by means of thermal characterisation.

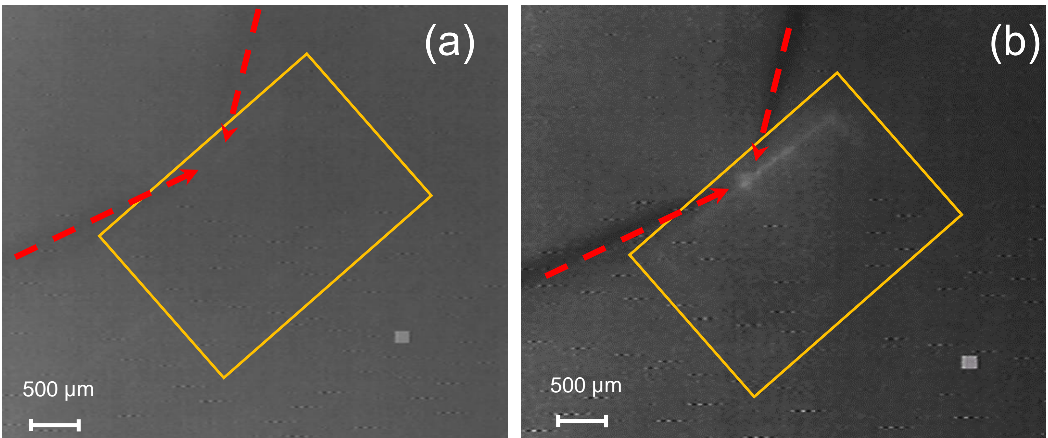


Figure 58: *Thermal maps acquired for D7_G3 in TP1 sample collected (a) prior and (b) after the application of a power signal. The orange line account the DUT perimeter while the red-dashed arrows point out the direction of the used tips.*

In conclusion, thermal analyses were carried out on all samples identified by visual inspection. A preliminary analysis of current as a function of DC voltage was performed to simulate real testing conditions where some non-functional devices may

pass the electrical test without been suppressed. With the aim to overcome such limitation, a home-made thermal characterisation technique was developed based on the evaluation of the thermal emission upon the application of a power signal at 30 MHz in AC. A preliminary validation phase was undertaken by collecting thermal maps on both “good” and “fail” sites as individuated in-line inspection and I-V analysis, to *calibrate* the setup and provide necessary references for data evaluation. Then, measurements were conducted on the remaining devices, which in most cases showed consistent results with respect to those achieved through the I-V analysis. On the other hand, the D7_G3 site for TP1 exhibit unexpected behaviour, probably due to a defect not seen during the in-line inspections and not detected through I-V analysis. In this case, the thermal characterization played a key role in defect detection for reliability purposes, proving to be a reliable and efficient approach to quickly assess the device functionality. However, the employed experimental parameters do not allow the precise localization of the defect for which frequencies of the order of GHz should be required. Finally, in order to industrialize such process, it is essential to increase the statistical sample size, and it would be useful to run tests on "finished" devices rather than *test pattern.*

Considering that the applications of MOM capacitor-based devices vary depending on their specific use and design, ranging from high-frequency and power electronics to automotive control systems, the necessity for robust and reliable techniques turns out to be fundamental for compensate the unreliable outputs provided by conventional electrical tests. This is the purpose the developing of an innovative protocol based on the evaluation of thermal maps to discriminate the correct functioning of MOM components, was proved to be an efficient method for the assessment of reliability issues.

5.2 **Stress-Induced Frequency Shifts in Gallium Nitride (GaN) Devices Probed by Micro-Raman Spectroscopy**

The engineering of high-quality Gallium Nitride (GaN) semiconductors for power devices has gained, only in recent years, considerable attention by the scientific community. This is due not only to their unique structural properties and higher electrical performances with respect to standard silicon-based technologies, but also

to their increasing demand/attention in the automotive, renewable energies and aerospace industries. Monitoring the internal stresses occurring in GaN crystals allows the development of high-quality substrates which positively affect the yield of the final device. In this sense, micro-Raman spectroscopy proved to be a valuable tool for the evolution of localized residual stresses inside GaN substrates, starting from the analysis of the frequency shifts exhibited by specific spectral features upon mechanical perturbation. In this study, the variation of the A_1(TO), E_1(TO) and E_2(high) peaks in a GaN epitaxy layer, grown on 6" n-Si(111) substrate, was evaluated following the application of a uniaxial tensile stress. The correlation between the applied stress and Raman shift for each contribution was properly quantified using an in-house three-point mechanical configuration, revealing a diminishing of the corresponding frequencies with respect to those calculated in a stress-free material (used as reference). The proposed methodology could, in principle, be implemented in large-scale semiconductor industrial processes with the aim to assess the quality of GaN substates, prior the "growth" of the final device.

In the development of power electronic and optoelectronic devices based on GaN technology, one of the main challenges is represented by the epitaxial growth of GaN semiconductors, due to the high cost and small size of the crystals itself. For this reason, a suitable substrate must be chosen [124]. Nowadays, commonly employed substrates are sapphire (Al_2O_3), silicon carbide (SiC) and silicon (Si) [73]. In the case of sapphire and SiC, high amount of crystallographic defects are introduced within the GaN crystal lattice during the epitaxy process. This aspect, together with the high costs and possibility to produce only small-sized wafers, led to a massive use of Si-based substrates in the industrial production. Unfortunately, the presence of a not-negligible lattice mismatch between the GaN(0001) and Si(111) (-17%) layers (see Figure 59) leads to high dislocation density (up to 109 cm^{-2}) within the material, negatively affecting the quality of the active area. In addition, the aforementioned lattice mismatch causes the occurrence of a measurable residual-strain at the GaN/Si interface, which propagate along the device [49].

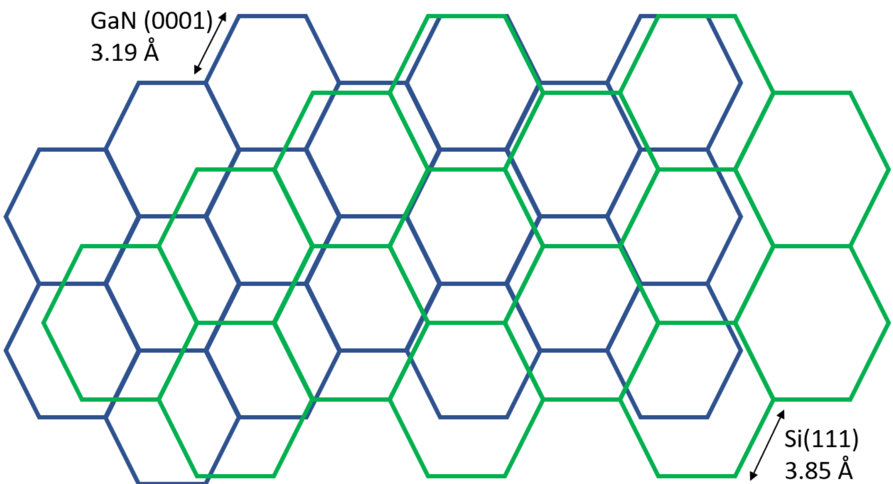


Figure 59: *Representation of the reticular mismatch at the GaN-on-Si interface. GaN(0001) reticular dimension is 3.19Å while for Si(111) is 3.85Å.*

The GaN epitaxy layer investigated in this work belongs to a more complex structure as reported in Figure 60.

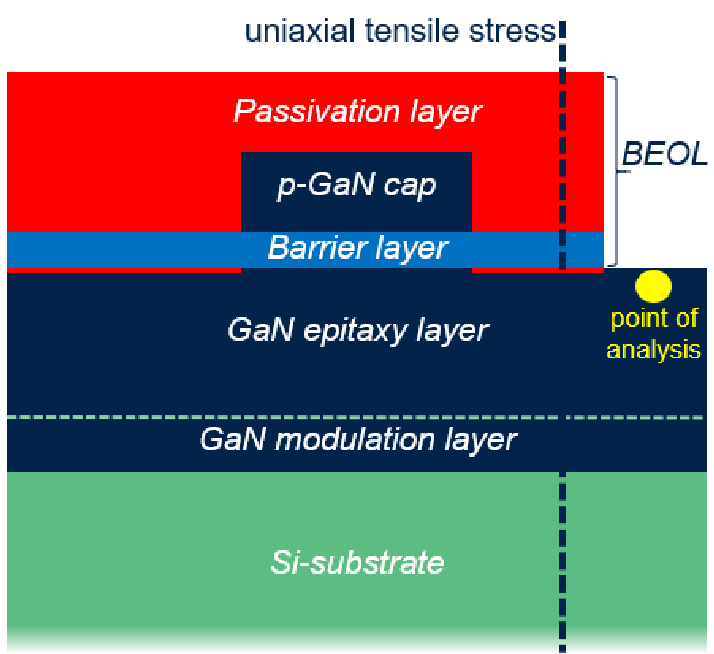


Figure 60: *Schematic representation of the GaN-based device investigated in this work. The vertical black dashed line indicates the direction of the applied uniaxial tensile stress, while the yellow dot highlights the point where Raman measurements were collected.*

In particular, it consists of an initial GaN(0001) modulation layer grown on a n-Si(111) substrate through metal-organic chemical vapor deposition (MOCVD). The n-Si(111) is characterized by a triangular symmetry which better support the hexagonal structure of GaN itself. Such modulation layer is generally grown at low temperature to mitigate the mechanical strain and reduce the crystallographic defects and dislocation density. It also plays a key role in reducing the reticular mismatch between the Si-substrate and the GaN epitaxy layer of interest, grown over it. In our case, experimental micro-Raman spectra were collected on a specific point (yellow dot in Figure 60) of the GaN epitaxy layer, following the application of a uniaxial tensile stress along the device (vertical black dashed line in Figure 60). Finally, depending on the electrical characteristics of the final device, a barrier, metallization and passivation layers (here all grouped under the heading BEOL (back-end of line), see Figure 60) are built on the structure with different designs.

A home-made set-up, consisting of a three-point assembly, two supporting pins and a loading one, was used to generate the uniaxial tensile stress along the device. It is equipped with a manual micrometer with a screw pitch of 0.5 mm - and division on thimble 50 - to monitor and regulate the strain applied to the GaN layer (see Figure 61). In our case, the total deformation applied on the system was of ~ 200 µm, achieved in 10 steps.

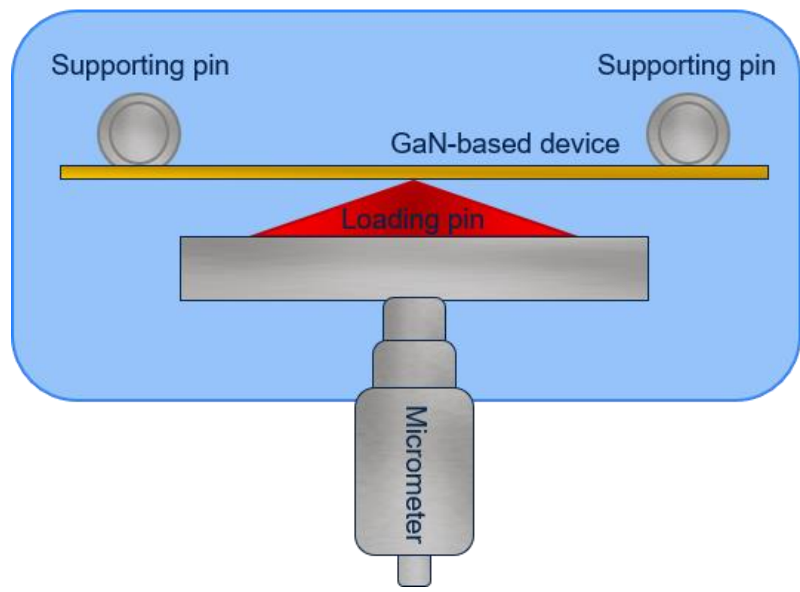


Figure 61: *Schematic representation of the home-made set-up used in this work.*

In our case, all measurements were carried out in backscattering geometry, using the microscope lens of the instrument to optimize the collection of the scattered light.

Figure 62 shows a typical micro-Raman spectrum of a MOCVD-grown GaN film, with no tensile stress applied, in the frequency region between 500 and 600 cm^{-1}.

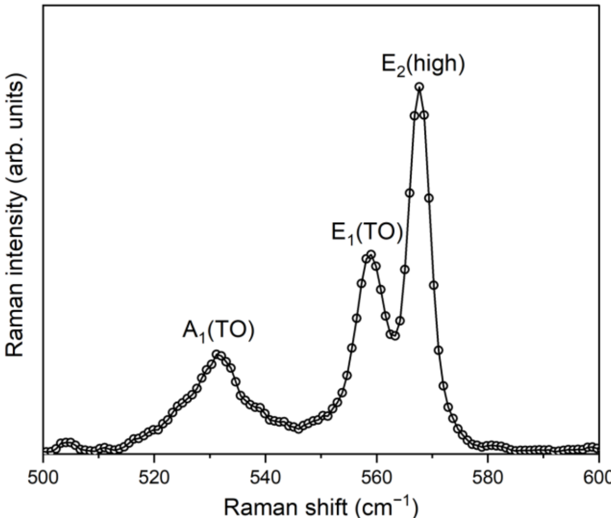


Figure 62: *Stress-free micro-Raman spectrum collected on the investigated point of analysis of the MOCVD grown GaN epitaxy layer with excitation of 532 nm in backscattering geometry at RT in the 500 – 600 cm^{-1} wavenumber range.*

The hexagonal structure of wurtzite belongs to the crystallographic C^4_{6v} space group, which predicts 8 different optical modes: two A_1, two E_1, two E_2 and two B_1. However, only 4 of the aforementioned modes are Raman active, *i.e.* one A_1(TO), one E_1(TO) and two E_2 (low and high, respectively), and hence observable through Raman spectroscopy [125]. The detected micro-Raman profile (see Figure 62) revealed all these first-order Raman modes other than the E_2(low) symmetry mode which falls outside the investigated wavenumber range (141 cm^{-1}). In particular, the A_1(TO), E_1(TO) and E_2(high) modes can be clearly distinguished (see Figure 62), respectively falling at 531.7 cm^{-1}, 558.7 cm^{-1} and 567.7 cm^{-1}. It is worth of note that if, on one side, the observed peak's width and intensity provide valuable information about the quality of the substrate, on the other side, their frequency-centre can be used to monitor internal stresses occurring in the epitaxial film of GaN crystals. Accordingly, with the aim to evaluate the evolution of localized residual stresses inside the MOCVD-grown GaN substrate, a detailed analysis of the frequency shifts exhibited by the aforementioned spectral features upon mechanical perturbation was accomplished [126]. For this purpose, the MOCVD-grown GaN epitaxy layer was subjected to ten different tensile loads up to 5.8 GPa (above which the sample break down), and for each configuration a micro-Raman spectrum was collected. The A_1(TO), E_1(TO) and E_2(high) peaks were first fitted with Lorentzian lineshape profiles (see Figure 63a) and then their position was derived as a function of the applied stress. The correlation between the tensile stress and Raman shift for each mode (A_1(TO), E_1(TO) and E_2(high)) is reported in Figure 63b. In all cases, frequency-centres (ω) were found to monotonically decrease as the uniaxial tensile stress increases. More in detail, the E_2(high) mode appears to be more susceptible to the mechanical perturbation with respect to both A_1(TO) and E_1(TO), in agreement with literature [127].

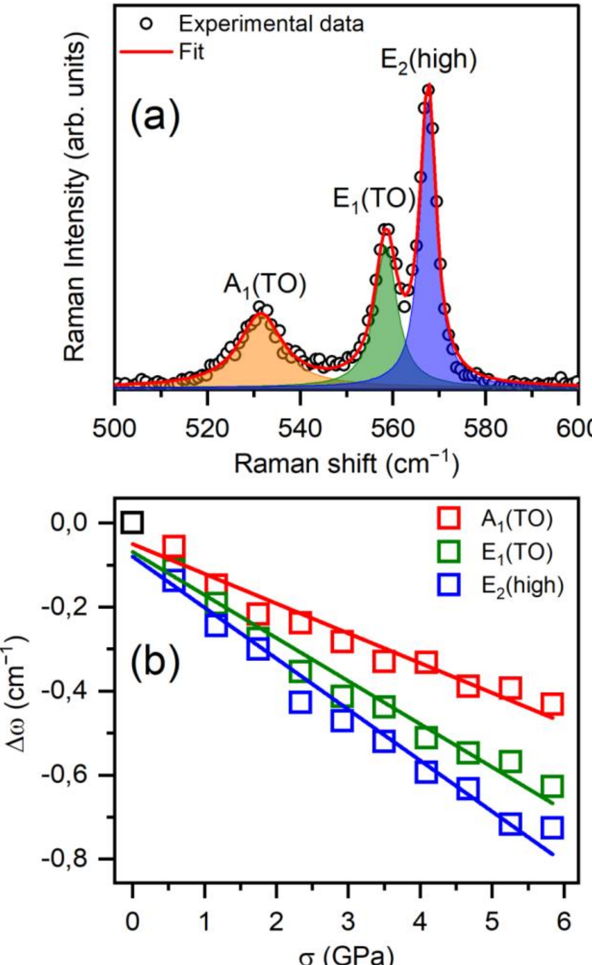


Figure 63*: (a) Experimental micro-Raman spectrum of MOCVD-grown GaN epitaxy layer (black dots), together with the obtained fitting curve (red line) using Lorentzian functions. (b) Raman frequency shifts, $\Delta\omega = \omega - \omega_0$ (where ω_0 accounts for the corresponding stress-free peak position), for all the investigated modes upon increase in the tensile stress. Stress values, in GPa, were calculated starting from the applied manual deformation values and considering the Young module of the GaN material (that is 295 GPa). Coloured lines account for the linear fits of the observed frequency shift trends (see text for details).*

This can be reasonably due to the fact that the E_2(high) mode involves atomic oscillations almost perpendicular to the c-axis of wurtzite, and hence more sensitive to the stress along the chosen axis (see Figure 60). Going on, the observed trends reported in Figure 63b allowed us to calculate the residual stress inside the GaN substrate. As a matter of fact, the frequency shift ($\Delta\omega$) behaviour usually traces a linear relationship

with the applied stress (σ) which can be modelled, in the case of polycrystalline structure, through the following statistical relation:

$$\langle \Delta\omega \rangle = \Psi_{PS} \langle \sigma \rangle,$$

where Ψ_{PS} is the piezo-spectroscopic coefficient equal to the trace of the piezo-spectroscopic tensor. Based on the assumption that, in first approximation, the residual stress Ψ_{RS} can be considered as equi-triaxial [128], it can be calculated as:

$$\Psi_{RS} = 3\Psi_{PS}$$

Based on the aforementioned considerations, starting from the linear regressions of the Raman frequency shifts upon increase in the tensile stress shown in Figure 63b, the Ψ_{PS} values associated to the A1(TO), E1(TO) and E2(high) modes were found to be equal to -0.08 cm^{-1} GPa^{-1}, -0.012 cm^{-1} GPa^{-1} and -0.013 cm^{-1} GPa^{-1}, respectively. According to above equation, the obtained values of Ψ_{PS} provides residual stresses Ψ_{RS} equal to -0.24 cm^{-1} GPa^{-1}, -0.36 cm^{-1} GPa^{-1} and -0.39 cm^{-1} GPa^{-1}.

5.3 **Evaluation of stress induced by packaging in GaN devices using Raman spectroscopy**

A micro-Raman spectroscopy analysis was carried out to evaluate the localized residual stresses [129] in AlGaN/GaN high electron mobility transistors (HEMTs) (Gallium Nitride (GaN)-based devices) [130], provided by *STMicroelectronics S.r.l.*, by analysing the frequency shifts [131] induced by device packaging (PD) on specific spectral components. In integrated circuits (IC), the PD plays a key role in protecting the device core from the external environment, thus minimizing the damage from mechanical impact, and exposure to light and chemical solutions, while maintaining a good heat dissipation rate. Nowadays, although the PD is a required step for the proper functioning of a ready-to-use electronic device, its application typically provides non-negligible residual stresses in the AlGaN/GaN HEMTs that may cause different reliability failures. In this frame the study of the residual stress induced by the

packaging may play a key role as this information can aid to improve the design with the aim to compensate the stress among the layers improving the overall quality of the devices. Indeed, compensating the residual stress allows to improve the dynamic range where the device is able to work, as the residual stresses can add to those induced by thermomechanical effects resulting from the device's operation and create the critical conditions beyond which the device fails. To the above purpose, we compared the residual stress of a packaged AlGaN/GaN HEMT (AlGaN/GaN HEMT-PD) with respect to the bare AlGaN/GaN HEMT (AlGaN/GaN HEMT-B), (both provided by *STMicroelectronics S.r.l*) (Figure 64), studying the frequency shift, along the GaN and GaN/Si interfaces, of the E_2(high) Raman peak [132]. The correlation between the stress induced from the package and Raman shifts for the specific spectral feature was properly quantified revealing peaks shift towards lower frequencies. The proposed methodology could in principle be implemented in large-scale semiconductor industrial processes with the aim to help novel designs and focus on different reliability issues related to the packaging [133].

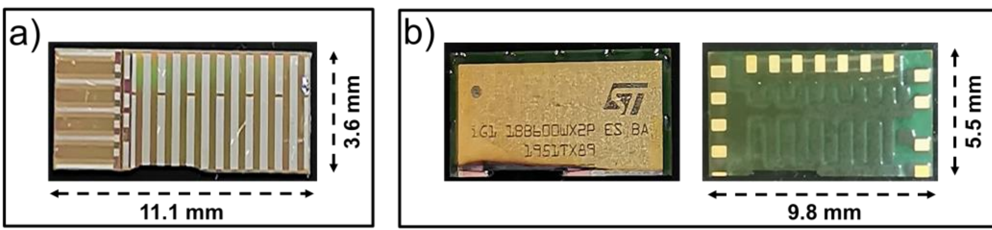


Figure 64: *AlGaN/GaN HEMT-B (a) and AlGaN/GaN HEMT-PD (b) samples investigated in this study.*

According to the aforementioned consideration, the E_2(high) mode frequency-center (ω) was monitored, for both AlGaN/GaN HEMT-PD and AlGaN/GaN HEMT-B samples, along a vertical direction (from the bottom to the top of HEMT device), crossing all the AlGaN/GaN heterostructures. This, together with the use of specific strain/stress relation, allows to correlate the optical data, as achieved by micro-Raman spectroscopy, and residual stress existing within the layers of the device under test [73,134–136]. Knowledge of the aforementioned not only helps to evaluate the reliability and performance of GaN-based electronic for several applications but also

may provide useful information for the understanding of unknown failure mechanisms which compromise their lifetime.

Figure 65 shows the AlGaN/GaN HEMT structure investigated in this work. It consists of a GaN(0001) modulation layer grown on a n-Si(111) substrate through metal-organic chemical vapor deposition (MOCVD).

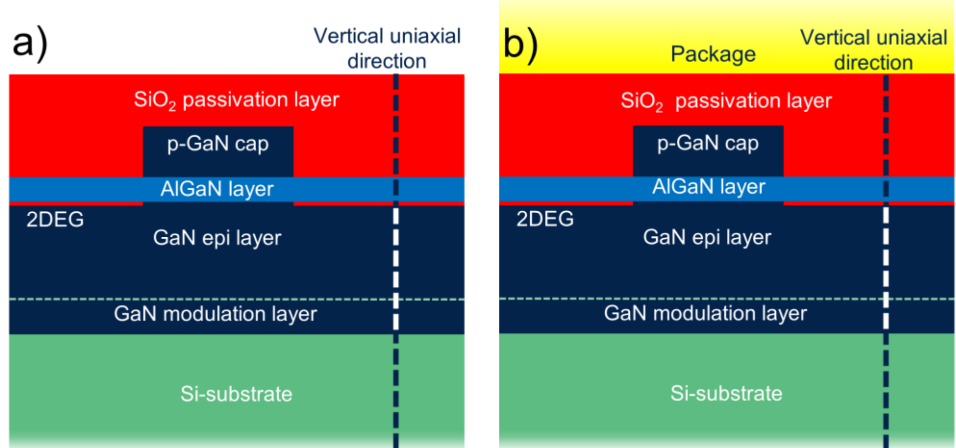


Figure 65: *Schematic representation of the internal structure of AlGaN/GaN HEMT-B (a) and AlGaN/GaN HEMT-PD (b) devices investigated in this work (not to scale). The vertical dashed line indicates the uniaxial direction along which micro-Raman measurements were collected.*

Such modulation layer plays a key role in the reduction of the lattice mismatch between the Si-substrate and the GaN epitaxy layer, grown over it. A two-dimensional electron gas (2DEG) sheet at the GaN epitaxy/AlGaN heterojunction interface guaranteed the conductive channels within the device. Furthermore, to use AlGaN/GaN HEMT for power switching applications, normally-off working conditions are required. The only commercially available transistors capable to accomplish the aforementioned features require the employments of a p-GaN cup gate, which creates a region of accumulation or depletion charge in the 2DEG channel, stabilizes the threshold voltage and improves the HEMTs reliability. Above the AlGaN metallization layer, a SiO_2 passivation coat was laid with different designs. To measure the Raman spectrum of the layers composing the device, it was necessary to cut it transversely. However, a simple cut and subsequent polishing were not suitable experimental strategies because they would induce mechanical stress, leading to

inaccurate measurements. For this reason, an ion beam milling technique was employed as this technique avoids external compressions or deformations phenomena. In particular, two identical devices were prepared, one of which was at wafer level – Bare (B) while the second was encapsulated – Packaged device (PD), in order to compare their Raman spectra and highlight the effect of encapsulation on residual stress.

The samples were positioned in such a way to face the cross-section upwards taking advantage of a home-made sample holder set-up as shown in Figure 66. For each sample, 128 micro-Raman spectra were collected along the vertical uniaxial direction crossing through GaN heterostructure (see Figure 65) with a step size of 78 nm covering a 10 µm path, for a total of 64 minutes collection time (30 s acquisition time for each spectrum).

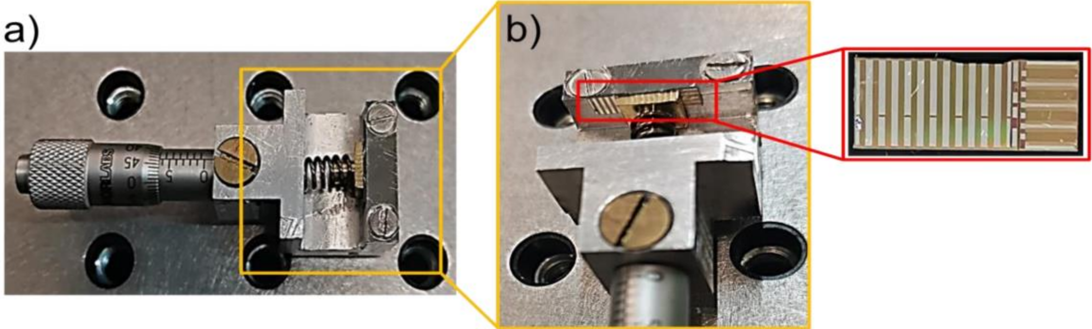


Figure 66: *Picture of the sample holder (a) with details of the sample position (b).*

A detailed view of the 10 µm scanned path, together with the resulting Raman map obtained by acquiring 128 spectra along the chosen direction is shown in Figure 67. Figure 67b shows the behaviour of the Raman peaks as a function of the position along the line marked in Figure 67a.

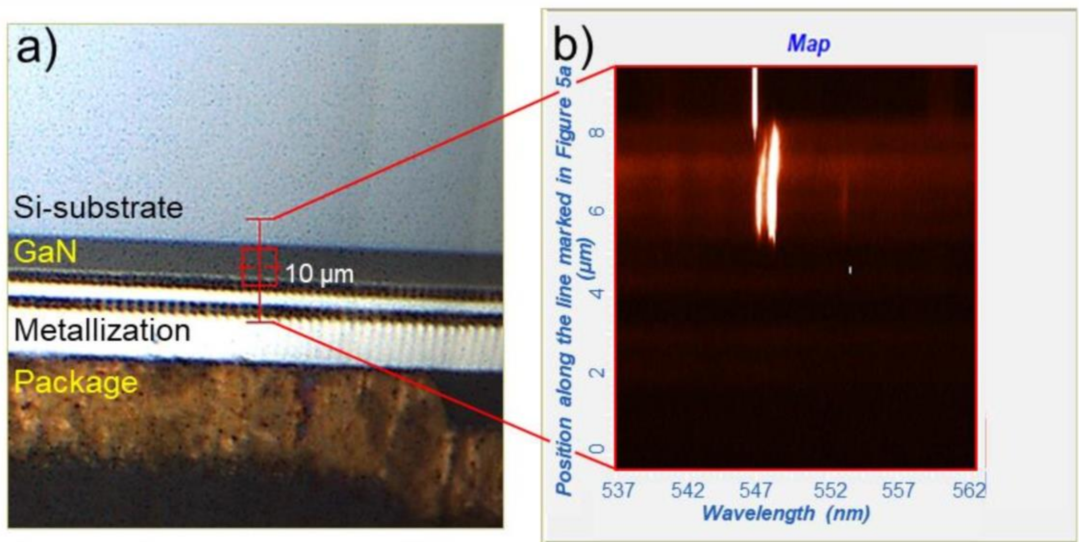


Figure 67: *Detailed view of the 10 µm scanned path (a), together with resulting Raman map (b) obtained by acquiring 128 spectra along the chosen path.*

Figure 68 shows typical micro-Raman spectra collected at the GaN epitaxy layer (Figure 68a) and at the interface between GaN/Si (Figure 68b), respectively, in the frequency region between 500 and 600 cm^{-1}.

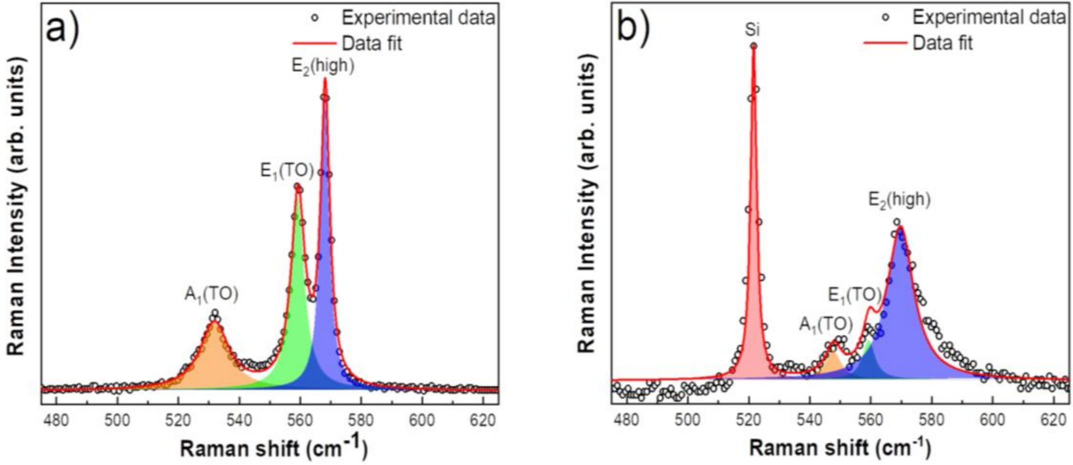


Figure 68: *Micro-Raman spectrum collected at the GaN epitaxy layer (a) and at the interface between GaN/Si (b) respectively of the AlGaN/GaN HEMT in the 500-600 cm^{-1} wavenumber range.*

The detected micro-Raman profile collected at the GaN epitaxy layer (Figure 68a) revealed contributions at 531.7 cm^{-1}, 558.7 cm^{-1}, and 567.7 cm^{-1} respectively

associated to the A_1(TO), E_1(TO) and E_2(high) modes of the hexagonal structure of wurtzite. Moving from the GaN epitaxy layer to the GaN/Si interface (Figure 68b), the characteristic Si Raman peak centered at 521.4 cm^{-1}, arising from the Si layer, can be clearly distinguished. Furthermore, all the Raman modes deriving from the GaN structures, i.e. A_1(TO), E_1(TO), and E_2(high), can be also observed, falling at 547.4 cm^{-1}, 559.2 cm^{-1}, and 569.6 cm^{-1}. The high-frequency shift observed for the A_1(TO), E_1(TO), and E_2(high) modes passing from the GaN substrate to the GaN/Si interface can be attributed to the different stress conditions insisting on these two regions. It is well known that the frequency centre of Raman peaks can be considered as intimately correlated to the nature of the interatomic potential between atoms [137]. Accordingly, changes in the interatomic potential arising from intrinsic stress existing within the crystal, are typically accompanied by Raman shifts of specific and characteristic vibrational modes of the structure, regardless of its origin [137]. To properly quantify the packaging impact on the frequency-center of the A_1(TO), E_1(TO), and E_2(high) Raman modes in HEMT devices, the entire spectrum was first fitted with Lorentzian line shapes profile and then the ω_0 of the E_2(high) mode was extrapolated as a function of the position along the scanned uniaxial direction.

In Figure 69 the E_2(high) ω-value, obtained by scanning along a vertical line crossing the AlGaN/GaN heterostructure (see Figure 67) with a specific focus on the GaN layer,(i.e. from 5 µm to 7 µm) is displayed for both HEMT-B and HEMT-PD samples.

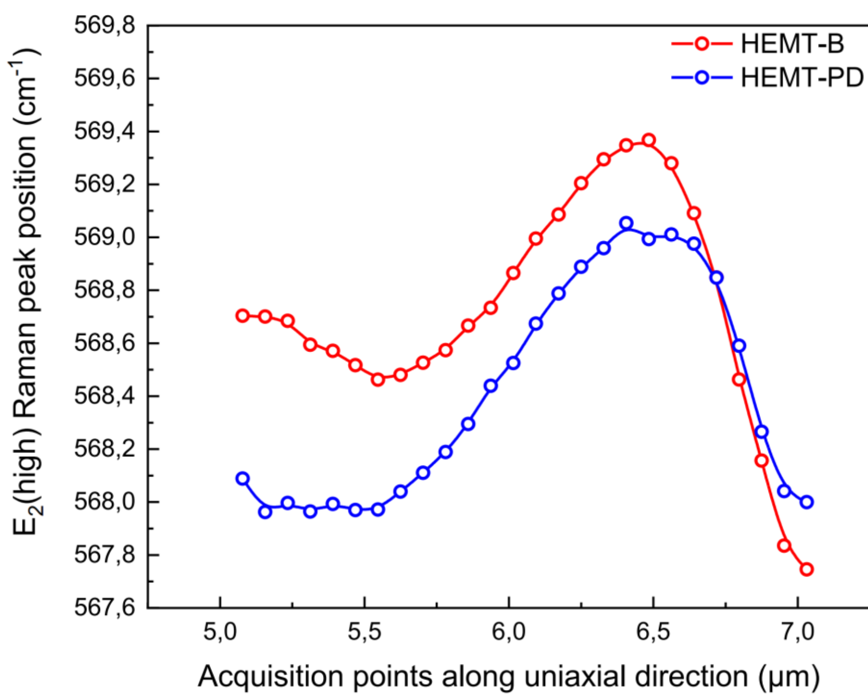


Figure 69: *E_2 (high) Raman peak position in function of acquisition points along uniaxial direction in the GaN layer, ranging from 5 µm to 7 µm, for both AlGaN/GaN HEMT-B and AlGaN/GaN HEMT-PD devices.*

Taking into account the E_2 (high) mode ω-value trend for AlGaN/GaN HEMT devices, it is worth noting that the influence of the package is mainly visible in the range from 5 µm to 6 µm (region of interest). On the other hand, from 6 µm to 7 µm, the GaN/Si lattice mismatch induces a greater tensile stress, which is visible through the redshift of the E_2 mode, compared to the packaging effect. Moreover, the non-monotonic behaviour of the ω-value trend can be attributed to the multilayer structure and to the doping of the device. Based on the previously mentioned considerations, looking at the HEMT-B frequency-centre position versus of the acquisition points (red curve) from 5 µm to 6 µm, a small shift towards lower values, representative of tensile stress, is observed. Furthermore, concerning the E_2 (high) mode ω-value trend for the HEMT-PD device (blue curve), a small shift towards the higher frequencies is visible moving from the package side to the inner part of the device. Such behaviour suggests the presence of compressive stress introduced by the packaging process. The observed trends reported in Figure 69 allowed us to calculate the residual stress inside the AlGaN/GaN HEMT samples. As a matter of fact, the frequency shift (Δω) behaviour

usually traces a linear relationship with the residual stress (σ) which can be modelled, in the case of polycrystalline structure, through the following statistical relation: $\langle \Delta\omega \rangle = K\langle \sigma \rangle$, where K is the stress coefficient equal to 4.3 cm^{-1}/GPa for GaN grown on c-direction silicon [138], while $\Delta\omega = \omega - \omega_0$ where ω_0 accounts for the corresponding stress-free E_2(high) peak position that is 568 cm^{-1} [139]. In Table 4, the residual stress σ, along the uniaxial direction, calculated starting from the E_2(high) ω-values for both HEMT-B and HEMT-PD, is reported.

Table 4: *Stress values σ, in GPa, calculated starting from the E_2(high) ω-values for both AlGaN/GaN HEMT-B and AlGaN/GaN HEMT-PD devices.*

Acquisition points along the uniaxial direction (μm)	**HEMT-B**	**HEMT-PD**
	Stress σ (GPa)	
5,08	0,16	0,02
5,16	0,16	-0,01
5,23	0,16	0,00
5,31	0,14	-0,01
5,39	0,13	0,00
5,47	0,12	-0,01
5,55	0,11	-0,01
5,63	0,11	0,01
5,70	0,12	0,03
5,78	0,13	0,04
5,86	0,16	0,07
5,94	0,17	0,10
6,02	0,20	0,12
6,09	0,23	0,16
6,17	0,25	0,18
6,25	0,28	0,21
6,33	0,30	0,22
6,41	0,31	0,24
6,48	0,32	0,23
6,56	0,30	0,23
6,64	0,25	0,23
6,72	0,20	0,20
6,80	0,11	0,14
6,88	0,04	0,06
6,95	-0,04	0,01

Based on the aforementioned considerations, as the relationship between the stress and the frequency shift is linear, we can conclude that for both AlGaN/GaN HEMT-B and AlGaN/GaN HEMT-PD devices, the stress along the layers follows the same behaviour as in Figure 69. In particular, taking into account the acquisition points close to the zone of interest, the difference between the HEMT-B and HEMT-PD stress values is about 0.1 GPa, and we can conclude that packaging procedure introduces a compressive stress which tends to compensate the intrinsic tensile stress existing at the wafer level device.

In conclusions, both the proposed studies furnished insights about the employment of micro-Raman spectroscopy for the assessment of potential reliability risk introduced not only during the FEoL production step, but also during the BEoL step, including the packaging process. Each failure, in fact, represents a customer return that can have a significant impact particularly in our daily lives depending on the specific device applications, i.e. *automotive* devices installed in vehicles to control brakes, lights, airbags, and electronic control systems.

CONCLUSIONS

In this thesis, a thermal characterization in Metal-Oxide-Metal (MOM) Si-based substrates and micro-Raman spectroscopy investigations in high electron mobility transistors (HEMTs) GaN-based device, were performed to analyse the device reliability, provided by *STMicroelectronics S.r.l.*, under specific conditions.

Considering MOM capacitors, a preliminary evaluation of two *test pattern* (TP1 and TP2), wafers characterized by at least 4-times larger MOM area with respect to the “standard” BCD8 device, was carried out through visual inspection, SEM review, defect classification and current-DC voltage (I-V) analysis. The aforementioned methodologies were of paramount importance for the identification of the DUT failure arising from the production processes. The idea lying below the proposed method is strictly bonded to the MOM structure. It mainly consists of a capacitor, applying a suitable alternate electrical field it is possible to dissipate energy inside the dielectric due to the displacement current. This energy results in a small increasing of the temperature that can be observed by a thermal camera. If the dielectric is not perfect due to the presence of dielectric or metallic particles the temperature behaviour increases much and may be localized in one or more areas of the device because the current increases much following specific paths which comes from the MOM structure. This method is absolutely innovative in the semiconductor’s reliability field. The technique allows the identification of defects arising from the production process. In the case of metallic defects, short circuits between MOM strips often occur, and failure is easily detectable even with conventional techniques that involve evaluating the component's leakage current. This is not the case with particles of dielectric material, which, although predisposing the component to early failure, do not show obvious signs when using DC measurement-based techniques but are easily detected by the proposed method. The home-made thermal characterisation set-up mainly consists of a home-made probe station equipped with a high frequency generator

(30MHz) and a thermal camera (FLIR) able to catch very small temperature increases. An initial validation phase involved the acquisition of the thermal maps for both "good" and "fail" sites previously identified. This was a key phase used to *calibrate* the setup and establish necessary references for data evaluation. Going on, measurements were carried out on the remaining selected devices, yielding mostly consistent results compared to those achieved through the I-V analysis. On the other hand, the D7_G3 site for TP1 exhibited unexpected behaviour, probably due to a defect not detected through both the in-line inspections I-V analysis. In this case, the thermal characterization played a pivotal role in the detection for reliability purposes, proving to be a reliable and efficient approach to quickly assess the device functionality. However, it is worth noting that the method does not allow for the precise localization of the defect. Better results can be achieved by increasing the frequency of the signal input into the device, for example, up to frequencies typical of microwaves. Moreover, conducting tests on "finished" devices rather than *test patterns* and the increase of samples to obtain more statistics is essential considering an industrial production scenario.

Regarding studies conducted using Raman spectroscopy to characterize the residual stresses between the semiconductor layers constituting the devices and the packaging effect on these stresses, we successfully measured both the residual stresses in a the GaN substrate and the stress/strain induced by the packaging process in AlGaN/GaN high electron mobility transistors (HEMTs) Gallium Nitride (GaN)-based devices. In particular, in the first study, a diminishing of the frequency centre value of different specific modes of the material (i.e. A_1(TO), E_1(TO) and E_2(high)), upon increasing of the uniaxial tensile load, was observed. A linear regression procedure allowed us to properly calculate the residual stresses Ψ_{RS}, starting from the evaluation of the piezo-spectroscopic coefficient Ψ_{PS}. Obtained values of Ψ_{RS} were -0.24 cm^{-1} GPa^{-1}, -0.36 cm^{-1} GPa^{-1} and -0.39 cm^{-1} GPa^{-1}, respectively from the A_1(TO), E_1(TO) and E_2(high) frequency-centre behaviour. With the aim to further improve the overall quality of the data, a computer-controlled micrometre will be implemented in the experimental set-up, together with a steel wedge (instead of a plastic wedge). Finally, the influence of applied stress over the device active area will be also the subject of future investigations. In the second scenario to evaluate the effect of the packaging process

two sample with (HEMT-PD) and without (HEMT-B) package was considered. In both cases, the acquisition of many spectra moving along the device were collected and analysed using a Lorentzian fit procedure to properly quantify the frequency-center (ω) shift of E2(high) phonon mode, that constitute a good marker for the GaN layer, for both HEMT-B and HEMT-PD devices. A diminishing for HEMT-B and increasing for the HEMT-PD sample was observed for the E2(high) frequency center. A linear relationship that links Raman frequency shift $\Delta\omega$ with the stress σ, was used to demonstrate that a tensile stress is present in HEMT-B device, while a compressive stress is visible in the HEMT-PD sample closely to the package. Through this investigation, it was found that the compressive stress induced by the packaging process strongly mitigates the residual tensile stress present in the bare device. With this approach, it has been confirmed that the packaging plays a crucial role in the design of GaN-based devices, ensuring better performance and reliability.

BIBLIOGRAPHY

1. Yu, P.Y.; Cardona, M. *Fundamentals of Semiconductors*; Springer Berlin Heidelberg: Berlin, Heidelberg, 1996; ISBN 978-3-540-61461-6.
2. Rudan, M. *Physics of Semiconductor Devices*; Springer New York: New York, NY, 2015; ISBN 978-1-4939-1150-9.
3. Inoguchi, T. Semiconductor Physics and Semiconductor Devices. *J. Inst. Telev. Eng. Japan* **1974**, *28*, 723–730, doi:10.3169/itej1954.28.723.
4. Fu, W.Y.; Choi, H.W. GaN PNP Light-Emitting Bipolar Junction Transistor. *J. Phys. D. Appl. Phys.* **2022**, *55*, 015101, doi:10.1088/1361-6463/ac296b.
5. Böer, K.W.; Pohl, U.W. *Semiconductor Physics*; Springer International Publishing: Cham, 2023; ISBN 978-3-031-18285-3.
6. Grundmann, M. *The Physics of Semiconductors (2nd Edition)*; 2010; ISBN 9783642138836.
7. Sharma, S.; Kumar, P. Quaternary Semiconductors Cu2MgSnS4 and Cu2MgSnSe4 as Potential Thermoelectric Materials. *J. Phys. Commun.* **2017**, doi:10.1088/2399-6528/aa9286.
8. Salik, L.; Bouhemadou, A.; Boudiaf, K.; Saoud, F.S.; Bin-Omran, S.; Khenata, R.; Al-Douri, Y.; Reshak, A.H. Structural, Elastic, Electronic, Magnetic, Optical, and Thermoelectric Properties of the Diamond-like Quaternary Semiconductor CuMn2InSe4. *J. Supercond. Nov. Magn.* **2020**, *33*, 1091–1102, doi:10.1007/s10948-019-05331-1.
9. Ghemud, V.S.; Jadhav, P.R.; Kolhe, P.T.; Shelke, P.N.; Dahiwale, S.S.; Kshirsagar, A. Experimental and Computational Study of Cu2FeSnS4: An Emerging Quaternary Semiconductor. *Opt. Mater. (Amst).* **2023**, *142*, 114123, doi:10.1016/j.optmat.2023.114123.
10. Shree, S.; Paradisanos, I.; Marie, X.; Robert, C.; Urbaszek, B. Guide to Optical Spectroscopy of Layered Semiconductors. *Nat. Rev. Phys.* **2020**, *3*, 39–54,

doi:10.1038/s42254-020-00259-1.

11. Szkopek, T. A Longer-Lasting Memory in Layered Semiconductors. *Nat. Nanotechnol.* **2018**, *13*, 357–357, doi:10.1038/s41565-018-0132-0.

12. Si, K.; Huang, Y.; Zhao, Q.; Zhu, L.; Zhang, L.; Yao, Z.; Xu, X. Terahertz Surface Emission from Layered Semiconductor WSe 2. *Appl. Surf. Sci.* **2018**, doi:10.1016/j.apsusc.2018.04.117.

13. Ding, J.; Cheng, P.; Ye, T.; Xu, W.; Zeng, H.; Yao, D.; Pan, X.; Zhang, J. Pressure-Induced Two-Dimensional to Three-Dimensional Structural Phase Transition in 2H-Type Layered Lead Iodide PbI2. *Appl. Phys. Lett.* **2022**, doi:10.1063/5.0081461.

14. Cong, C.; Shang, J.; Niu, L.; Wu, L.; Chen, Y.; Zou, C.; Feng, S.; Qiu, Z.; Hu, L.; Tian, P.; et al. Anti-Stokes Photoluminescence of van Der Waals Layered Semiconductor PbI 2. *Adv. Opt. Mater.* **2017**, *5*, 1700609, doi:10.1002/adom.201700609.

15. Awol, N.; Amente, C.; Verma, G.; Kim, J.Y. A Versatile Lead Iodide Particle Synthesis and Film Surface Analysis for Optoelectronics. *J. Alloys Compd.* **2020**, *829*, 154486, doi:10.1016/j.jallcom.2020.154486.

16. Sun, L.; Wang, C.; Xu, L.; Wang, J.; Chen, X.; Yi, G.-C. Millimeter-Sized PbI 2 Flakes and Pb 5 S 2 I 6 Nanowires for Flexible Photodetectors. *J. Mater. Chem. C* **2018**, *6*, 7188–7194, doi:10.1039/C8TC01657G.

17. Kelley, T.W.; Baude, P.F.; Gerlach, C.; Ender, D.E.; Muyres, D.; Haase, M.A.; Vogel, D.E.; Theiss, S.D. Recent Progress in Organic Electronics: Materials, Devices, and Processes. *Chem. Mater.* 2004.

18. Kato, K.; Kobayashi, H.; Shishido, H.; Isa, T.; Aoyama, T.; Jimbo, Y.; Hodo, R.; Kusunoki, K.; Kunitake, H.; Yamazaki, S. 5,291-ppi OLED Display Enabled by Monolithic Integration of C -axis-aligned Crystalline IGZO FET and Si CMOS. *J. Soc. Inf. Disp.* **2022**, *30*, 690–698, doi:10.1002/jsid.1167.

19. Shi, J.; Zhang, J.; Yang, L.; Qu, M.; Qi, D.; Zhang, K.H.L. Wide Bandgap Oxide Semiconductors: From Materials Physics to Optoelectronic Devices. *Adv. Mater.* **2021**, *33*, 2006230, doi:10.1002/adma.202006230.

20. Kleemann, H.; Krechan, K.; Fischer, A.; Leo, K. A Review of Vertical Organic Transistors. *Adv. Funct. Mater.* 2020.

21. Sun, C.; Wang, X.; Auwalu, M.A.; Cheng, S.; Hu, W. Organic Thin Film Transistors-

based Biosensors. *EcoMat* **2021**, *3*, doi:10.1002/eom2.12094.

22. Wang, J.; Ye, D.; Meng, Q.; Di, C.; Zhu, D. Advances in Organic Transistor-Based Biosensors. *Adv. Mater. Technol.* **2020**, *5*, doi:10.1002/admt.202000218.

23. Zschieschang, U.; Borchert, J.W.; Giorgio, M.; Caironi, M.; Letzkus, F.; Burghartz, J.N.; Waizmann, U.; Weis, J.; Ludwigs, S.; Klauk, H. Roadmap to Gigahertz Organic Transistors. *Adv. Funct. Mater.* **2020**, *30*, doi:10.1002/adfm.201903812.

24. Xue, F.; Zhang, C.; Ma, Y.; Wen, Y.; He, X.; Yu, B.; Zhang, X. Integrated Memory Devices Based on 2D Materials. *Adv. Mater.* **2022**, *34*, doi:10.1002/adma.202201880.

25. Kim, D.; Kim, I.-J.; Lee, J.-S. Memory Devices for Flexible and Neuromorphic Device Applications. *Adv. Intell. Syst.* **2021**, doi:10.1002/aisy.202000206.

26. Wei, Y.Y.; Eres, G. Directed Assembly of Carbon Nanotube Electronic Circuits. *Appl. Phys. Lett.* **2000**, *76*, 3759–3761, doi:10.1063/1.126772.

27. Zou, J.; Zhang, Q. Advances and Frontiers in Single-Walled Carbon Nanotube Electronics. *Adv. Sci.* **2021**, *8*, 2102860, doi:10.1002/advs.202102860.

28. Sun, D.-M.; Timmermans, M.Y.; Kaskela, A.; Nasibulin, A.G.; Kishimoto, S.; Mizutani, T.; Kauppinen, E.I.; Ohno, Y. Mouldable All-Carbon Integrated Circuits. *Nat. Commun.* **2013**, *4*, 2302, doi:10.1038/ncomms3302.

29. Liu, Y.; Wang, S.; Liu, H.; Peng, L.-M. Carbon Nanotube-Based Three-Dimensional Monolithic Optoelectronic Integrated System. *Nat. Commun.* **2017**, *8*, 15649, doi:10.1038/ncomms15649.

30. Xu, Y.; Srivastava, A.; Sharma, A.K. Emerging Carbon Nanotube Electronic Circuits, Modeling, and Performance. *VLSI Des.* **2010**, *2010*, 1–8, doi:10.1155/2010/864165.

31. Pérez-Tomás, A.; Fontserè, A.; Placidi, M.; Jennings, M.R.; Gammon, P.M. Modelling the Metal–Semiconductor Band Structure in Implanted Ohmic Contacts to GaN and SiC. *Model. Simul. Mater. Sci. Eng.* **2013**, *21*, 035004, doi:10.1088/0965-0393/21/3/035004.

32. Chowdhury, S.; Gurpinar, E.; Ozpineci, B. Capacitor Technologies: Characterization, Selection, and Packaging for Next-Generation Power Electronics Applications. *IEEE Trans. Transp. Electrif.* **2022**, *8*, 2710–2720, doi:10.1109/TTE.2021.3139806.

33. Li, F.; Roccaforte, F.; Greco, G.; Fiorenza, P.; La Via, F.; Pérez-Tomas, A.; Evans, J.E.; Fisher, C.A.; Monaghan, F.A.; Mawby, P.A.; et al. Status and Prospects of Cubic

Silicon Carbide Power Electronics Device Technology. *Materials (Basel).* **2021**, *14*, 5831, doi:10.3390/ma14195831.

34. Dimitris Karaventzas, V.; Nawaz, M.; Iannuzzo, F. Reliability Assessment of SiC Power MOSFETs from the End User's Perspective. In Proceedings of the 2016 IEEE Energy Conversion Congress and Exposition (ECCE); IEEE, September 2016; pp. 1–8.

35. Gurpinar, E.; Ozpineci, B.; Chowdhury, S. Design, Analysis and Comparison of Insulated Metal Substrates for High Power Wide-Bandgap Power Modules. In Proceedings of the ASME 2019 International Technical Conference and Exhibition on Packaging and Integration of Electronic and Photonic Microsystems; American Society of Mechanical Engineers, October 2019.

36. Arumugam, P.; Xu, Z.; La Rocca, A.; Vakil, G.; Dickinson, M.; Amankwah, E.; Hamiti, T.; Bozhko, S.; Gerada, C.; Pickering, S.J. High-Speed Solid Rotor Permanent Magnet Machines: Concept and Design. *IEEE Trans. Transp. Electrif.* **2016**, *2*, 391–400, doi:10.1109/TTE.2016.2592684.

37. Feng, W.; Ding, H.; Chen, F.; Lee, S.; Chen, K.; Jahns, T.; Sarlioglu, B. Design of High Power Density 100 KW Surface Permanent Magnet Machine with No Heavy Rare Earth Material Using Current Source Inverter for Traction Application. In Proceedings of the 2021 IEEE Transportation Electrification Conference & Expo (ITEC); IEEE, June 2021; pp. 1–6.

38. Murari, B.; Contiero, C.; Gariboldi, R.; Sueri, S.; Russo, A. Smart Power Technologies Evolution. In Proceedings of the Conference Record of the 2000 IEEE Industry Applications Conference. Thirty-Fifth IAS Annual Meeting and World Conference on Industrial Applications of Electrical Energy (Cat. No.00CH37129); IEEE, 2000; Vol. 1, pp. P10–P19.

39. Andreini, A.; Contiero, C.; Galbiati, P. A New Integrated Silicon Gate Technology Combining Bipolar Linear, CMOS Logic, and DMOS Power Parts. *IEEE Trans. Electron Devices* **1986**, *33*, 2025–2030, doi:10.1109/T-ED.1986.22862.

40. Pendharkar, S. Integration of Substrate-Isolated High Voltage Devices in Junction Isolated Technologies. In Proceedings of the Proceedings of 35th European Solid-State Device Research Conference, 2005. ESSDERC 2005.; IEEE, 2005; pp. 485–488.

41. Forsberg, M.; Johansson, T.; Liu, W.; Vellaikal, M. A Shallow and Deep Trench

Isolation Process Module for RF BiCMOS. *J. Electrochem. Soc.* **2004**, *151*, G839, doi:10.1149/1.1811596.

42. Chil, M.N.; Yang, O.S.; Ke, D.; Mo, K.J.; Kun, L.; Tiong, M.; Purakh, R.V.; Nair, R. Advanced 300mm 130nm BCD Technology from 5V to 85V with Deep-Trench Isolation. In Proceedings of the 2016 28th International Symposium on Power Semiconductor Devices and ICs (ISPSD); IEEE, June 2016; pp. 403–406.

43. Shaneyfelt, M.R.; Dodd, P.E.; Draper, B.L.; Flores, R.S. Challenges in Hardening Technologies Using Shallow-Trench Isolation. *IEEE Trans. Nucl. Sci.* **1998**, *45*, 2584–2592, doi:10.1109/23.736501.

44. Gabrielli, C.; Moçotéguy, P.; Perrot, H.; Zdunek, A.; Sanz, D.N. A Model for Copper Deposition in the Damascene Process. *J. Electrochem. Soc.* **2007**, *154*, D13, doi:10.1149/1.2364831.

45. Jonghae Kim; Plouchart, J.-O.; Zamdmer, N.; Sherony, M.; Liang-Hung Lu; Yue Tan; Meeyoung Yoon; Jenkins, K.A.; Kumar, M.; Ray, A.; et al. 3-Dimensional Vertical Parallel Plate Capacitors in an SOI CMOS Technology for Integrated RF Circuits. In Proceedings of the 2003 Symposium on VLSI Circuits. Digest of Technical Papers (IEEE Cat. No.03CH37408); Japan Soc. Appl. Phys, 2003; pp. 29–32.

46. Hang Hu; Chunxiang Zhu; Lu, Y.F.; Li, M.F.; Byung Jin Cho; Choi, W.K. A High Performance MIM Capacitor Using HfO 2 Dielectrics. *IEEE Electron Device Lett.* **2002**, *23*, 514–516, doi:10.1109/LED.2002.802602.

47. Chen, N.-C.; Chou, P.-Y.; Graeb, H.; Lin, M.P.-H. High-Density MOM Capacitor Array with Novel Mortise-Tenon Structure for Low-Power SAR ADC. In Proceedings of the Design, Automation & Test in Europe Conference & Exhibition (DATE), 2017; IEEE, March 2017; pp. 1757–1762.

48. Liu, C.C.; Chang, S.J.; Huang, G.Y.; Lin, Y.Z. A 10-Bit 50-MS/s SAR ADC with a Monotonic Capacitor Switching Procedure. In Proceedings of the IEEE Journal of Solid-State Circuits; 2010.

49. Roccaforte, F.; Leszczynski, M. Introduction to Gallium Nitride Properties and Applications. In *Nitride Semiconductor Technology*; Wiley, 2020; pp. 1–39.

50. Johnson, W.C.; Parsons, J.B.; Crew, M.C. Nitrogen Compounds of Gallium: III. Gallium Nitride. *J. Phys. Chem.* **1932**, *36*, 2651–2654.

51. Juza, R.; Hahn, H. Über Die Kristallstrukturen von Cu 3 N, GaN Und InN Metallamide Und Metallnitride. *Zeitschrift für Anorg. und Allg. Chemie* **1938**, *239*, 282–287, doi:10.1002/zaac.19382390307.

52. Maruska, H.P.; Tietjen, J.J. The Preparation and Properties of Vapor-Deposited Single-Crystal-Line GaN. *Appl. Phys. Lett.* **1969**, *15*, 327–329, doi:10.1063/1.1652845.

53. Maruska, H.P.; Stevenson, D.A.; Pankove, J.I. Violet Luminescence of Mg-Doped GaN. *Appl. Phys. Lett.* **1973**, *22*, 303–305, doi:10.1063/1.1654648.

54. Manasevit, H.M.; Erdmann, F.M.; Simpson, W.I. The Use of Metalorganics in the Preparation of Semiconductor Materials: IV . The Nitrides of Aluminum and Gallium. *J. Electrochem. Soc.* **1971**, *118*, 1864–1868.

55. Manasevit, H.M. The Use of Metalorganics in the Preparation of Semiconductor Materials: Growth on Insulating Substrates. *J. Cryst. Growth* **1972**, *13–14*, 306–314, doi:10.1016/0022-0248(72)90175-3.

56. Amano, H.; Sawaki, N.; Akasaki, I.; Toyoda, Y. Metalorganic Vapor Phase Epitaxial Growth of a High Quality GaN Film Using an AlN Buffer Layer. *Appl. Phys. Lett.* **1986**, *48*, 353–355, doi:10.1063/1.96549.

57. Asif Khan, M.; Bhattarai, A.; Kuznia, J.N.; Olson, D.T. High Electron Mobility Transistor Based on a GaN-Al x Ga1− x N Heterojunction. *Appl. Phys. Lett.* **1993**, *63*, 1214–1215, doi:10.1063/1.109775.

58. Song, L.-N.; Lü, Y.-W. Effect of Inserted InGaN Layer on the Two-Dimensional Electron Gas in AlxGa1–XN/InyGa1–YN/GaN. *Acta Phys. Sin.* **2021**, *70*, 177201, doi:10.7498/aps.70.20202223.

59. Ambacher, O.; Smart, J.; Shealy, J.R.; Weimann, N.G.; Chu, K.; Murphy, M.; Schaff, W.J.; Eastman, L.F.; Dimitrov, R.; Wittmer, L.; et al. Two-Dimensional Electron Gases Induced by Spontaneous and Piezoelectric Polarization Charges in N- and Ga-Face AlGaN/GaN Heterostructures. *J. Appl. Phys.* **1999**, *85*, 3222–3233, doi:10.1063/1.369664.

60. Ibbetson, J.P.; Fini, P.T.; Ness, K.D.; DenBaars, S.P.; Speck, J.S.; Mishra, U.K. Polarization Effects, Surface States, and the Source of Electrons in AlGaN/GaN Heterostructure Field Effect Transistors. *Appl. Phys. Lett.* **2000**, *77*, 250–252, doi:10.1063/1.126940.

61. Shinohara, K.; Regan, D.C.; Tang, Y.; Corrion, A.L.; Brown, D.F.; Wong, J.C.; Robinson, J.F.; Fung, H.H.; Schmitz, A.; Oh, T.C.; et al. Scaling of GaN HEMTs and Schottky Diodes for Submillimeter-Wave MMIC Applications. *IEEE Trans. Electron Devices* **2013**, *60*, 2982–2996, doi:10.1109/TED.2013.2268160.

62. Freedsman, J.J.; Egawa, T.; Yamaoka, Y.; Yano, Y.; Ubukata, A.; Tabuchi, T.; Matsumoto, K. Normally-OFF Al 2 O 3 /AlGaN/GaN MOS-HEMT on 8 in. Si with Low Leakage Current and High Breakdown Voltage (825 V). *Appl. Phys. Express* **2014**, *7*, 041003, doi:10.7567/APEX.7.041003.

63. Www.Transphormusa.Com/En/.

64. Kikkawa, T.; Hosoda, T.; Shono, K.; Imanishi, K.; Asai, Y.; Wu, Y.; Shen, L.; Smith, K.; Dunn, D.; Chowdhury, S.; et al. Commercialization and Reliability of 600 V GaN Power Switches. In Proceedings of the 2015 IEEE International Reliability Physics Symposium; IEEE, April 2015; pp. 6C.1.1-6C.1.6.

65. Roccaforte, F.; Fabrizio, M. *Nitride Semiconductor Technology: Power Electronics and Optoelectronic Devices*; 2020; ISBN 9783527825264.

66. Leszczynski, M.; Teisseyre, H.; Suski, T.; Grzegory, I.; Bockowski, M.; Jun, J.; Porowski, S.; Pakula, K.; Baranowski, J.M.; Foxon, C.T.; et al. Lattice Parameters of Gallium Nitride. *Appl. Phys. Lett.* **1996**, *69*, 73–75, doi:10.1063/1.118123.

67. Paszkowicz, W.; Adamczyk, J.; Krukowski, S.; Leszczyński, M.; Porowski, S.; Sokolowski, J.A.; Michalec, M.; Łasocha, W. Lattice Parameters, Density and Thermal Expansion of InN Microcrystals Grown by the Reaction of Nitrogen Plasma with Liquid Indium. *Philos. Mag. A* **1999**, *79*, 1145–1154, doi:10.1080/01418619908210352.

68. Taniyasu, Y.; Kasu, M.; Kobayashi, N. Lattice Parameters of Wurtzite Al1−xSixN Ternary Alloys. *Appl. Phys. Lett.* **2001**, *79*, 4351–4353, doi:10.1063/1.1428768.

69. Ishida, T. GaN HEMT Technologies for Space and Radio Applications. *Microw. J.* **2011**, *54*, 56–66.

70. Trew, R.J.; Bilbro, G.L.; Kuang, W.; Liu, Y.; Yin, H. Microwave AlGaN/GaN HFETs. *IEEE Microw. Mag.* **2005**, *6*, 56–66, doi:10.1109/MMW.2005.1417998.

71. Islam, N.; Mohamed, M.F.P.; Khan, M.F.A.J.; Falina, S.; Kawarada, H.; Syamsul, M. Reliability, Applications and Challenges of GaN HEMT Technology for Modern

Power Devices: A Review. *Crystals* **2022**, *12*, 1581, doi:10.3390/cryst12111581.

72. Cho, J.; Li, Z.; Asheghi, M.; Goodson, K.E. Near-Junction Thermal Management: Thermal Conduction in Gallium Nitride Composite Substrates. *Annu. Rev. Heat Transf.* **2015**, *18*, 7–45, doi:10.1615/AnnualRevHeatTransfer.2015011335.

73. Liu, L.; Edgar, J.H. Substrates for Gallium Nitride Epitaxy. *Mater. Sci. Eng. R Reports* **2002**, *37*, 61–127, doi:10.1016/S0927-796X(02)00008-6.

74. Schuster, M.; Wachowiak, A.; Szabo, N.; Jahn, A.; Merkel, U.; Ruf, A.; Mikolajick, T.; Murad, S.; Hu, C.; Groh, L.; et al. HEMT Test Structure Technology for Fast On-Wafer Characterization of Epitaxial GaN-on-Si Material. In Proceedings of the 2013 International Semiconductor Conference Dresden - Grenoble (ISCDG); IEEE, September 2013; pp. 1–3.

75. Neudeck, P.G.; Okojie, R.S.; Liang-Yu Chen High-Temperature Electronics - a Role for Wide Bandgap Semiconductors? *Proc. IEEE* **2002**, *90*, 1065–1076, doi:10.1109/JPROC.2002.1021571.

76. Baliga, B.J. Silicon Carbide Power Devices. In *Springer Handbooks*; 2023; pp. 491–523.

77. Jain, S.C.; Willander, M.; Narayan, J.; Overstraeten, R. Van III–Nitrides: Growth, Characterization, and Properties. *J. Appl. Phys.* **2000**, *87*, 965–1006, doi:10.1063/1.371971.

78. Sze, S.M.; Ng, K.K. Physics of Semiconductor Devices. *Phys. Semicond. Devices, 3rd Ed. John Wiley Sons, Inc.; NJ* **2007**.

79. Roccaforte, F.; Fiorenza, P.; Nigro, R. Lo; Giannazzo, F.; Greco, G. Physics and Technology of Gallium Nitride Materials for Power Electronics. *Riv. del Nuovo Cim.* **2018**, *41*, 625, doi:10.1393/ncr/i2018-10154-x.

80. Roccaforte, F.; Greco, G.; Fiorenza, P.; Iucolano, F. An Overview of Normally-Off GaN-Based High Electron Mobility Transistors. *Materials (Basel).* **2019**, *12*, 1599, doi:10.3390/ma12101599.

81. Chung, J.W.; Roberts, J.C.; Piner, E.L.; Palacios, T. Effect of Gate Leakage in the Subthreshold Characteristics of AlGaN/GaN HEMTs. *IEEE Electron Device Lett.* **2008**, *29*, 1196–1198, doi:10.1109/LED.2008.2005257.

82. Roccaforte, F.; Fiorenza, P.; Greco, G.; Vivona, M.; Lo Nigro, R.; Giannazzo, F.; Patti,

A.; Saggio, M. Recent Advances on Dielectrics Technology for SiC and GaN Power Devices. *Appl. Surf. Sci.* **2014**, *301*, 9–18, doi:10.1016/j.apsusc.2014.01.063.

83. Daumiller, I.; Theron, D.; Gaquiere, C.; Vescan, A.; Dietrich, R.; Wieszt, A.; Leier, H.; Vetury, R.; Mishra, U.K.; Smorchkova, I.P.; et al. Current Instabilities in GaN-Based Devices. *IEEE Electron Device Lett.* **2001**, *22*, 62–64, doi:10.1109/55.902832.

84. Binari, S.C.; Ikossi, K.; Roussos, J.A.; Kruppa, W.; Doewon Park; Dietrich, H.B.; Koleske, D.D.; Wickenden, A.E.; Henry, R.L. Trapping Effects and Microwave Power Performance in AlGaN/GaN HEMTs. *IEEE Trans. Electron Devices* **2001**, *48*, 465–471, doi:10.1109/16.906437.

85. Vetury, R.; Zhang, N.Q.; Keller, S.; Mishra, U.K. The Impact of Surface States on the DC and RF Characteristics of AlGaN/GaN HFETs. *IEEE Trans. Electron Devices* **2001**, *48*, 560–566, doi:10.1109/16.906451.

86. Meneghesso, G.; Verzellesi, G.; Pierobon, R.; Rampazzo, F.; Chini, A.; Mishra, U.K.; Canali, C.; Zanoni, E. Surface-Related Drain Current Dispersion Effects in AlGaN–GaN HEMTs. *IEEE Trans. Electron Devices* **2004**, *51*, 1554–1561, doi:10.1109/TED.2004.835025.

87. Institute of Electrical and Electronics Engineers IEEE Standard Glossary of Software Engineering Terminology. *Office* **1990**, *121990*.

88. Ciappa, M. *Some Reliability Aspects of IGBT Modules for High-POwer Applications*; 2000; ISBN 3-89649-657-3.

89. Onuki, J.; Koizumi, M.; Suwa, M. Reliability of Thick Al Wire Bonds in IGBT Modules for Traction Motor Drives. *IEEE Trans. Adv. Packag.* **2000**, *23*, 108–112, doi:10.1109/6040.826768.

90. Hirschmann, D.; Tissen, D.; Schroder, S.; De Doncker, R.W. Reliability Prediction for Inverters in Hybrid Electrical Vehicles. *IEEE Trans. Power Electron.* **2007**, *22*, 2511–2517, doi:10.1109/TPEL.2007.909236.

91. Gopi Reddy, L.; Tolbert, L.; Ozpineci, B. Power Cycle Testing of Power Switches: A Literature Survey. *IEEE Trans. Power Electron.* **2014**, *30*, 2465–2473, doi:10.1109/TPEL.2014.2359015.

92. Kostandyan, E.E.; Sørensen, J.D. Physics of Failure as a Basis for Solder Elements Reliability Assessment in Wind Turbines. *Reliab. Eng. Syst. Saf.* **2012**, *108*, 100–107,

doi:10.1016/j.ress.2012.06.020.

93. Janicki, M.; Napieralski, A. Modelling Electronic Circuit Radiation Cooling Using Analytical Thermal Model. *Microelectronics J.* **2000**, *31*, 781–785, doi:10.1016/S0026-2692(00)00059-8.

94. Alessandrino, S.; Carbone, B.; Cordiano, F.; Mazza, B.; Russo, A.; Coco, W.; Boscaglia, M.; Salvo, A. Di; Lombardo, A.; Scarcella, D.; et al. Failure Analysis Addressing Method of Optically Undetected Defectivity on 4H-SiC PowerMOSFET Epitaxial Layer. In Proceedings of the 2022 IEEE International Reliability Physics Symposium (IRPS); IEEE, March 2022; pp. P61-1-P61-4.

95. Carbone, B.; Alessandrino, M.S.; Russo, A.; Vitanza, E.; Giannazzo, F.; Fiorenza, P.; Roccaforte, F. Carrot-like Crystalline Defects on the 4H-SiC PowerMOSFET Yield and Reliability. In Proceedings of the 2023 IEEE International Reliability Physics Symposium (IRPS); IEEE, March 2023; pp. 1–5.

96. Escobar, L.A.; Meeker, W.Q. A Review of Accelerated Test Models. *Stat. Sci.* **2006**, *21*, 552–577, doi:10.1214/088342306000000321.

97. Vodyakho, O.; Steurer, M.; Neumayr, D.; Edrington, C.S.; Karady, G.; Bhattacharya, S. Solid-State Fault Isolation Devices: Application to Future Power Electronics-Based Distribution Systems. *IET Electr. Power Appl.* **2011**, *5*, 521, doi:10.1049/iet-epa.2010.0258.

98. Essely, F.; Guitard, N.; Darracq, F.; Pouget, V.; Bafleur, M.; Perdu, P.; Touboul, A.; Lewis, D. Optimizing Pulsed OBIC Technique for ESD Defect Localization. *IEEE Trans. Device Mater. Reliab.* **2007**, *7*, 617–624, doi:10.1109/TDMR.2007.911381.

99. Nikawa, K.; Inoue, S.; Morimoto, K.; Sone, S. Failure Analysis Case Studies Using the IR-OBIRCH (Infrared Optical Beam Induced Resistance Change) Method. In Proceedings of the Proceedings Eighth Asian Test Symposium (ATS'99); IEEE Comput. Soc, 1999; pp. 394–399.

100. Wang, Y.; Zhu, Q.; Huang, C. `Failure Analysis of Short-Circuit Failure of Metal-Oxide-Metal Capacitor. *Microelectron. Reliab.* **2022**, *137*, 114691, doi:10.1016/j.microrel.2022.114691.

101. Yang, H.; Chen, R.; Han, J.; Liang, Y.; Ma, Y.; Wu, H. Preliminary Study on the Model of Thermal Laser Stimulation for Defect Localization in Integrated Circuits. *Appl. Sci.* **2020**, *10*, 8576, doi:10.3390/app10238576.

102. Chauhan, P.S.; Choubey, A.; Zhong, Z.; Pecht, M.G. *Copper Wire Bonding*; Springer New York: New York, NY, 2014; ISBN 978-1-4614-5760-2.

103. Chen, J.; Degryse, D.; Ratchev, P.; DeWolf, I. Mechanical Issues of Cu-to-Cu Wire Bonding. *IEEE Trans. Components Packag. Technol.* **2004**, *27*, 539–545, doi:10.1109/TCAPT.2004.831745.

104. Picardi, M.F.; Nimje, K.N.; Papadakis, G.T. Dynamic Modulation of Thermal Emission—A Tutorial. *J. Appl. Phys.* **2023**, *133*, doi:10.1063/5.0134951.

105. Zhu, H.; Li, Q.; Zheng, C.; Hong, Y.; Xu, Z.; Wang, H.; Shen, W.; Kaur, S.; Ghosh, P.; Qiu, M. High-Temperature Infrared Camouflage with Efficient Thermal Management. *Light Sci. Appl.* **2020**, *9*, 60, doi:10.1038/s41377-020-0300-5.

106. Gui, B.; Wang, J.; Lu, X.; Zhu, Y.; Zhang, L.; Feng, M.; Huang, W.; Wang, J.; Ma, H.; Qu, S. Spectrally-Switchable Infrared Selective Emitters for Adaptive Camouflage. *Infrared Phys. Technol.* **2022**, *126*, 104363, doi:10.1016/j.infrared.2022.104363.

107. JI, Q.; CHEN, X.; LAUDE, V.; LIANG, J.; FANG, G.; WANG, C.; ALAEE, R.; KADIC, M. Selective Thermal Emission and Infrared Camouflage Based on Layered Media. *Chinese J. Aeronaut.* **2023**, *36*, 212–219, doi:10.1016/j.cja.2022.08.004.

108. Fiorino, A.; Thompson, D.; Zhu, L.; Mittapally, R.; Biehs, S.-A.; Bezencenet, O.; El-Bondry, N.; Bansropun, S.; Ben-Abdallah, P.; Meyhofer, E.; et al. A Thermal Diode Based on Nanoscale Thermal Radiation. *ACS Nano* **2018**, *12*, 5774–5779, doi:10.1021/acsnano.8b01645.

109. Kathmann, C.; Reina, M.; Messina, R.; Ben-Abdallah, P.; Biehs, S.-A. Scalable Radiative Thermal Logic Gates Based on Nanoparticle Networks. *Sci. Rep.* **2020**, *10*, 3596, doi:10.1038/s41598-020-60603-4.

110. Li, Q.; He, H.; Chen, Q.; Song, B. Radiative Thermal Diode via Hyperbolic Metamaterials. *Phys. Rev. Appl.* **2021**, *16*, 064022, doi:10.1103/PhysRevApplied.16.064022.

111. Wang, S.; Cottrill, A.L.; Kunai, Y.; Toland, A.R.; Liu, P.; Wang, W.-J.; Strano, M.S. Microscale Solid-State Thermal Diodes Enabling Ambient Temperature Thermal Circuits for Energy Applications. *Phys. Chem. Chem. Phys.* **2017**, *19*, 13172–13181, doi:10.1039/C7CP02445B.

112. Huth, F.; Schnell, M.; Wittborn, J.; Ocelic, N.; Hillenbrand, R. Infrared-

Spectroscopic Nanoimaging with a Thermal Source. *Nat. Mater.* **2011**, *10*, 352–356, doi:10.1038/nmat3006.

113. Fan, S. Thermal Photonics and Energy Applications. *Joule* **2017**, *1*, 264–273, doi:10.1016/j.joule.2017.07.012.

114. Domenichini, G. Misure Di Temperatura Tramite Radiazione Infrarossa. *Bachelor Thesis* 24–27.

115. Ben-Abdallah, P.; Joulain, K. Fundamental Limits for Noncontact Transfers between Two Bodies. *Phys. Rev. B* **2010**, *82*, 121419, doi:10.1103/PhysRevB.82.121419.

116. Dey, T. Microplastic Pollutant Detection by Surface Enhanced Raman Spectroscopy (SERS): A Mini-Review. *Nanotechnol. Environ. Eng.* **2023**, *8*, 41–48, doi:10.1007/s41204-022-00223-7.

117. Houston, W. V.; Lewis, C.M. Rotational Raman Spectrum of CO 2. *Proc. Natl. Acad. Sci.* **1931**, *17*, 229–231, doi:10.1073/pnas.17.4.229.

118. Haken, H.; Wolf, H.C.; Soos, Z.G. Molecular Physics and Elements of Quantum Chemistry: Introduction to Experiments and Theory . *Phys. Today* **1997**, doi:10.1063/1.881653.

119. Claron Hoskins, L. Pure Rotational Raman Spectroscopy of Diatomic Molecules. *J. Chem. Educ.* **1975**, doi:10.1021/ed052p568.

120. Breaux, L.; Singh, B. Automatic Defect Classification System for Patterned Semiconductor Wafers. In Proceedings of the Proceedings of International Symposium on Semiconductor Manufacturing; IEEE, 1995; pp. 68–73.

121. Albawi, S.; Mohammed, T.A.; Al-Zawi, S. Understanding of a Convolutional Neural Network. In Proceedings of the 2017 International Conference on Engineering and Technology (ICET); IEEE, August 2017; pp. 1–6.

122. Song, Y.Y.; Lu, Y. Decision Tree Methods: Applications for Classification and Prediction. *Shanghai Arch. Psychiatry* **2015**, *27*, 130–135, doi:10.11919/j.issn.1002-0829.215044.

123. Nakazawa, T.; Kulkarni, D. V. Anomaly Detection and Segmentation for Wafer Defect Patterns Using Deep Convolutional Encoder–Decoder Neural Network Architectures in Semiconductor Manufacturing. *IEEE Trans. Semicond. Manuf.* **2019**, *32*, 250–256, doi:10.1109/TSM.2019.2897690.

124. Kizilyalli, I.C.; Bui-Quang, P.; Disney, D.; Bhatia, H.; Aktas, O. Reliability Studies of Vertical GaN Devices Based on Bulk GaN Substrates. *Microelectron. Reliab.* **2015**, *55*, 1654–1661, doi:10.1016/j.microrel.2015.07.012.

125. Feng, Z.C.; Wang, W.; Chua, S.J.; Zhang, P.X.; Williams, K.P.J.; Pitt, G.D. Raman Scattering Properties of GaN Thin Films Grown on Sapphire under Visible and Ultraviolet Excitation. *J. Raman Spectrosc.* **2001**, *32*, 840–846, doi:10.1002/jrs.765.

126. Zhang, J.M.; Ruf, T.; Cardona, M.; Ambacher, O.; Stutzmann, M.; Wagner, J.-M.; Bechstedt, F. Raman Spectra of Isotopic GaN. *Phys. Rev. B* **1997**, *56*, 14399–14406, doi:10.1103/PhysRevB.56.14399.

127. Sugie, R.; Uchida, T. Determination of Stress Components in 4H-SiC Power Devices via Raman Spectroscopy. *J. Appl. Phys.* **2017**, *122*, 195703, doi:10.1063/1.5003613.

128. Lee, C.J.; Pezzotti, G.; Okui, Y.; Nishino, S. Raman Microprobe Mapping of Residual Microstresses in 3C-SiC Film Epitaxial Lateral Grown on Patterned Si(1 1 1). *Appl. Surf. Sci.* **2004**, *228*, 10–16, doi:10.1016/j.apsusc.2004.01.052.

129. Xu, Z.; He, Z.; Song, Y.; Fu, X.; Rommel, M.; Luo, X.; Hartmaier, A.; Zhang, J.; Fang, F. Topic Review: Application of Raman Spectroscopy Characterization in Micro/Nano-Machining. *Micromachines* **2018**, *9*, doi:10.3390/mi9070361.

130. Choi, S.; Heller, E.; Dorsey, D.; Vetury, R.; Graham, S. Analysis of the Residual Stress Distribution in AlGaN/GaN High Electron Mobility Transistors. *J. Appl. Phys.* **2013**, *113*, doi:10.1063/1.4794009.

131. Ma, L.; Qiu, W.; Fan, X. Stress/Strain Characterization in Electronic Packaging by Micro-Raman Spectroscopy: A Review. *Microelectron. Reliab.* **2021**, *118*, 114045, doi:10.1016/j.microrel.2021.114045.

132. Kamarudzaman, A.; Abu Bakar, A.S. Bin; Azman, A.; Omar, A.Z.; Supangat, A.; Talik, N.A. Positioning of Periodic AlN/GaN Multilayers: Effect on Crystalline Quality of a-Plane GaN. *Mater. Sci. Semicond. Process.* **2020**, *105*, doi:10.1016/j.mssp.2019.104700.

133. Maize, K.; Pavlidis, G.; Heller, E.; Yates, L.; Kendig, D.; Graham, S.; Shakouri, A. High Resolution Thermal Characterization and Simulation of Power AlGaN/GaN HEMTs Using Micro-Raman Thermography and 800 Picosecond Transient Thermoreflectance Imaging. *Tech. Dig. - IEEE Compd. Semicond. Integr. Circuit Symp. CSIC* **2014**, doi:10.1109/CSICS.2014.6978561.

134. Rieger, W.; Metzger, T.; Angerer, H.; Dimitrov, R.; Ambacher, O.; Stutzmann, M. Influence of Substrate-Induced Biaxial Compressive Stress on the Optical Properties of Thin GaN Films. *Appl. Phys. Lett.* **1995**, *970*, 970, doi:10.1063/1.116115.

135. Zhao, D.G.; Xu, S.J.; Xie, M.H.; Tong, S.Y.; Yang, H. Stress and Its Effect on Optical Properties of GaN Epilayers Grown on Si(111), 6H-SiC(0001), and c-Plane Sapphire. *Appl. Phys. Lett.* **2003**, *83*, 677–679, doi:10.1063/1.1592306.

136. Kisielowski, C.; Krüger, J.; Ruvimov, S.; Suski, T.; Ager, J.; Jones, E.; Liliental-Weber, Z.; Rubin, M.; Weber, E.; Bremser, M.; et al. Strain-Related Phenomena in GaN Thin Films. *Phys. Rev. B - Condens. Matter Mater. Phys.* **1996**, *54*, 17745–17753, doi:10.1103/PhysRevB.54.17745.

137. Beechem, T. Metrology of GaN Electronics Using Micro-Raman Spectroscopy. *Thesis* **2008**.

138. Tripathy, S.; Chua, S.J.; Chen, P.; Miao, Z.L. Micro-Raman Investigation of Strain in GaN and AlxGa1−xN/GaN Heterostructures Grown on Si(111). *J. Appl. Phys.* **2002**, *92*, 3503–3510, doi:10.1063/1.1502921.

139. Harima, H. Properties of GaN and Related Compounds Studied by Means of Raman Scattering. *J. Phys. Condens. Matter* **2002**, *14*, doi:10.1088/0953-8984/14/38/201.