Investigation of Gate Direct-Current and Fluctuations in Organic p-Type Thin-Film Transistors

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***Abstract*— Investigation of gate dielectric conduction properties in organic p-type staggered thin-film transistors is reported by means of direct-current, capacitance–voltage, and noise measurements. Results suggest that transport in the CYTOP^{TM} gate dielectric is dominated, at low currents, by Schottky conduction due to the emission at the aluminum gate interface through a barrier $\phi_B \approx 1$ eV, while is limited, at higher currents, by space-charge conduction in the trap-limited regime with an effective mobility $\mu\theta$ estimated in the order of 10^{-9} cm^2/(Vs). Gate current noise follows a $1/f$ law and it is found to be proportional to I_G^2, which is inconsistent with the commonly assumed mobility fluctuation. Traps responsible for gate noise are dielectric-bulk traps, not located at the semiconductor interface, since the gate noise is found to be uncorrelated with drain noise.**

***Index Terms*— Organic TFT, low frequency noise, low frequency noise measurements, gate noise.**

I. Introduction

ORGANIC thin film transistors (OTFTs) have captured a large space in the electronics market due to the particular mechanical properties of organic materials which make OTFTs suitable for applications in the field of flexible-electronics, such as sensors and displays [1]. Extensive investigation of direct-current (DC) and noise properties of OTFTs has been reported in recent years. However this analysis has been limited to the study of the drain current, hence on the electrical properties of the semiconductor (the active layer) and of the semiconductor/dielectric interface. Minor attention has been devoted to the conduction properties of the gate dielectric. In this work we investigate the conduction properties of the gate dielectric (CYTOP^{TM}) in p-type staggered top-gate OTFTs by gate DC, capacitance-voltage (CV) and gate noise measurements. Gate noise has the major advantage, with respect to drain noise, that it is sensible to defects located in the entire gate stack and not only close to the channel-dielectric interface as is the case of drain noise [2]–[6]. To our knowledge no previous work regarding neither gate DC nor gate noise in OTFTs has been reported so far. Thanks to a purposely designed high-sensitivity instrumentation system [7], [8] we were able to measure the gate noise at the low gate DC level of OTFTs (pA÷nA range).

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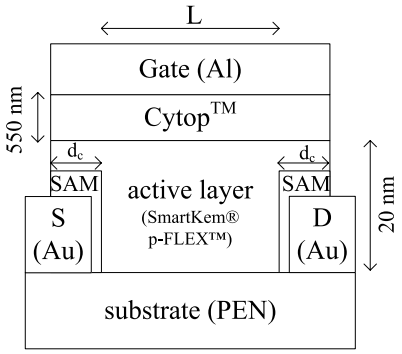

Fig. 1. Device structure (not in scale) of the investigated p-type OTFT

II. Device Structure

OTFTs, with staggered top-gate configuration (Fig. 1a), were fabricated on flexible (125 μm thick) polyethylene-naphtalate (PEN, DuPont Teijin Teonex® Q65HA) by using solution processed semiconductor and dielectric. Investigated devices have gate width (W) ranging from 70 to 220 μm and gate length (L) ranging from 2 to 100 μm. The organic semiconductor is SmartKem® p-FLEX™, 20 nm thick, while the gate dielectric is poly(perfluorobutenylvinylether), Cytop^{TM}, 550 nm thick and relative dielectric constant $\sim$2.1. Source and drain are made in Gold while the gate is in Aluminum. Source and drain contacts were pre-treated by a Self-Assembled Monolayer (SAM) of 2,3,4,5,6-pentafluorobenzenethiol and the total longitudinal overlap between the gate and source/drain is $2d_c \approx 50\mu$m (see Fig. 1). Due to processing requirements the semiconductor is present also below the gate contact pad which has an area equal to $A_{G,PAD} = (200\mu m)^2$. The total gate area is then $A_G = W(2d_c + L) + A_{G,PAD}$ and is dominated by $A_{G,PAD}$ so that, even in devices with strongly different WL, A_G is not so dissimilar. More processing details can be found in [10].

III. DC Measurements

Gate current (I_G) vs. gate voltage (V_G) measurements have been performed with the experimental setup presented in [7] and [8] with a bias delay of 1s. Fig. 2 shows a typical I_G-V_G curve (symbol) measured in a device with L=100 μm and W=120 μm. We were able to interpret the low-current regime and the higher current regime through two different

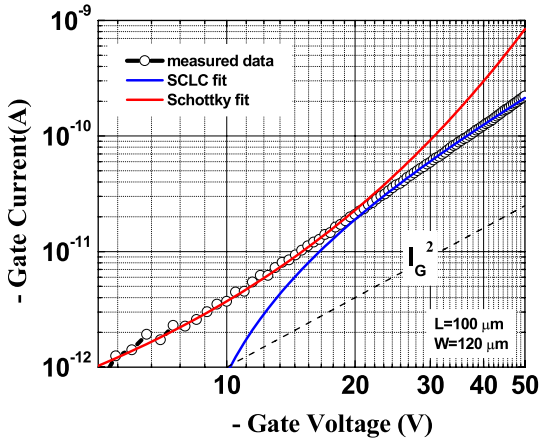

Fig. 2. I_G-V_G fit at low and high currents in a device with L = 100 μm and W = 120 μm. Low current regime fits well with Schottky emission, while the high current range fits well with space-charge limited conduction.

physical mechanisms. Since the semiconductor thickness is much thinner with respect to the dielectric thickness (t_{ox}), it is reasonable to assume that the gate voltage appears entirely across the dielectric. The low-current range fits well with Schottky conduction [11] (red fit in Fig. 2), that is $\ln(I_G) = a + b\sqrt{F_{ox}}$ where F_{ox} is the dielectric field (assumed constant) $F_{ox} \approx V_G/t_{ox}$, according to a barrier-height $\phi_B \approx 1$ eV. This value is consistent with the band-offset between the Aluminum gate (work-function $\approx$ 4eV) and CYTOP (electron affinity $\approx$ 2.8eV [12]) so that the measured gate current is most certainly due to electron injection from the gate to the CYTOP dielectric. Indeed hole injection from the semiconductor or from source/drain to the gate is less probable due to the large dielectric gap ($\approx$6.3eV [12]).

The higher current range of the measured I_G-V_G fits well with space-charge limited conduction (SCLC) [11] (blue fit in Fig. 2) where the current has a quadratic dependence with respect to the applied voltage. Space-charge currents have been already observed in organic layers [13]. At low injection the CYTOP is neutral, the dielectric field is constant, and the transport is dominated by the Schottky emission at the gate due to a non negligible barrier ($\approx$1eV) towards the CYTOP. As the injection level is sufficiently high, space-charge effect takes place and the transport in the CYTOP is limited by the drift of the injected charge. In the SCLC regime the field in the CYTOP is not constant due to the space-charge and controls, at the gate interface, the barrier lowering and Schottky emission. Stated in other words, the SCL current is a Schottky current controlled by an interfacial field $F_0 \neq V_G/t_{ox}$ generated by the space-charge. Gate current densities, in the SCL regime, have been averaged in order to extract the average effective mobility $\mu\theta$ where μ is the dielectric mobility and $\theta = n/n_{inj}$ is the fraction of the mobile charge (n) with respect the injected charge (n_{inj}). We estimated a value of $\mu\theta \approx 5 \cdot 10^{-9}$ cm^2/(Vs) which is consistent with other reports [13]. Since this value is much lower with respect to typical values of μ in organic layers, we have to assume that $\theta \ll 1$, meaning that the SCLC is limited by the thermal activation of dielectric traps (trap-limited regime).

IV. CV Measurements

Fig. 3 shows the scaled gate capacitance (C_G) measured at f=1kHz in several devices with different W and L as a function of V_G (source and drain grounded). Fig. 3(top) shows that the

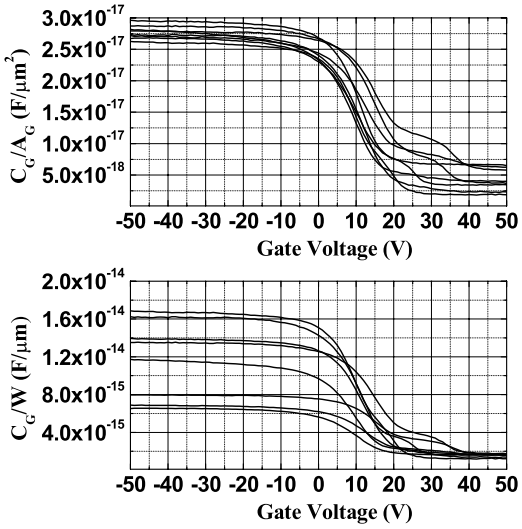

Fig. 3. Gate capacitance vs. gate voltage (at f=1kHz) in several devices with different W and L.

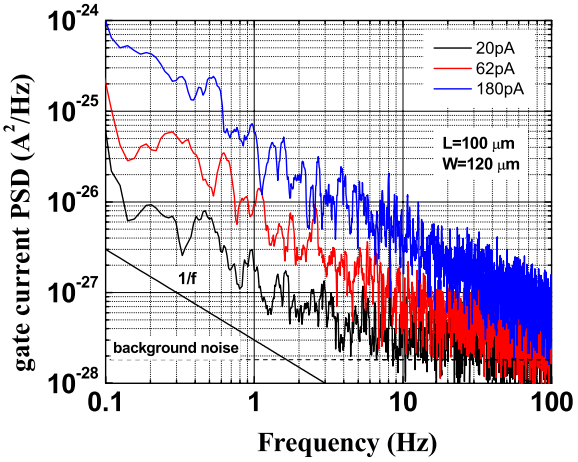

Fig. 4. Gate current PSD as a function of the frequency (device of Fig.2) for 3 different bias currents.

scaling with the gate area A_G works quite well in accumulation and that the measured C_G/A_G is very close to the theoretical oxide capacitance per unit area $\varepsilon_{ox}/t_{ox} \approx 3.38 \cdot 10^{-17}$ F/μm^2. This result is consistent with top gate injection, as discussed in Section III. Fig. 3(bottom) shows that, for positive V_G, the gate capacitance scales with W. In particular $C_G/W \approx \varepsilon_{ox}/t_{ox}.2d_c$, which is consistent with back injection from the overlap between source/drain and gate. We have to notice that the gate current is below the instrumentation background for positive V_G. This result is consistent with back hole injection from the overlap regions which is blocked by the large band offset between the contacts and the dielectrics.

V. Noise Measurements

The experimental setup for gate noise measurements is presented in [7] and [8]. Fig. 4 shows the measured power spectral density (PSD) of the gate current S_{IG} as a function of the frequency for 3 bias gate currents in the SCLC regime (same device of Fig. 2). The measured spectra show a clear $1/f^{\gamma}$ behavior with $\gamma \approx 1$, meaning that the noise is generated by a continuous distribution of dielectric traps. Fig. 5 shows S_{IG} (extrapolated at f = 1Hz) as a function of I_G in several

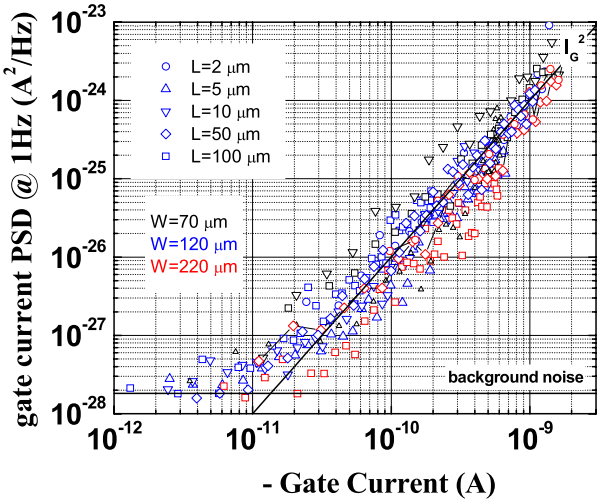

Fig. 5. Gate current noise PSD (at f = 1Hz) as a function of I_G in several devices with different W and L.

devices with different W and L. The scaled gate noise $S_{IG} \cdot A_G$ (not shown) shows a similar dispersion to S_{IG} consistent with a small effective gate area (A_G) variation even for devices with strong differences in WL. As can be observed in Fig. 4, the noise is proportional to I_G^2, that is S_{IG}/I_G^2 = constant. Let us observe that the measured noise is meaningful only in the current interval where the transport is limited by the space-charge effect (let us say > 10pA). In fact in the Schottky conduction range the noise is very low and the instrumentation background prevails. Current fluctuations associated to space-charge currents have been studied in the past [14] and they have been attributed to mobility fluctuation (MF). However we have to rule out MF as the main cause of current fluctuations. In fact the normalized noise (S_{IG}/I_G^2) due to MF has been found to be bias dependent, while we observed bias independence of S_{IG}/I_G^2. In terms of SCL current the only other possible source of noise is the fluctuation of the parameter $\theta = n/n_{inj}$ while, in terms of Schottky current, the noise may be generated by fluctuations of ϕ_B and/or F_0. Fluctuations of n_{inj} induced by ϕ_B could result in bias independency of S_{IG}/I_G^2. Gate current fluctuations, with S_{IG}/I_G^2 constant, induced by barrier fluctuations have been observed and modeled in MOSFETs [3], [5]. The fluctuations of ϕ_B may be generated, in OTFTs, by fluctuations of the dielectric trap occupancy.

Cross-correlation measurements in the linear region ($V_{DS} = -1V$) have been performed between drain and gate currents using a two-channel spectrum analyzer [8]. After M=1000 spectra-averages the resulting module (|C|) of the cross-correlation coefficient ($C = S_{IG,ID}/(S_{IG}S_{ID})^{1/2}$, where $S_{IG,ID}$ is the cross-spectrum between gate and drain currents and S_{ID} is the PSD of the drain current), is in the order of the "background noise" given by $1/\sqrt{M}$=0.03 at all investigated frequencies and bias. This result allows us to conclude that the microscopic physical origin of gate and drain noise are different. While drain noise is generated at the semiconductor-dielectric interface [9], [10] gate noise is generated away from the interface into the dielectric. This result is consistent with carrier injection from the gate.

VI. Summary and Conclusion

In this letter we reported, for the first time, gate DC and gate noise measurements in (p-type staggered) OTFTs. At low (negative) bias the gate current is dominated by Schottky conduction into the dielectric according to a barrier height of ≈1eV, while at higher (negative) bias the current is found to be consistent with SCLC according to an effective mobility $\mu\theta \approx 5 \cdot 10^{-9}$cm^2/(Vs), meaning that transport is limited by the activation of in-band dielectric traps. Both mechanisms are consistent with electron top injection from the gate. In the SCLC regime the field in the CYTOP is not constant and controls, at the gate interface, the barrier lowering and Schottky emission. Gate current noise follows a 1/f law and is proportional to I_G^2. Such behavior cannot be explained, in the SCLC context, by mobility fluctuation. A possible mechanism for gate noise is barrier height fluctuation induced by dielectric traps occupancy fluctuation. These traps are dielectric-bulk traps, not located at the semiconductor interface since the gate noise is found to be uncorrelated with drain noise. Future work will be devoted to modeling the gate noise in OTFTs.

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