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PhD in Engineering and Chemistry of Materials and Construction

Multi-Level Inverters exploiting an Open-end Winding configuration

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Introduction

Multilevel converters are becoming more and more popular, overcoming some key limitations of conventional two-level structures in handling medium voltages and high voltage gradients. Today they provide the ground for the realization of high efficiency energy conversion systems for medium voltage applications, such as pumps, compressors, extruders, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, wind energy conversion, and railway traction. A detailed overview of multilevel converters is provided in Chapter 1, while, the state of the art of Open-end Winding Systems is described in Chapter 2. The last systems can be considered as special multilevel inverter structures, tailored around an electrical machine fed from both the ends of the stator, or primary, winding. Overvoltage phenomena generated in industrial motor drives at motor terminals by long feeding cables are investigated in Chapter 3 and an Open-end Winding configuration approach is presented to actively mitigate them. Moreover, an adaptive algorithm is described to make independent the active overvoltage mitigation from system parameters. The main contribution of this work is the development of a new multilevel inverter topology, the Asymmetrical Hybrid Multilevel Inverter (AHMLI), which is introduced in Chapter 4. According to the AHMLI structure, an open end winding machine (motor, generator or transformer) is supplied on one end by a main multilevel converter, fully managing the active power stream, and, on the other end by an auxiliary two level inverter. This acts as an active power filter, suitably shaping the electrical machine phase current. A mathematical analysis of the proposed structure is first provided, followed by an exhaustive comparison between AHMLI and conventional multilevel structures, emphasizing advantages in terms of efficiency and output current THD. Voltage and current control systems, optimally coping with key characteristics of the AHMLI structure are carried out and an original input capacitors voltage equalization technique is also presented. The application of the AHMLI concept to industrial induction motor drives is then evaluated by simulation and experimental test. A possible exploitation of the AHMLI approach in the realization of photovoltaic and wind plants, as well as STATCOM devices is also assessed. Moreover, a high efficiency three phase rectifier for high speed generation systems exploiting the AHMLI configuration is carried out. Finally, the application of the AHMLI approach to Multiple Motor Drive systems is proposed in Chapter 5. Two new topologies are presented, namely: Open-end Winding Multi Motor Single Converter (MMSC) and Open-end Winding Multi Motor Multi Converter (MMMC). Both configurations exploit the

AHMLI structure but the MMMC exploits a five-leg two level inverter to independently control the stator currents of two induction motors.

1 Chapter: State of the Art of Multilevel Converters

Multilevel converters are today successfully exploited in many industrial applications such as pumps, compressors, extruders, fans, grinding mills, rolling mills, conveyors, crushers, blast furnace blowers, gas turbine starters, mixers, mine hoists, reactive power compensation, marine propulsion, high-voltage direct-current (HVDC) transmission, hydro pumped storage, wind energy conversion, and railway traction [1]-[10]. However, such a technology is still under development, and many new contributions and new circuital topologies have been proposed in the last few years. Many publications of tutorial nature have recently addressed the multilevel converter technology, emphasizing the growing importance of multilevel converters for high-power applications [4]-[9]. These works cover in depth traditional and well-established multilevel converter topologies, such as the neutral point clamped (NPC), cascaded H-bridge (CHB), and flying capacitor (FC), as well as specific modulation strategies. The most attractive features of multilevel inverters, over conventional two-level inverters, are:

- MLIs can generate output voltages with low distortion in term of Total Harmonic Distortion THDv;
- MLIs draw input current with very low distortion in term of THDi;
- MLIs generate output voltages with lower *dv/dt*, thus reducing the voltage stress across power devices and at the same time mitigating overvoltages at the load terminals;
- MLIs generate smaller common-mode voltage CMVs, thus reducing the bearing currents. Additional modulation methods can be adopted in order to eliminate the CMVs;
- MLIs can operate with a lower switching frequency.

In this chapter an overview of classic multilevel topologies is presented, together with the latest developments of multilevel modulation strategies. A particular attention is also played to multilevel converter control and operational issues, such as harmonic elimination and DC Bus capacitors voltage balancing.

1.1 Standard Multilevel inverter topologies

The development of the multilevel converter technology was started in the late 1960s with the introduction of a series-connected H-bridge converter with a multilevel stepped waveform voltage modulation, which became the H-Bridge converter (CHB) topology [11]. This was closely followed by low-power development of a Flying Capacitor (FC) converter topology [12]. In the late 1970s, the Diode-Clamped Converter (DCC)

[13] has been first introduced, that is today known as Neutral Point Clamped (NPC) inverter. This last has been proposed in [14], [15] and it can be considered as the first real multilevel power converter for medium-voltage applications. In the late 1980s [16], the CHB has been reintroduced although it reached more industrial relevance in the mid-1990s [17]. In the same way, in the early 1990s, the original low power FC converter evolved to the medium-voltage multilevel converter topology we know today [18]. Through the years, the FC has also been reported as the imbricated-cell and multi-cell converter. CHB, NPC and FC multilevel converters are considered now as the classic or traditional multilevel topologies and their development turned out in industrial products during the last two decades, Fig. 1. 1. These converters are today produced by several firms [19]–[34], offering different power ratings, front-end configurations, cooling systems, semiconductor devices, and control schemes. The most relevant parameters and ratings for each classic topology are listed in Table 1.1.

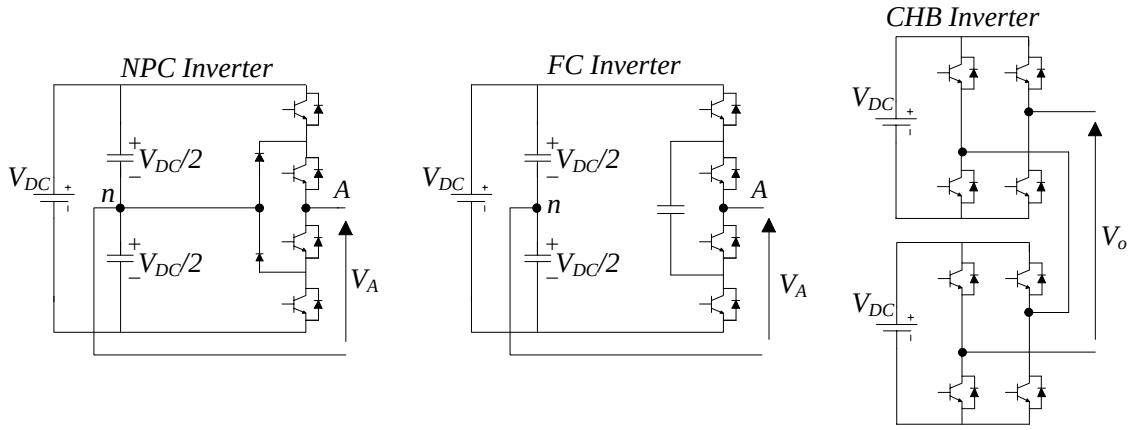

Fig. 1. 1 Standard Multilevel inverter topologies: Three-level NPC inverter 3L-NPC (left). Three-level Flying Capacitor inverter 3L-FC (middle). Five-level CHB inverter (right)

Some major differences among NPC, CHB and FC inverters come apparent from Table 1.1:

- The NPC features medium-/high-voltage devices (integrated gate-commutated thyristor (IGCT) and medium/high-voltage insulated-gate bipolar transistors (IGBTs)), whereas the CHB exclusively uses low-voltage IGBTs (LV-IGBTs).
- The CHB reaches higher voltage and higher power levels. The NPC is also definitely more suitable for back-to-back regenerative applications.
- The CHB needs a substantially higher number of devices to achieve a regenerative option (a three-phase two-level voltage source inverter (VSI) per cell).

- The CHB needs a phase-shifting transformer, usually conforming a 36-pulse rectifier system. This is more expensive but improves the input power quality. The NPC has a simpler circuit structure, leading to a smaller footprint.
- Although the three topologies generate the same amount of voltage levels when using the same number of power switches, commercially available CHBs shows more output voltage levels (up to 17, compared with three for the NPC). Hence, lower average device switching frequencies are possible for the same output voltage waveform quality. Therefore, air cooling and higher fundamental output frequency can be achieved without efficiency derating and without using of an output filter.

Table 1.1 Classic multilevel topology commercial ratings and specifications

Parameters	Multilevel Topologies		
	3L-NPC	CHB	4L-FC
Max Power	27MW[1], 31.5MVA[2], 40MVA[3], 44MW[4] 33.6MW[5], 3.7MW[6,9], 27MVA[8], 10MW[14]	120MW[2], 15MW[3], 40MVA[7] 10MVA[10], 11.1MVA[11], 6MVA[12], 6.2MW[13]	2.2MW[15],
Output Voltage [kV]	2.3/3.3/4/4.16[1,2], 2.3/3.3/4.16[4,6,8,9,14] 3.3/6.6[5]	2.3-13.8[2], 3.3/6.6[3,12], 2.3/4.16/6/11[5] 3/6/10[10], 3/4/6/10[11], 3/3.3/4.16/6.6/10[13]	2.3/3.3/4.16[15]
Max Output Freq. [Hz]	82.5[1], 250[2], 90[3], 140[4,14], 300[5]), 120[6]	330[2], 120[3,7,11-13], 50[10]	120[15]
Diode front-end	12/24[1-5,8], 24[6], 12/18[9], 12/24/36[14]	18/36[2,3,12], 30[7], 36[11], 24/30/42/48[13]	18/24[15]
Active front-end option	3L-NPC in back to back[1-5,8,14]	3-phase VSI per cell[10]	4L back to back[15]
Power semiconductor	IGCT[1,2,4,8], MV/HV IGBT[2,5,8,9,14] IEGT[3,8],	LV IGBT[2,3,7,10-13]	MV-IGBT[15]
Cooling system	Air/water[1,2,4,8,14], water[3,5], air[9]	Air/water[2,13], air[3,7,11,12]	air[15]
Modulation method	PWM[2-6,14], SHE[3,9], SVM[8,9]	PS-PWM[2,3,7,10-13]	PS-PWM[15]
Control method	DTC[1], v/f and FOC[2-4,14], FOC[5,6,8] v/f[9], DPC[4], VOC[2-5,8,14]	v/f and FOC[2,3,7,11,12], FOC[10,13]	v/f and FOC[15]
Voltage levels	3	9/13[2], 7/13[3,12], 11[7], 7/11/13/19[10]	4[15]
Power cells	-	4/6[2], 3/6[3,12], 5[7], 3/5/6/9[10]	3[15]

[1][11], [2][12], [3][13], [4][14], [5][15], [6][16], [7][17], [8][18],[9][19], [10][20], [11][21], [12][22], [13][23], [14][24], [15][25]

A classification of multilevel converter topologies is shown in Fig. 1. 2. Generally, the medium-voltage sector ranges from 2.3 to 6.6kV and high power sector ranges from 1 to 50MW. The classification also includes direct AC-AC converters and current source converters as cycloconverter and load commutated inverters (LCIs) for very high power, high torque, low speed applications and pulsewidh-modulated current source inverter for high power variable speed drives. The three standard topologies are compared in [35]–[37] in terms of losses and output voltage quality. The 3L-NPC has become quite popular because of a simple transformer rectifier power circuit structure, with a lower device count when considering both the inverter and rectifier, and less capacitors. Although the NPC concept can be extended to structures with higher number of levels, these are less attractive because of higher losses and uneven distribution of losses in the outer and inner devices [5]. In particular, DC-link capacitor voltage balance becomes unattainable in higher level topologies with a passive front end when using conventional modulation strategies [38]–[40]. In this case, the classic multilevel stepped waveform cannot be retained, and higher *dv/dts* (more-than one-level transitions) is necessary to balance the capacitors for certain modulation indexes.

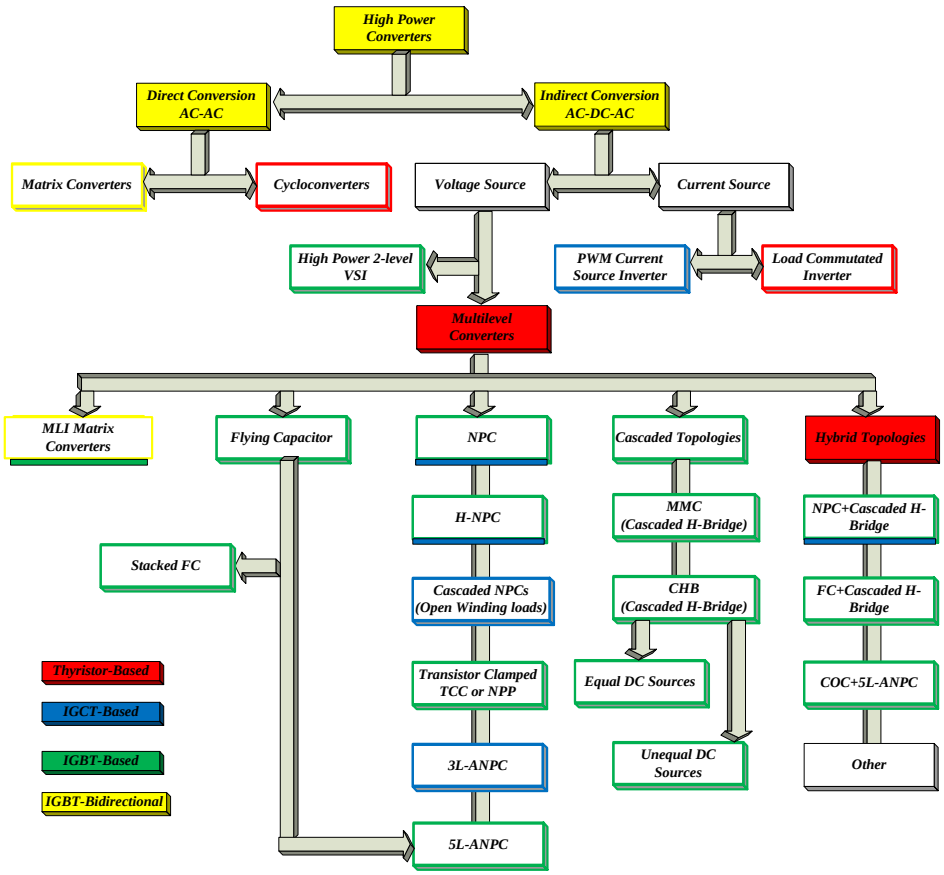

Fig. 1. 2 Multilevel Converter classification

On the other hand, the CHB is well suited for high-power applications because of the modular structure that enables higher voltage operation with classic low-voltage semiconductors. The phase shifting of the carrier

signals moves the harmonics to the higher frequency range, and this, together with the high number of levels, enables the reduction of the average device switching frequency (≤ 500 Hz), allowing air cooling and lower losses. However, it requires a large number of isolated DC sources, which have to be fed from phase-shifting isolation transformers, which are more expensive and bulky, compared with the standard transformer used for the NPC.

Although the FC is modular in structure, like the CHB, it has found less favor, compared to the NPC and CHB, mainly because higher switching frequencies are necessary to keep capacitor voltages properly balanced, whether a self-balancing or a control-assisted balancing modulation method is used (e.g., greater than 1200 Hz) [5]. So high switching frequencies are not feasible in high-power applications, where power switch limitations usually restrict the frequency range on 500–700 Hz. This topology also requires a proper initialization of the FC voltages.

1.1.1 Neutral Point Clamped Inverter

The conventional 3L-NPC inverter is shown in Fig. 1. 3. The DC-Bus voltage V_{DC} is split into three levels by two series-connected bulk capacitors C_1 and C_2. The middle point of the two capacitors *n* is defined as the neutral point. In order to show the switching states, a single phase 3L-NPC inverter and its associated output voltage waveform V_{An} are considered in Fig. 1. 4. The output voltage V_{An} assumes three voltage levels: $V_{DC}/2$, $-V_{DC}/2$ and *0*, as depicted in Tab. 1.2. For voltage level $V_{DC}/2$, switches S_{a1} and S_{a2} need to be turned on; for voltage level $-V_{DC}/2$, switches S_{a3} and S_{a4} need to be turned on and for the 0-voltage level, switches S_{a2} and S_{a3} need to be turned on. The key components that distinguish this topology from a conventional two-level inverter are the clamped diode D_{a1} and D_{a2}.

These two diodes clamp the switch voltage to half of the DC-Bus voltage. When both S_{a1} and S_{a2} turn on, the voltage across A and 0 is V_{DC}, i.e., $V_{AO}=V_{DC}$. In this case, D_{a2} balances out the voltage sharing between S_{a3} and S_{a4} with S_{a3} blocking the voltage across C_1 and S_{a4} blocking the voltage across C_2. The difference between V_{An} and V_{AO} is the voltage across C_2, which is $V_{DC}/2$.

Fig. 1. 5 shows a 5L-NPC inverter and their switching states. In this case, the DC-Bus consists of four capacitors C_1, C_2, C_3 and C_4. Assuming a V_{DC} DC-Bus voltage, the voltage across each capacitor is $V_{DC}/4$, and the voltage stress on each device will be limited to $V_{DC}/4$ through clamping diodes. Fig. 1. 6 shows the output voltage waveform which consists of four voltage levels: $V_{DC}/2$, $V_{DC}/4$, *0*, $-V_{DC}/4$ and $-V_{DC}/2$. In order to obtain the $V_{DC}/2$ voltage level, switches S_{a1}, S_{a2}, S_{a3} and S_{a4} need to be turned on, while, $V_{DC}/4$, is generated by

turning on switches S_{a2}, $S_{a3,}$ S_{a4} and S_{a5}. Voltage levels *0* and -V_{DC} */4* are respectively obtained by turning on switches S_{a3}, $S_{a4,}$ S_{a5}, S_{a6} and S_{a4}, $S_{a5,}$ S_{a6}, S_{a7}. Finally, by turning on S_{a5}, $S_{a6,}$ S_{a7} and S_{a8} a -V_{DC} */2* voltage is produced.

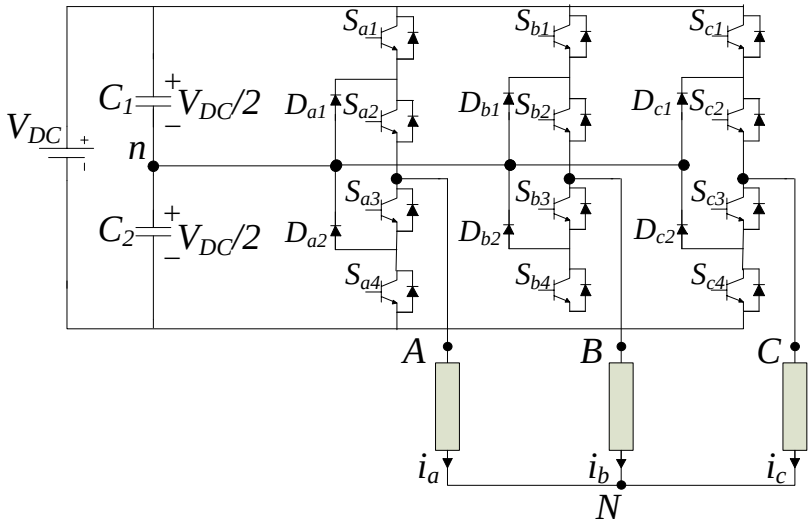

Fig. 1. 3 Conventional three-phase 3L-NPC inverter

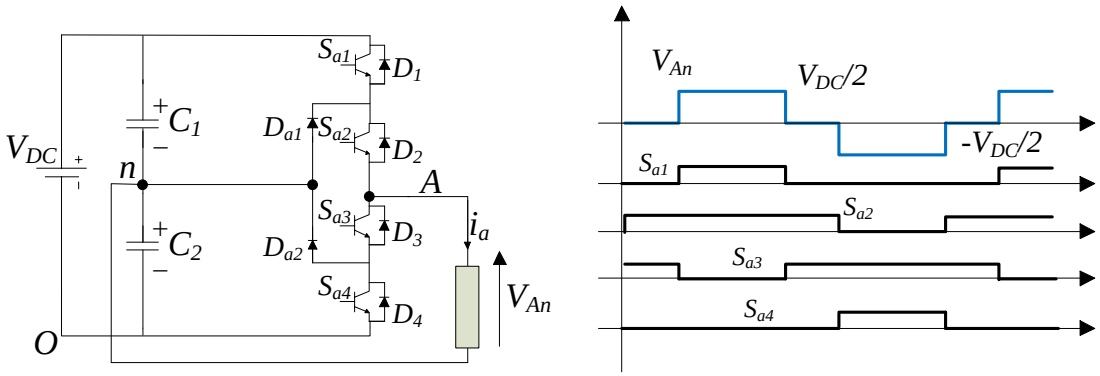

Fig. 1. 4 Conventional single-phase 3L-NPC inverter and associated waveform

Table 1.2 Switching states for a 3L-NPC inverter

S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{An}	Component conduction
1	1	0	0	V_{DC} */2*	If i_a>0 $S_{a1,}$ S_{a2} If i_a<0 $D_{1,}$ D_2
0	1	1	0	*0*	If i_a>0 $D_{a1,}$ S_{a2} If i_a<0 $D_{a2,}$ S_{a3}
0	0	1	1	-V_{DC} */2*	If i_a>0 $D_{4,}$ D_3 If i_a<0 $S_{a3,}$ S_{a4}

A *p*-phase *n*-level NPC inverter is equipped with *2p(n-1)* switching devices, *p(n-1)(n-2)* clamping diodes and *(n-1)* capacitors. Although each active device is only required to block a V_{DC} */(n-1)* voltage, the clamping diodes must have different voltage ratings to cope with reverse voltage blocking. For example, when lower

devices S_{a5}, S_{a6}, S_{a7} and S_{a8} are turned on, D_{a2} needs to block three capacitor voltage, or $3V_{DC}/4$. Notice that when the number of voltage levels n is sufficiently high, the number of switching devices and diodes will make the system impractical to implement.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{AO}
1	1	1	1	0	0	0	0	V_{DC}
0	1	1	1	1	0	0	0	$3V_{DC}/4$
0	0	1	1	1	1	0	0	$V_{DC}/2$
0	0	0	1	1	1	1	0	$V_{DC}/4$
0	0	0	0	1	1	1	1	0

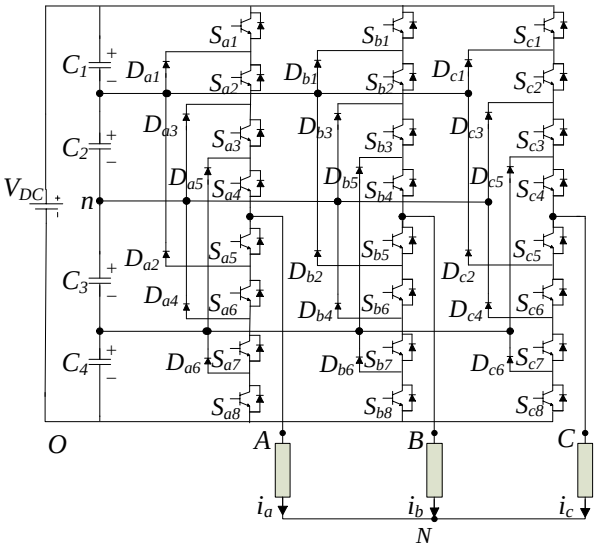

Fig. 1. 5 Switching States for a conventional three-phase 5L-NPC inverter

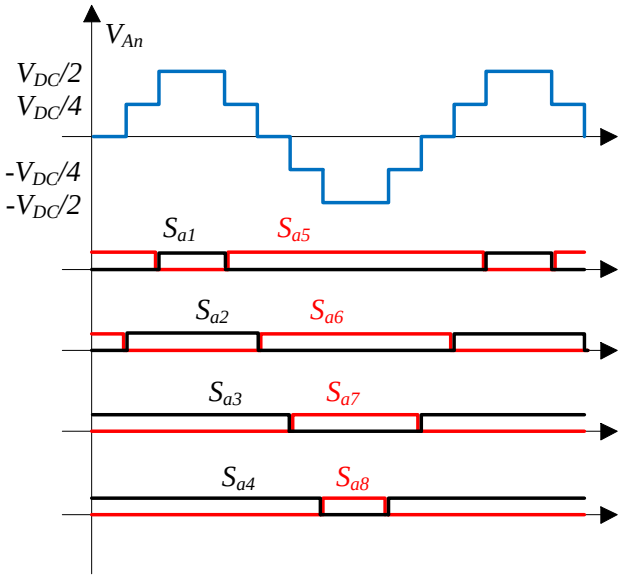

Fig. 1. 6 Output voltage waveform for a 5L-NPC inverter

1.1.2 Flying Capacitor Inverter

Fig. 1. 7 depicts the fundamental building block of a three-phase three-level flying capacitor inverter. A major advantage of this topology is that it eliminates the clamping diode issues typical of the NPC topology. Additionally, this topology naturally limits the *dv/dt* stress across the devices and introduces additional

switching states that can be used to maintain the charge balance in the capacitors. Unlike the NPC, the FC topology has enough switching states to control the charge balance on each leg, even if the phase current is unidirectional. The voltage change between two adjoining capacitor legs gives the size of the voltage steps in the output waveform.

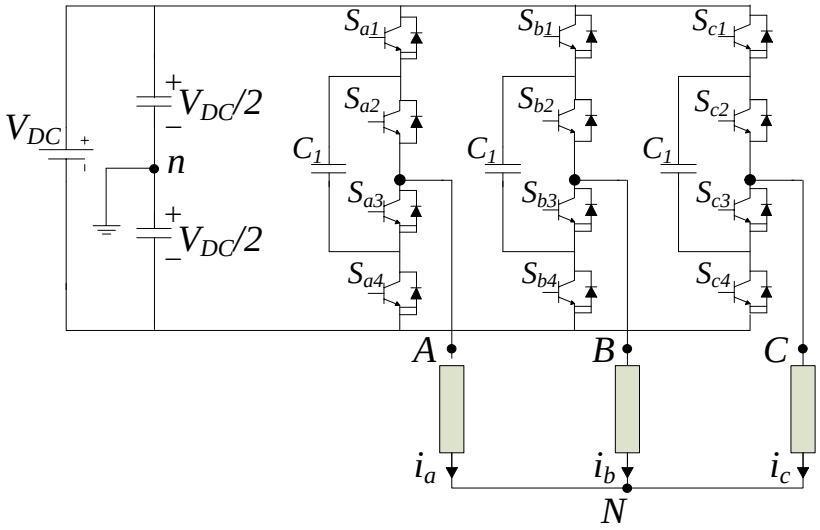

Fig. 1. 7 Conventional three-phase 3L-FC inverter

The output voltage inverter V_{An} in Fig. 1. 8 assumes three voltage levels: $V_{DC}/2$, $-V_{DC}/2$ and *0*. In order to obtain $V_{DC}/2$, switches S_{a1} and S_{a2} need to be turned on, while $-V_{DC}/2$, is produced by turning on switches S_{a3} and S_{a4} and a 0-voltage level is obtained by turning on S_{a1}-S_{a3} or S_{a2}-S_{a4}. Clamping capacitor C_1 is charged when S_{a1} and S_{a3} are turned on, and is discharged when S_{a2} and S_{a4} are turned on. The charge of C_1 can be balanced by proper selection of the 0-level switch combination. Major advantages of the FC-MLI topology consist in making unnecessary the filter and the control of active and reactive power flows through phase redundancies.

However, troubles related to the capacitors voltage balance, as well as, to the initial capacitors charge procedure, in addition to a larger number of capacitors, disadvantage this topology. Moreover, on a FC inverter, capacitor voltages must be maintained within suitable limits. Thus, the capacitance of flying capacitors increases almost inversely with the switching frequency, making the FC topology impractical at low and medium switching frequencies (≥ 1500-1800 Hz).

The voltage synthesis in a 5L-FC converter has more flexibility than a NPC converter. Fig. 1. 9 shows a 5L-FC topology and the switching states. As an example, using the last diagram, the voltage of a five-level phase-leg *A* output referred to the neutral point *n*, V_{An}, can be synthesized by the following switch combinations.

1. Voltage level $V_{DC}/2$*:* all upper switches S_{a1}-S_{a4} are turned on.

2. Voltage level $V_{DC}/4$: three possible combinations exist: a) S_{a1}, S_{a2}, S_{a3}, S_{a5} are turned on and $V_{An}=V_{DC}/2$ of upper C_1's -$V_{DC}/4$ of C_1. b) S_{a2}, S_{a3}, S_{a4}, S_{a8} are turned on and $V_{An}= 3V_{DC}/4$ of C_3's, $V_{DC}/2$ of lower C_4's. c) S_{a1}, S_{a3}, S_{a4}, S_{a7} are turned on and $V_{An}= V_{DC}/2$ of upper C_4's, -$3V_{DC}/4$ of lower C_3's+ $V_{DC}/2$ of C_2's.
3. 0-voltage level: six combinations exist: a) S_{a1}, S_{a2}, S_{a5}, S_{a6} are turned on and $V_{An}= V_{DC}/2$ of upper C_4's -$V_{DC}/2$ of C_2's. b) S_{a3}, S_{a4}, S_{a7}, S_{a8} are turned on and $V_{An}= V_{DC}/2$ of C_2 -$V_{DC}/2$ of lower C_4. c) S_{a1}, S_{a3}, S_{a5}, S_{a7} are turned on and $V_{An}= V_{DC}/2$ of upper C_4's -$3V_{DC}/4$ of C_3's+ $V_{DC}/2$ of C_2's-$V_{DC}/4$ of C_1. d) S_{a1}, S_{a4}, S_{a6}, S_{a7} are turned on and $V_{An}= V_{DC}/2$ of upper C_4's -$3V_{DC}/4$ of C_3's+$V_{DC}/4$ of C_1. e) S_{a2}, S_{a4}, S_{a6}, S_{a8} are turned on and $V_{An}= 3V_{DC}/4$ of upper C_3's -$3V_{DC}/4$ - $V_{DC}/4$ of C_2's+$V_{DC}/4$ of C_1-$V_{DC}/2$ of lower C_4's. f) S_{a2}, S_{a3}, S_{a5}, S_{a8} are turned on and $V_{An}= 3V_{DC}/4$ of C_3's -$V_{DC}/4$ of C_1, $V_{DC}/2$ of lower C_4's.
4. Voltage level -$V_{DC}/4$: three possible combinations exist: a) S_{a1}, S_{a5}, S_{a6}, S_{a7} are turned on and $V_{An}=V_{DC}/2$ of upper C_4's -$3V_{DC}/4$ of C_3's. b) S_{a4}, S_{a6}, S_{a7}, S_{a8} are turned on and $V_{An}= V_{DC}/4$ of C_1, -$V_{DC}/2$ of lower C_4's. c) S_{a3}, S_{a5}, S_{a7}, S_{a8} are turned on and $V_{An}= V_{DC}/2$ of C_2's, -$V_{DC}/4$ of C_1-$V_{DC}/2$ of lower C_4's.
5. Voltage level -$V_{DC}/2$: all lower switches S_{a5}-S_{a8} are turned on.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{An}
1	1	0	0	$V_{DC}/2$
1	0	1	0	0
0	1	0	1	0
0	0	1	1	-$V_{DC}/2$

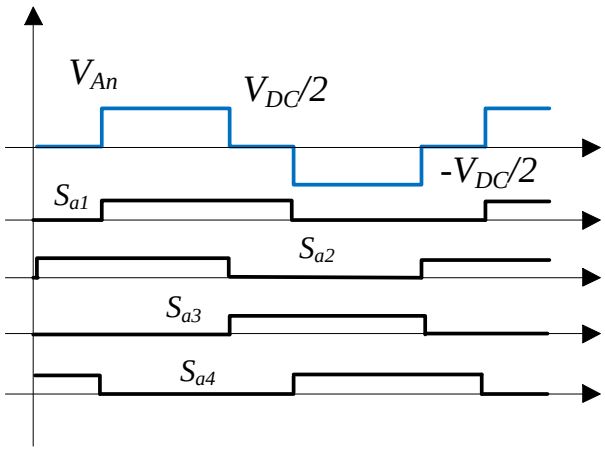

Fig. 1. 8 Switching states for a 3L-FC inverter

By proper selection of capacitor combinations, it is possible to balance the capacitor charge. Similarly, to the NPC inverter, the FC requires a large number of bulk capacitors to clamp the voltage. In an *n*-level structure, the FC inverter requires *(n-1)* DC-link capacitors and *(n-1) (n-2)/2* auxiliary capacitors per phase compared to NPC-MLI topology. The auxiliary capacitors are pre-charged to the voltage levels of V_{DC} /4, V_{DC} /2, 3 V_{DC} /4 respectively.

S_{a1}	S_{a2}	S_{a3}	S_{a4}	S_{a1}	S_{a2}	S_{a3}	S_{a4}	V_{AO}
1	1	1	1	0	0	0	0	V_{DC}
1	1	1	0	1	0	0	0	$3V_{DC}/4$
1	1	0	0	1	1	0	0	$V_{DC}/2$
1	0	0	0	1	1	1	0	$V_{DC}/4$
0	0	0	0	1	1	1	1	0

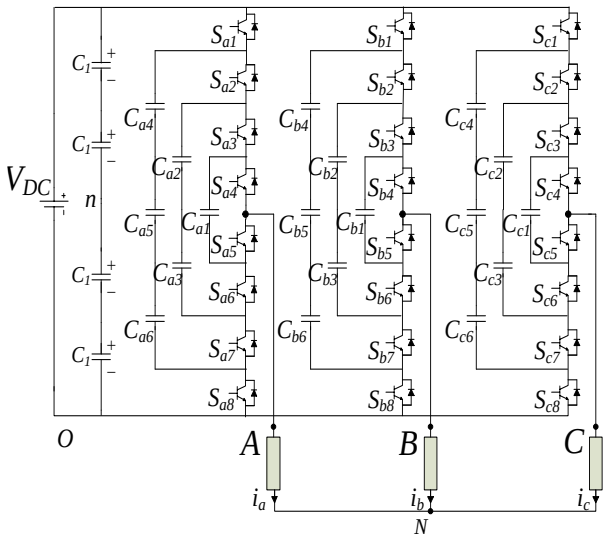

Fig. 1. 9 A conventional 5L-FC inverter with Switching states

1.1.3 Cascaded H-Bridge Inverters

As earlier mentioned, the cascaded H-bridge inverter (CHB) has been the first multilevel converter, developed in the late 1960s [11]. This topology is based on the series connection of single-phase inverters with separate DC sources [17]. Fig. 1. 10 shows a 5-level CHB inverter composed by two isolated H-bridge inverters.

The resulting phase voltage is synthesized by combination of the voltages generated by the cells. Each single-phase full-bridge inverter generates three output voltages levels: V_{DC}, $-V_{DC}$, and 0. This is made possible by connecting the capacitors sequentially to the AC side via the four power switches. The resulting output AC voltage swings from $-2V_{DC}$ to $2V_{DC}$ with 5 steps. The obtained staircase waveform is nearly sinusoidal, even without filtering. The switch power and the stored energy are reduced to about 80%, if compared to an NPC inverter.

However, a complex grid transformer, a large number of isolated power supplies, increased DC-link capacitances and a large number of semiconductor devices are major drawbacks of the CHB-MLI [41]-[42].

This topology has been used for active filter and reactive power compensation, electric vehicles, PV power conversion [42], Uninterruptible Power Supplies (UPSs), and magnetic resonance imaging etc. CHB-MLIs have been previously designed for static VAR compensators.

Main features of Neutral Point Clamped, Flying Capacitor and Cascaded H-Bridge are compared in Tab.1.3.

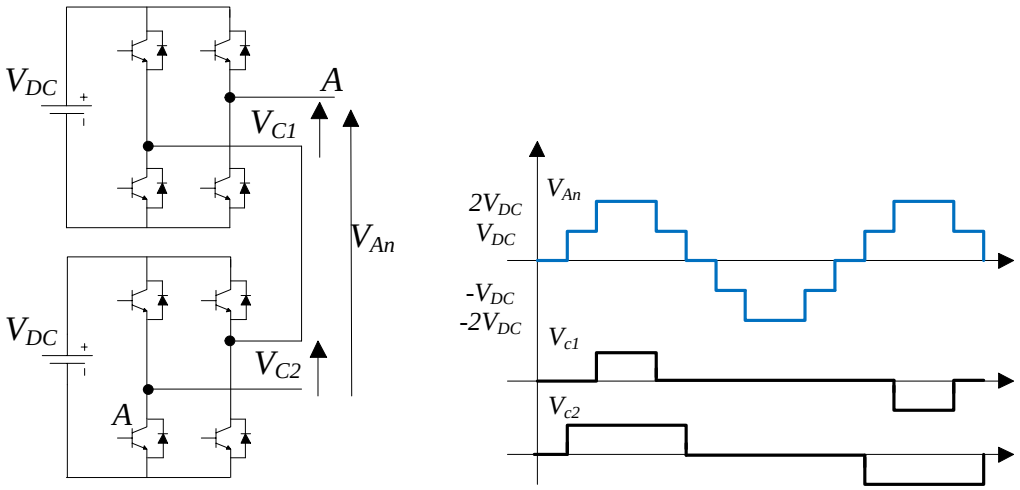

Fig. 1. 10 Cascaded 5L-CHB inverter

Table 1.3 Main features of MLIs

Topology	NPC	FC	CHB
Switching Devices	2(n-1)	2(n-1)	2(n-1)
Clamping diodes per phase	(n-1) (n-2)	0	0
DC.Bus Capacitors	(n-1)	(n-1)	Depends on type of supply
Balancing Capacitor per phase	0	(n-1)	-
Voltage unbalancing	Average	High	Very small
Applications	Motor drive systems STATCOM	Motor drive systems STATCOM	Motor drive system, PV, fuel cells, battery system

1.1.4 Recent advances in MLI topologies

Advanced multilevel converters have been proposed in literature [41]. Among them, the following have found practical application:

- five-level H-bridge NPC (5L-HNPC)
- three-level active NPC (3L-ANPC)
- five level active NPC (5L-ANPC)
- modular multilevel converter (MMC)
- cascaded matrix converter (CMC)
- transistor-clamped converter (TCC)
- CHB fed with unequal dc sources or asymmetric CHB

- cascaded NPC feeding open-end loads
- hybrid NPC-CHB and hybrid FCCHB topologies
- stacked FC or stacked multi-cell

These topologies are variations of the three classic topologies discussed in the previous section, as shown in Fig. 1. 2. Technical specifications are available in [11]-[25]. The 5L-HNPC converter is composed of the H-bridge connection of two classic 3L-NPC phase legs, as shown in Fig. 1. 11, forming a 5L-HNPC converter. This converter is found in practice with a 36-pulse rectifier system featuring IGCT devices, for the 2–7-MW (air cooled) or 5–22-MW (water cooled) power range. Several 5L-HNPC configurations have been developed with 24- or 36-pulse diode rectifier front ends, with medium-voltage IGBTs (MV-IGBTs), IEGTs, or GCTs, up to 7.8-kV output voltage, 120-Hz output frequency and 120 MVA output power [13]. Fig. 1. 12a shows a 3L-NPC inverter equipped with IGCTs, rating 20–200 MVA. One of the drawbacks of the 3L-NPC topology is the unequal share of losses between the inner and outer switching devices in each converter leg. Recently, a variation of the ANPC concept has been proposed, i.e., a five-level hybrid multilevel converter that combines a 3L-ANPC leg with a three-level FC power cell connected between the internal ANPC switching devices, as shown in Fig. 1. 12b. Although it is a hybrid topology, it has been called 5L-ANPC [48]–[50], [53]. Note that, instead of IGCTs, series-connected IGBTs are used in the NPC part of the converter, probably to keep all semiconductors of the same type. A commercial version of this topology has recently been introduced [11], [50], aimed to medium voltage, low-medium power applications. A variation of the hybrid 5L-ANPC has been proposed by adding a common cross converter (CCC) stage [55] to the 5L-ANPC, resulting in a nine-level hybrid converter [51], as shown in Fig. 1. 12c. Although this additional stage increases the number of levels, greatly improving the power quality, this comes at the expense of a quite complex structure and the need to balance both the CCC and FC capacitor voltages. Another multilevel converter that has recently found industrial applications, particularly for HVDC systems, is the MMC (also known as M2C) [56], [57]. Basically, the MMC is composed of series connected single-phase two-level voltage source converter (2L-VSC) legs, as illustrated in Fig. 1. 13(left). This topology found practical application on 200 power-cell/phase structures reaching 400 MW [55] and 1 GW [56]. The Transistor-Clamped Converter TCC concept is very similar to that of the DCC, however, bidirectional switches are used instead of diodes to clamp the connection points between switches and capacitors, Fig. 1. 13 (right). This gives a controllable path for the currents through the clamping devices, like the ANPC. This topology has been exploited [15], [58] in medium voltage (3.3, 6.6, and 9.9 kV) and high power (up to 48 MW) industrial applications. Power losses are shared among the devices,

enabling higher switching frequencies, thus increasing the maximum output frequency and making this converter suitable for variable high-speed drives, in railway traction applications.

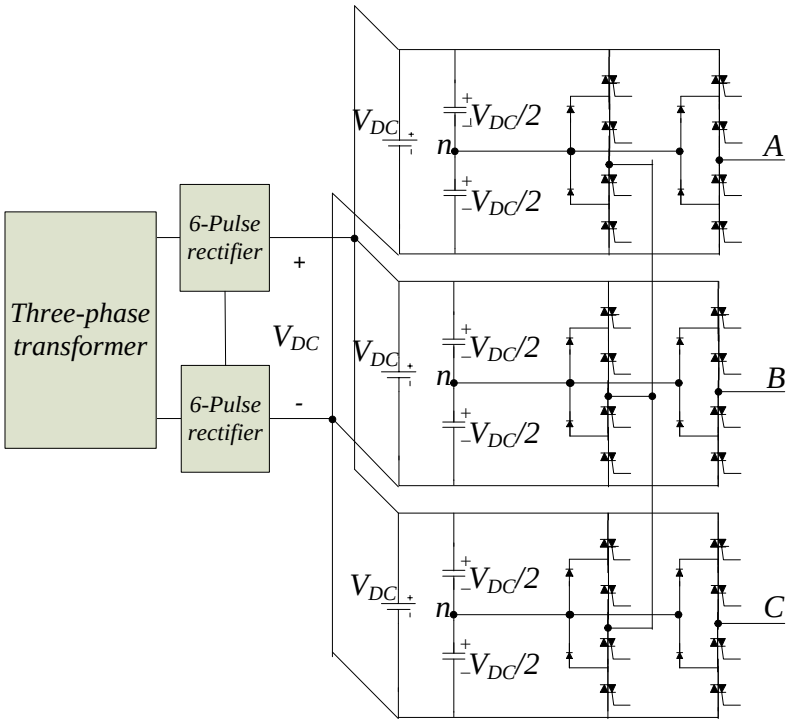

Fig. 1. 11 Three-phase 5L-HNPC inverter [43]-[45]

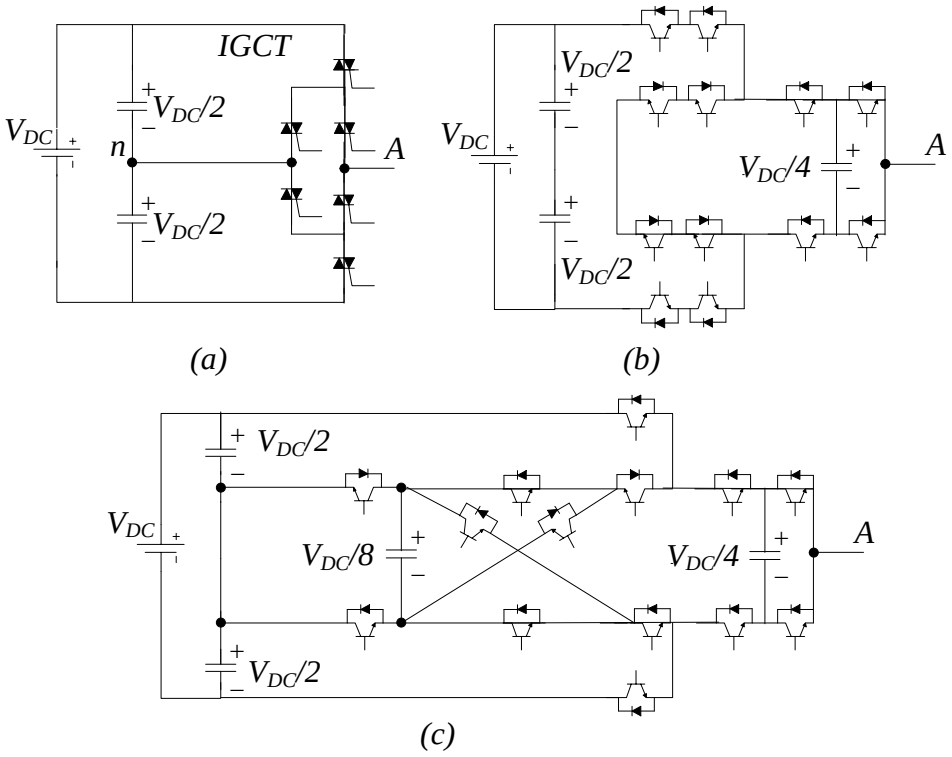

Fig. 1. 12 Active NPC. a) 3L-ANPC featuring IGCTs [46]-[47]. b) 5L-ANPC featuring IGBTs [48]-[50]. c) CCC stage plus 5L-ANPC hybrid nine-level inverter [51]

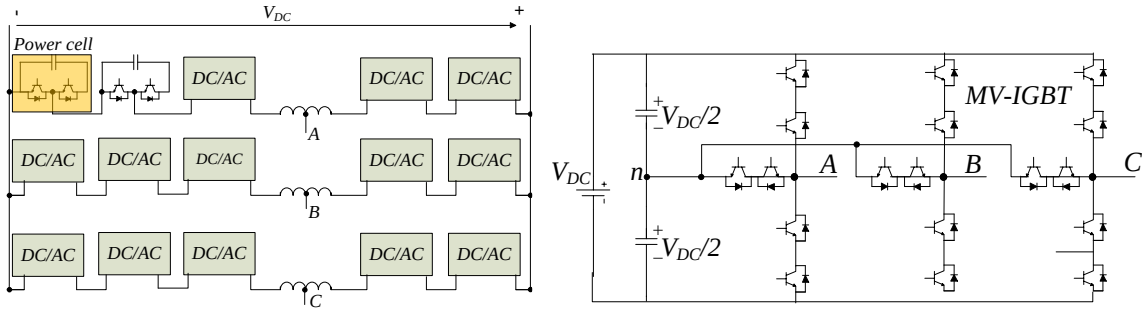

Fig. 1. 13 Modular Multilevel converter MMC (left), Three phase three-level TCC(right)

The combination of different multilevel converter topologies gives rise to hybrid multilevel converters. Two main hybrid multilevel converter are present in the literature, the NPC-CHB converter [59]-[65], depicted in Fig. 1. 14(left) and the Hybrid Multilevel Converters feeding Open-End Winding machine [66]-[81], Fig. 1. 14 (right).

The NPC-CHB, combines a 3L-NPC and single-phase H-bridge cells. On the H-bridge DC side a floating capacitor is present without a voltage supply. Hence, the addition of H-bridge stages only introduces more voltage levels but does not effectively increase the active power rating of the overall converter. The number of series connected H-bridge usually varies between one and two.

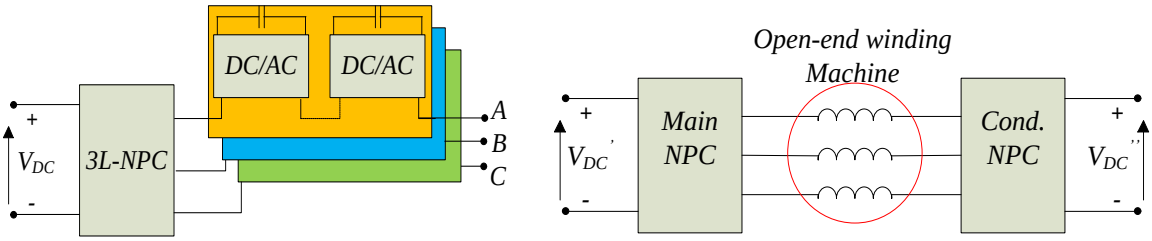

Fig. 1. 14 Multilevel NPC-CHB hybrid converter(left)[52]-[54], Cascaded NPC inverter connected in series through an open-end winding stator machine(right)

The concept of cascading two 3L-NPC converters, with one at each side of an open-end stator winding of an induction motor, was first introduced in [66]. Later, two separately excited two-level voltage source inverters (2L-VSIs) with different voltage ratios generating a four-level converter were introduced [69]. This concept evolved in a structure encompassing a MLI and a TLI. The first (the main inverter) supplies only active power to the load, while the second (the auxiliary inverter) acts as a series active filter [67]-[70]. In this way, high voltage power devices are adopted for the main inverter and low voltage fast power devices can be used on the auxiliary one.

1.1.5 Control and Modulation Strategy for MLIs

Modulation strategies for multilevel inverters can be divided into two main groups, namely: space vector and time domain, Fig. 1. 15. Furthermore, they can be classified according to switching frequency, as shown in Fig. 1. 16 [82], [83]. A very popular modulation strategy, largely used in industrial applications, is the classic carrier-based sinusoidal PWM (Sine-PWM) that uses the phase-shifting technique to reduce output voltage harmonics [17], [84], [85]. An interesting alternative is the Space Vector Modulation SVM strategy [82].

Strategies which work at low switching frequencies, generating a staircase output voltage waveform are the multilevel selective harmonic elimination [86], [87] and the space-vector control (SVC) [88]. Generally, a low-switching frequency features low switching losses while high-switching frequency features high switching losses.

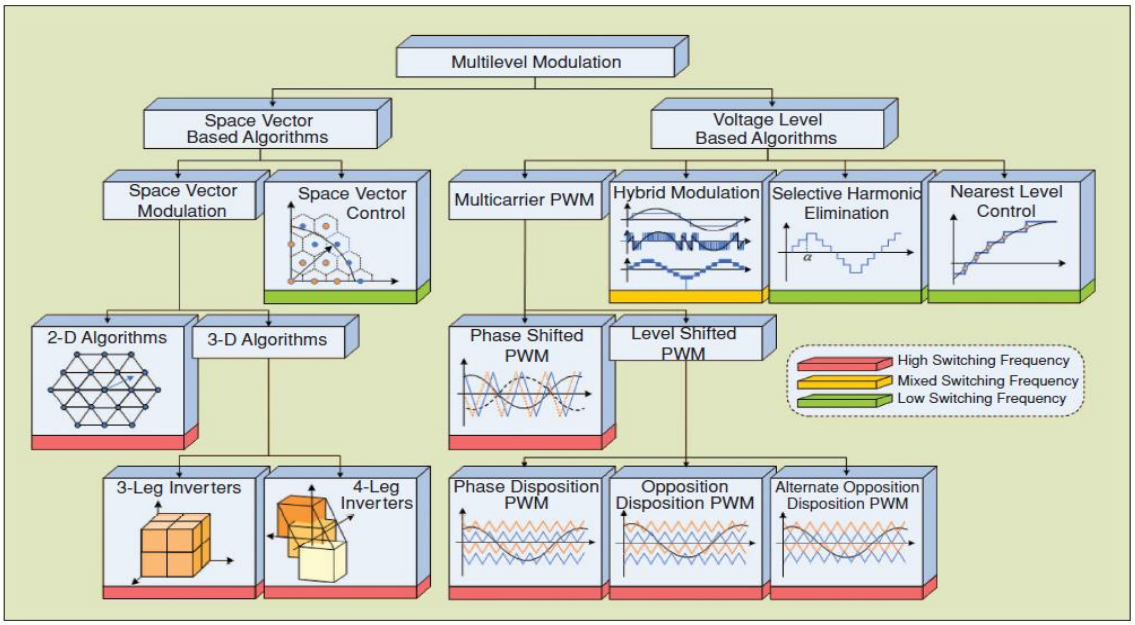

Fig. 1. 15 Classification of Multilevel modulation methods based on the domain in which they operate

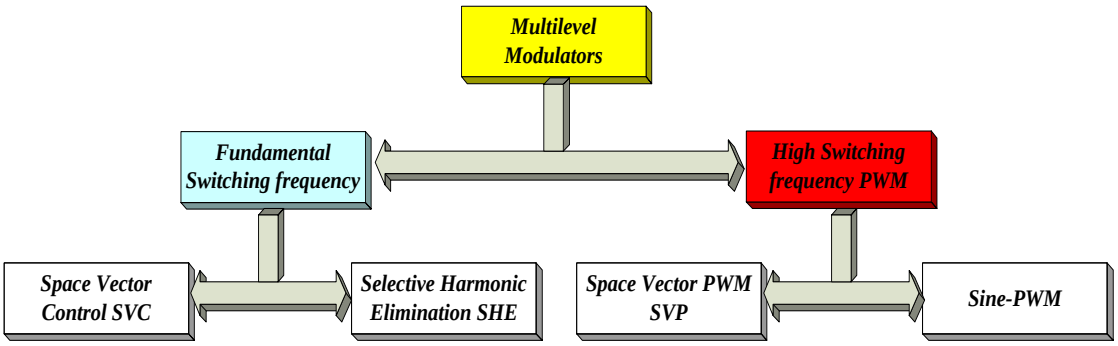

Fig. 1. 16 Classification of Multilevel modulation methods based on switching frequency

1.1.5.1 Sine-PWM Modulation

The most popular control technique for traditional inverters is the sinusoidal or "subharmonic" Pulse Width Modulation (SPWM). Its popularity is due to the easy implementation and the robustness [89]. When a single triangular carrier signal is used on a conventional three-phase two-level inverter, *n*-1 carriers will be needed on a *n*-level inverter in order to synthetize the pseudo-sinusoidal output voltage. In the last case, the carriers have the same frequency f_c, the same peak-to-peak amplitude A_c, and are deployed on contiguous bands. The phase displacement between two contiguous triangular carriers is free. Three configurations can be used, Fig. 1. 17:

- All the carriers are in opposition with the following one (APOD disposition, see Fig. 1. 17(left))
- All the carriers above the zero value reference are in phase among them, but in opposition with those located below the zero level (POD disposition, see Fig. 1. 17(middle))
- All the carriers are in phase among them (PH disposition, see Fig. 1. 17(right)).

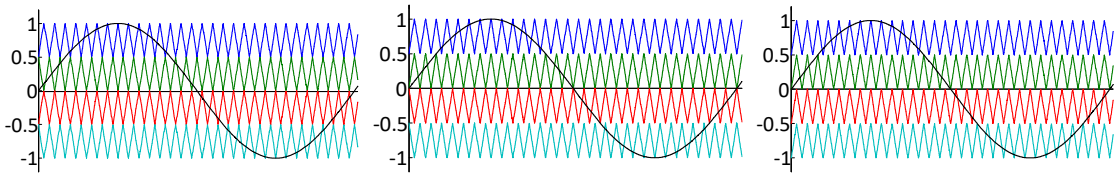

Fig. 1. 17 Carriers and reference waveforms for 5-level inverter. Left) APOD. Middle) POD. Right) PHD.

The amplitude modulation index m_a and the frequency ratio m_f are defined as:

$$m_a = \frac{A_m}{(n-1)\,A_c} \tag{1.1}$$

$$m_f = \frac{f_m}{f_c} \tag{1.2}$$

being A_m and f_m respectively the peak-to-peak amplitude of the fundamental voltage and the fundamental frequency. The harmonic content of the output voltage varies according to the selected configuration. In the APO and PO cases, the harmonics at the carrier frequency and multiples do not exist at all. For the PHD, no harmonics exist at even multiples of the carrier frequency. When the frequency ratio m_f is high, there are no substantial differences among the three configurations, because all the harmonics are moved to the high frequency range so they are easily filtered. The scenario changes when m_f is not sufficiently high. In this case the PH configuration seems the least interesting, due to large (greater than the fundamental) harmonic at f_c,

generated at low m_a values. However, dealing with three-phase inverters and using a single-phase modulation, that harmonic is of common mode nature, so it will not be present in the harmonic content of the phase current of a wye connected load. In this case the PH configuration becomes the most interesting one, due to the very little amplitude of the other harmonics. On a multilevel SPWM the apparent switching frequency of the output voltage is a multiple of the switching frequency of each cell. Such an advantageous feature allows a reduction of the effective switching frequency, thus reducing the switching losses.

1.1.5.2 Space Vector Modulation

According to the space vector modulation, the reference voltage *Vs* is synthetized by forcing the inverter to assume a suitable sequence of states (or voltage vectors) [90], [91]. Fig. 1. 18 shows the allowable states for a three-level inverter. A common characteristic to all SVM-based schemes is that the modulation algorithm is divided into three stages. In the first, a set of voltage vectors are selected, usually, the three closest to the reference voltage vector. On the second stage duty cycles are computed (or On and Off times) for each vector in order to achieve the desired reference voltage as average over a single switching time (the inverse of the switching frequency). In the final stage the vector sequence is generated.

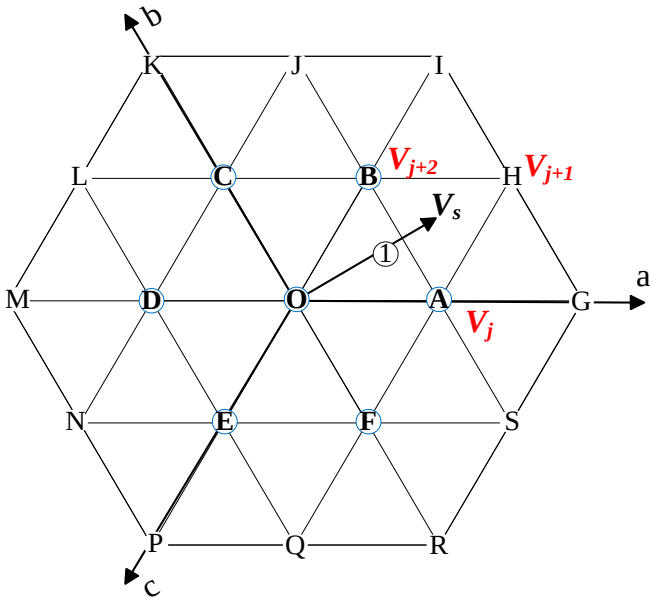

Fig. 1. 18 Space vector for a 3LI inverter.

The desired voltage vector can be synthesized by computing the duty cycles (T_j, T_{j+1} and T_{j+2}) of the three inverter voltage vectors.

$$V_s = \frac{T_j V_j + T_{j+1} V_{j+1}}{T} \tag{1.3}$$

SVPWM methods generally feature good utilization of DC-link voltage, low current ripple, and an easy hardware implementation by a digital signal processor (DSP). These features make it suitable for high voltage, high-power applications. As the number of levels increases, redundant switching states and the complexity of selection of switching states increase dramatically.

1.1.5.3 Selective Harmonic Elimination

The selective harmonic elimination is considered as a low-frequency modulation [86], [87]. Fig. 1. 19 shows a generalized quarter-wave symmetric stepped-voltage waveform synthesized by a *n*-level inverter, being *m* the number of switching angles. By applying the Fourier series analysis, the amplitude of any odd harmonic of the stepped waveform can be expressed as:

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{m} V_k \cos(n\theta_k) \tag{1.4}$$

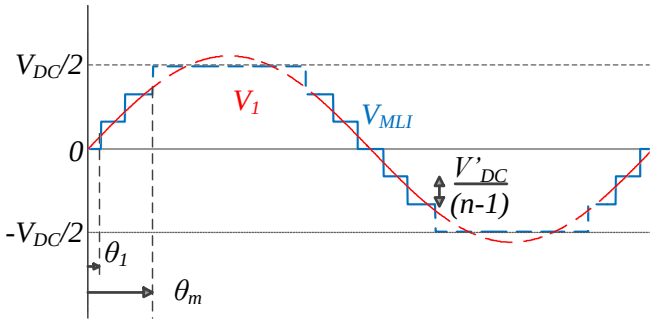

Fig. 1. 19 Generalized output stepped-voltage waveform for a n-level inverter

where V_k is the k^{th} level of DC voltage, n is the harmonic order and θ_k is the k^{th} switching angle. The amplitude of the staircase output phase voltage V_{MLI} is controlled by acting on $m=(n-1)/2$ switching angles $\theta_1,\theta_2,...,\theta_m$ $(0\leq\theta_1<\theta_2<\theta_m)/2\leq \pi/2)$. More specifically, switching angles are selected in order to obtain the required fundamental voltage reference V_1, while eliminating from the harmonic content of the output voltage, $n-1$ of the lowest odd, non-triple harmonics. Therefore, θ_1, θ_2,..., θ_m, are computed by solving the following set of (n-1)/2 non-linear transcendental equations:

$$\begin{aligned}
&\cos\theta_1 - \cos\theta_2 + ... + \cos\theta_{(n-1)/2} = m_a \\
&\cos 5\theta_1 - \cos 5\theta_2 + ... + \cos 5\theta_{(n-1)/2} = 0 \\
&.....\\
&\cos k\theta_1 - \cos k\theta_2 + ... + \cos k\theta_{(n-1)/2} = 0
\end{aligned} \tag{1.5}$$

where: k is the order of the highest harmonic that has to be eliminated and m_a is the modulation index defined as:

$$m_a = \frac{\pi}{4}\frac{V^*}{V_{DC}} \tag{1.6}$$

In general, the most significant low-frequency harmonics are selected for elimination, as high-frequency harmonic components can be readily removed by using additional filters.

1.1.5.4 Space Vector Control and Direct Torque Control

A conceptually different control method for multilevel inverters, based on the space-vector theory, is introduced in [83]. This control strategy, called Space Vector Control SVC, works with low switching frequencies. It is adopted for inverters with a large number of voltage levels, where voltage vectors are very close, as depicted in Fig. 1. 20.

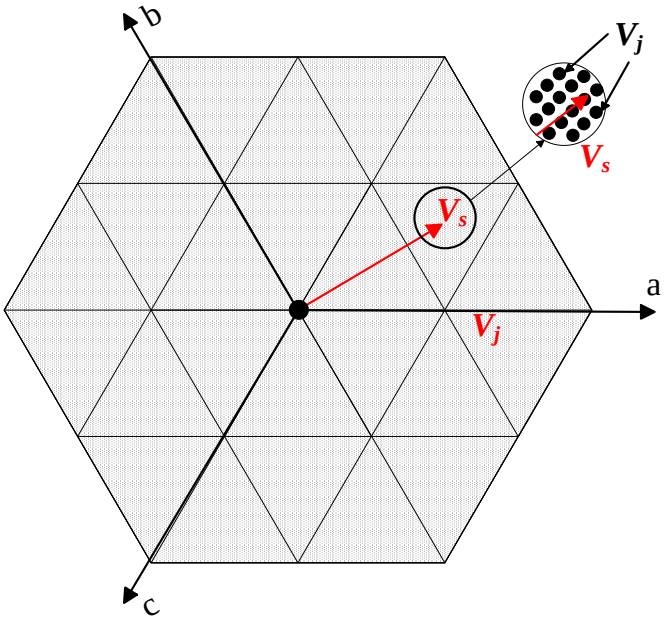

Fig. 1. 20 Space Vector locations for high number of level

The basic principle of SVC is to generate a voltage vector that minimizes the space error, or distance to the reference vector V_s. The high density of vectors produced by the *n*-level inverter (n>11) will generate only small space errors, a traditional PWM modulation strategy it is, therefore, unnecessary. The hexagon of Fig. 1. 20 shows the boundary of highest proximity, which allows to select the inverter voltage vector that is closest to the reference voltage vector. As the amount of inverter voltage levels drops, the SVC method becomes ineffective, as the space error raises, thus increasing the load current ripple. Finally, the DTC technique has been developed for low-voltage two-level inverters as an alternative to the field oriented method to effectively control torque and flux in ac drives [92]. DTC and hysteresis current control techniques have also been applied in multilevel inverters [93]. At least one major manufacturer has been selling medium-voltage three-level diode clamped inverters controlled with DTC [94].

1.1.5.5 Capacitor Balancing Techniques for MLIs

A typical issue of a MLI is the fluctuation of the neutral point of the DC-Bus, causing the distortion of the output voltage. This phenomenon is clearly discussed in [95]. The paper demonstrated that a diode-clamped multilevel inverter delivering only real power to the load cannot establish balanced voltages without admitting output voltage distortion. On the contrary, a voltage balancing method is not needed if a suitable reactive power is delivered to the load. Many techniques can be adopted in order to solve the problem of the fluctuation of the neutral point. In [96] the problem is solved by using a back to-back rectifier/inverter system and proper voltage balancing control. Other papers [97]–[99] suggested the use of additional voltage balancing circuits, such DC chopper, etc. The capacitor-clamped structure was originally proposed for high-voltage DC/DC conversions [100]. It is easy to balance the capacitor voltages in these applications because the load current is DC. Voltage balancing in a capacitor-clamped multilevel inverter, is a quite complex task [60], [101]. It has been shown theoretically that the capacitor-clamped inverter cannot self-balance the capacitor voltage when no real power is delivered to the load, such as in reactive power compensation. Moreover, voltage balancing become troublesome because each phase leg has its own floating capacitor. The cascaded multilevel inverter was first introduced for motor drive applications, exploiting an isolated and independent DC voltage source for each H-bridge [17]. However, a paper presented the idea of using cascade multilevel inverter for reactive and harmonic compensation, omitting isolated DC sources [96]. Additional works further demonstrated that the cascaded multilevel inverter is suitable for universal power conditioning in medium-voltage power systems [102], [103]. Such a configuration, in fact, provides lower costs, higher performance, less electromagnetic interference

(EMI), and higher efficiency than the traditional PWM inverter for power line conditioning applications. Although the cascaded inverter has an inherent self-balancing characteristic, because of power losses and limited controller resolution, a slight voltage imbalance can occur. A simple control scheme, which ensures a DC voltage balance, has been proposed for reactive and harmonic compensation [96]. Fig. 1. 21 shows its control block diagram. It contains a proportional–integral (PI) regulator to adjust the trigger angle and to ensure zero steady state error between the reference DC voltage and the DC-bus voltage. Multilevel rectifiers have been also proposed to eliminate phase shift transformers. For those applications not requiring regenerative capabilities, simplified (or reduced) multilevel rectifiers have been proposed in [104]. This specific rectifier, named the Vienna rectifier, has been used for telecommunication power supplies. Fig. 1. 22 shows the per-phase leg structure for a three-level Vienna rectifier.

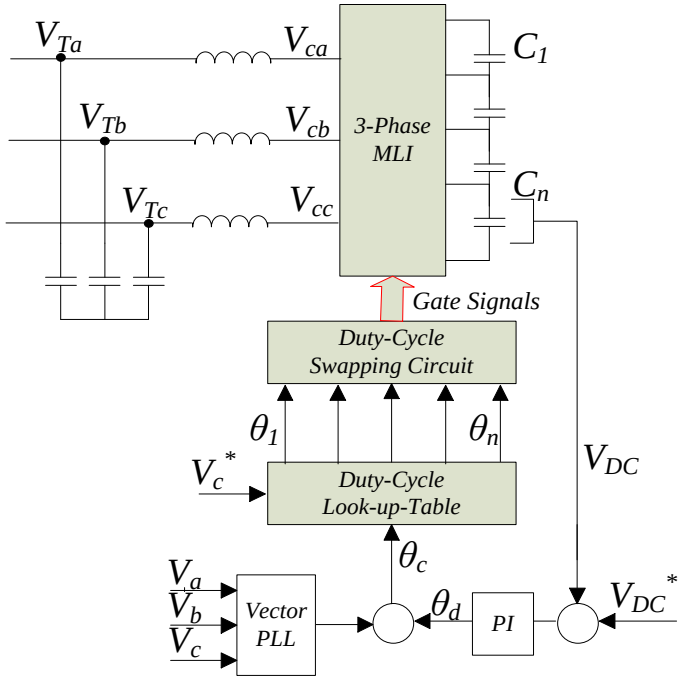

Fig. 1. 21 Control diagram for DC-Bus voltage control in a MLI

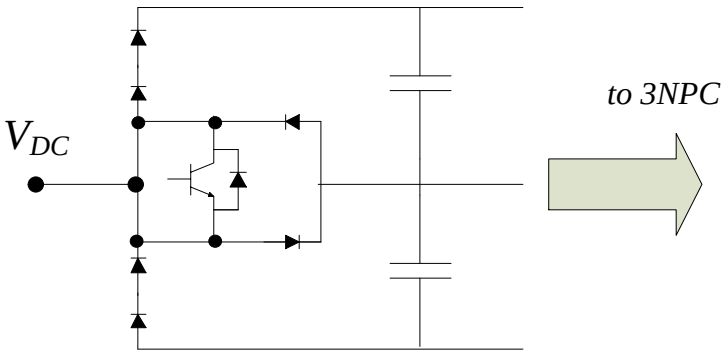

Fig. 1. 22 Vienna rectifier phase leg structure

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2 Chapter: Open-end Winding Systems

As discussed in chapter 1, alternative multilevel converter topologies have been proposed in the last two decades. Among them, a multilevel inverter structure obtained by feeding an open-end winding machine through two two-level inverters has gained a large interest. In this chapter, a review of Open-end Winding Systems (OWS) is given. In particular, benefits in terms of output voltage waveform, DC-Bus utilization and efficiency are highlighted. The chapter ends with a discussion of common-mode voltage and zero-sequence current issues.

2.1 Definition and features of an Open-end Winding System

Reliability and availability have become increasingly a priority for electrical drives in application fields as railway, ship propulsion, electrical vehicles etc. These systems are primarily based on induction machines powered by conventional 2-Level Inverters (TLI), although this association has some disadvantages. Specifically, several research efforts have been oriented to overcome limitations of conventional (TLI) in handling high voltages, high *dv/dt* levels, high switching frequency and Total Harmonic Distortion (THD) issues. Some of these solutions rely in the modification of the electric machine by adopting multi-phase (more than three) or multi-star windings. While, on the side of the power converter, new topologies and new modulation techniques have been developed. Among them, Multi-Level inverters are able to reduce the *dv/dt* stress on power devices as well as to improve the voltage and current harmonic content. In fact, a MLI, by increasing allowable output voltage levels, generates a lower load current THD for a given switching frequency, thus improving the efficiency. Main MLI topologies have been discussed earlier with their features. However, a special MLI can be obtained exploiting an Open-end Winding System (OWS) [1]-[30]. Basically, the term OWS derives from how the windings of an electrical machine (motor or transformer) are connected to the power supply. Two standard configurations are known: the wye-connected AC machine, where the neutral point of the windings is accessible and the delta-connected machine, as depicted in Fig. 2. 1. The basic OWS configuration is obtained by splitting the neutral connection of an AC machine and connecting each end-phase of the winding to an independent TLI, Fig. 2. 2.

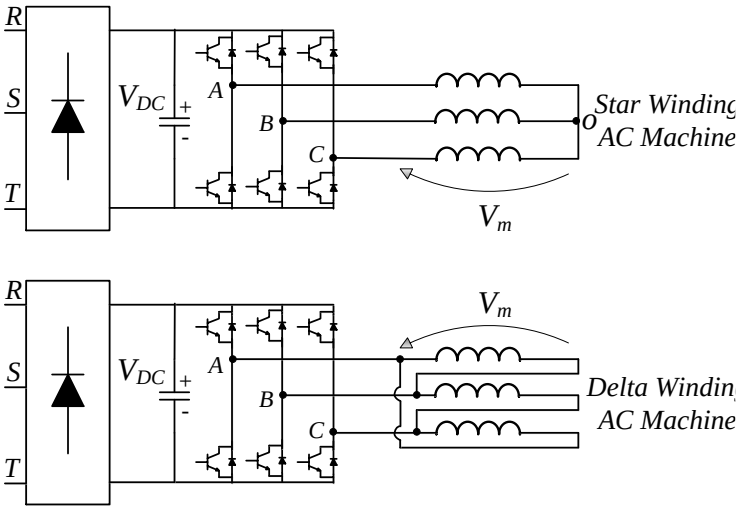


Fig. 2. 1 Standard configurations: wye-connected with neutral point 'o' and delta connected AC machine

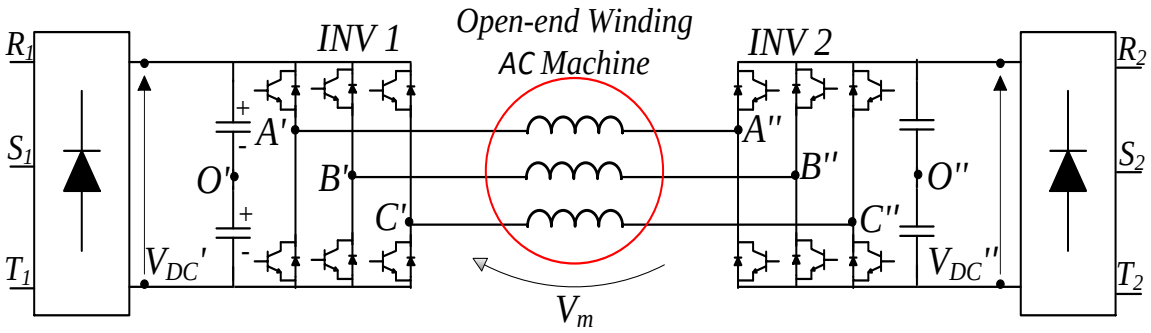


Fig. 2. 2 Standard scheme of an Open-end Winding System

A combination of two TLIs with three phase open-end winding AC machine results in 64 switching state vectors rather than 8, as for a conventional two-level three phase inverter, as depicted in Fig. 2. 3 [4]. For a given load current THD, such a large number of switching state vectors allows to reduce the inverter switching frequency [1], [5]-[7], [9], [11], [16], [18], [19]. In Fig. 2. 2, $V_{A'O'}$, $V_{B'O'}$, $V_{C'O'}$ are the pole voltages of inverter 1, while, $V_{A''O''}$, $V_{B''O''}$, $V_{C''O''}$ are the pole voltages of inverter 2. Allowable space vectors for each inverter are shown in Fig. 2. 3 (up), while the space phasors of the OWS system are shown in Fig. 2. 3 (down). Voltage vectors combinations are also summarized in Table 2.1, where a '1' means top switch in the inverter is 'on', a '0' means bottom switch in the inverter is 'on'. In all 64 space phasor combinations are possible exploiting both the inverters. For example, a combination 6'-1'' implies that the switching state for INV 1 is (101) and that for INV 2 is (100). The motor phase voltage can be computed from pole voltages of the two inverters. The 64 voltage space phasors define the vertices of 24 equilateral triangles, or sectors, Fig. 2. 3 (down). Six adjacent sectors form a hexagon. Thus, six hexagons can be identified, with their centers at A, B, C, D, E and F respectively. The externals vertices are identified as G, H, I, J, K, L, M, N, P, Q, R, S. The center of the composition of the six hexagons is located in O. The length of the vectors **OA** and **AG** is equal to V_{DC}' and

V_{DC}'' respectively, while the length of the vector **OG** is V_{DC}'+V_{DC}''. Assuming $\mathbf{V_s}$ as the reference voltage vector:

$$V_S = V_A^* + aV_B^* + a^2 V_C^* \tag{2.1}$$

where V_A^*, V_B^* and V_C^* are the reference voltages and:

$$\begin{aligned} a &= a^{j2/3\pi} \\ a^2 &= a^{j4/3\pi} \end{aligned} \tag{2.2}$$

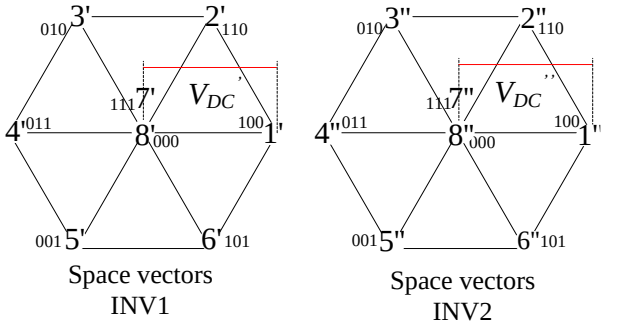
If $\boldsymbol{V_s}$' is the output voltage vector of the inverter 1 and $\boldsymbol{V_s}$'' is the output voltage vector of the inverter 2:

$$V_S' = V_{A'O'} + V_{B'O'} e^{j2/3\pi} + V_{C'O'} e^{j4/3\pi} \tag{2.3}$$

$$V_S'' = V_{A''O''} + V_{B''O''} e^{j2/3\pi} + V_{C''O''} e^{j4/3\pi} \tag{2.4}$$

the combined output voltage synthetized by the dual inverter system is obtained as:

$$V_S = V_S' + V_S'' = V_{A'A''} + V_{B'B''} e^{j2/3\pi} + V_{C'C''} e^{j4/3\pi} \tag{2.5}$$



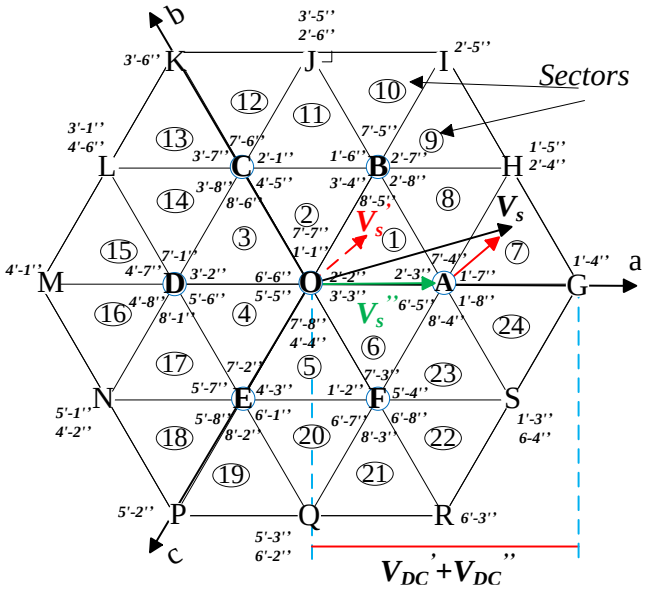


Fig. 2. 3 Space vectors OWS.

The dual two-level inverter-fed open-end winding machine system features some advantages such as redundancy of space-vector combinations and the absence of neutral point fluctuations [19]. This configuration provides also a mean to optimally exploit different types of semiconductor switches [3], [19] and [24].

Many PWM control strategies have been developed in order to synthetize the reference voltage V_s, by computing the right vectors $V_s^{'}$ and $V_s^{''}$. In particular, the phase-shifted carrier-based PWM, that is used for multilevel output voltage generation in [8]. Moreover, conventional voltage space-vector modulation strategies have been applied to cascaded converter configurations, consisting of two standard two-level voltage source inverters [19], [23], [24], [25]. Classical space-vector PWM, based on the asynchronous principle are burdened by generation of sub-harmonics of the output voltage fundamental component, that are very undesirable in medium/high power applications [26]-[27].

A method based on the principle of the synchronized modulation has been developed to control a dual inverter-fed open-end winding motor drives with a single DC voltage source [28] and with two separate DC sources (without power balancing between sources) [29]. A continuous control of the power sharing between two separate DC sources has been also proposed [11]. A new Space-Vector Pulse Width Modulation (SVPWM) scheme for an induction motor with open-end windings has been presented in [5]. Such a scheme requires two isolated power supplies and uses instantaneous phase reference voltages. The proposed PWM scheme employs two inverters which alternate their clamping and switching duties along each cycle. An improved PWM switching scheme is proposed in [6] aimed to reduce the number of switchings in a dual inverter system. A relevant 50% reduction is achieved. In [9] pulse width modulation for the two inverters is implemented through a simple but effective time placement, thus, eliminating the need of sector identification procedures and lookup tables. In order to avoid synchronism of conventional space-vector modulation, a synchronized PWM strategy has been used to control each inverter in a dual inverter-fed traction drive [22], [23]. In [30] a dual two-level inverter is exploited to extend the field weakening speed range of Surface Permanent Motor (SPM). The proposed method can increase the maximum speed of a SPM motor up to about 4 times the base speed without using a demagnetizing current.

Main features of dual two-level systems (D2LS) are:

- The load real power demand is equally shared between the two inverters;
- Each converter is rated at half of the load power;
- Independent control of the three stator currents;
- The apparent switching frequency is twice that of the two inverters;

• Readily extendible to systems with a greater number of phases;

• Machine losses are the same (or somewhat less) than in a conventional system with a wye connection;

• A 70% higher voltage is available across each phase winding for a given inverter voltage rating, resulting in an extended speed range.

Table. 2.1. Space Vector combinations.

States	Vector INV 1	Vector INV 2
000	8’	8’’
111	7’	7’’
100	1’	1’’
110	2’	2’’
010	3’	3’’
011	4’	4’’
001	5’	5’’
101	6’	6’’

A noticeable improvement of the voltage and current harmonic content is obtained by adopting an open-end winding configuration since the amount of output voltage levels is increased. Three dual-two level inverter topologies can be considered, namely: D2LS with symmetrical Isolated DC power supply (Fig. 2. 4), D2LS with symmetrical Single DC power supply (Fig. 2. 5) and D2LS with asymmetrical isolated DC power supply (Fig. 2. 6). If $V_{DC}^{'}=V_{DC}^{''}$ a symmetrical dual-two level inverter is obtained making 18 space vector voltage states available, as depicted in Fig. 2. 3. If $V_{DC}^{'}\neq V_{DC}^{''}$ an asymmetrical dual-two level inverter is obtained and 37 space vector voltage states are available, Fig. 2. 7. It will be shown in the following that the dual-two level inverter with an asymmetrical DC-Links works as a four-level inverter and a dual-two level inverter with symmetrical DC-Links works as a three-level inverter [3].

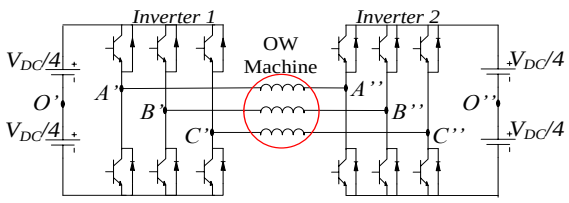


Fig. 2. 4. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with Symmetric Isolated DC-Links

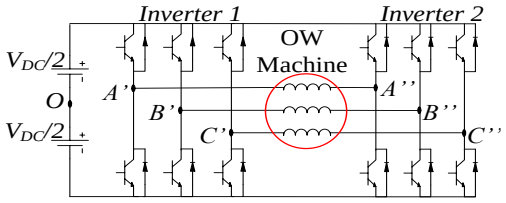


Fig. 2. 5. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with a single DC-Link

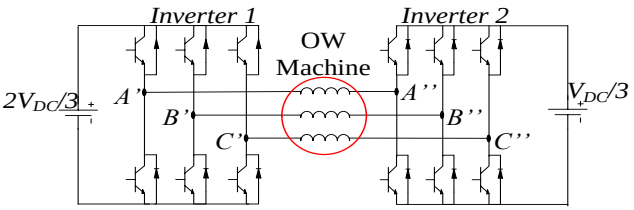


Fig. 2. 6. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with asymmetrical isolated DC-Links

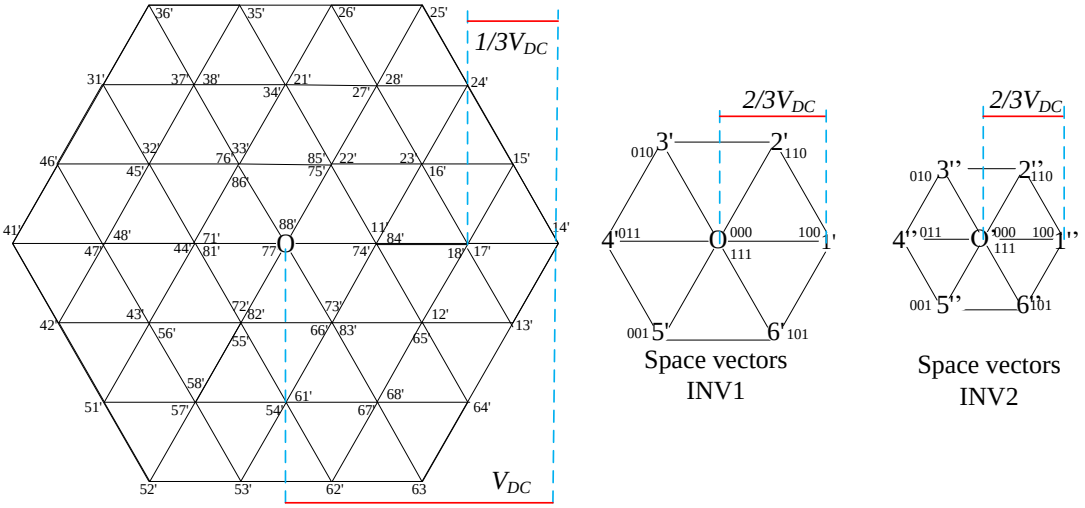


Fig. 2. 7 Space vectors for a Dual-Two-Level Inverter with asymmetric isolated DC-Links

2.1.1 Symmetrical Dual Two-level Inverter with single DC-Bus

A symmetrical dual-two level inverter is composed of two two-level three phase inverters of the same type and size [8], [12]-[14], [24]. These inverters are rated at 0.5 pu power with a DC Bus voltage $V_{DC}'=V_{DC}''=V_{DC}/2$, being V_{DC} the DC Bus voltage of an equivalent conventional three-phase configuration (with the machine windings wye or triangle connected). The DC power supply is common to the two inverters, resulting in a single DC-Bus voltage, Fig. 2. 8.

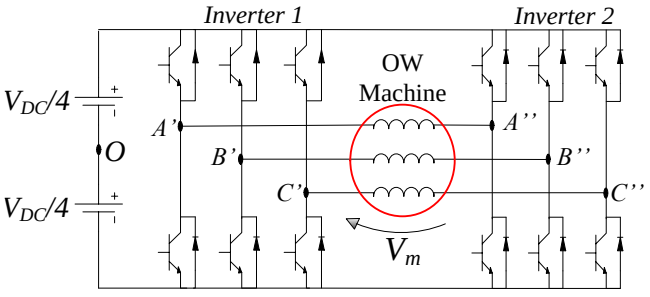


Fig. 2. 8. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with Symmetric and Single DC-Link

The inverter-1 *a'* leg output voltage, referred to the mid-point O of the DC-Bus is given by:

$$V_{A'O} = \frac{2l'-1}{4} V_{DC} \qquad l' = 0,1 \tag{2.6}$$

It may assume two non-zero voltage levels, namely; $+V_{DC}/4$ and $-V_{DC}/4$. The same applies for inverter-2:

$$V_{A''O} = \frac{2l''-1}{4} V_{DC} \qquad l'' = 0,1 \tag{2.7}$$

The voltage V_m applied to *a*-phase winding of the OW machine is given by:

$$\begin{aligned} V_m &= V_{A'O} - V_{A''O} = \left(\frac{2l'-1}{2} - \frac{2l''-1}{2} \right) V_{DC} \\ l' &= 0,1 \\ l'' &= 0,1 \end{aligned} \tag{2.8}$$

Thus, the phase voltage V_m may assume the zero voltage level and two non-zero voltage levels, namely; 0, $+V_{DC}/2$ and $-V_{DC}/2$. Hence, the symmetrical dual two-level inverter works as a three-level inverter. Usually, the output voltage of the inverter-2 is shifted by 180° from the output voltage of the inverter-1, Fig. 2. 9. As an example, the maximum phase voltage at the machine winding V_m^* is achieved by activating the state 1'(100) on inverter-1 and the state 4''(011) on inverter-2.

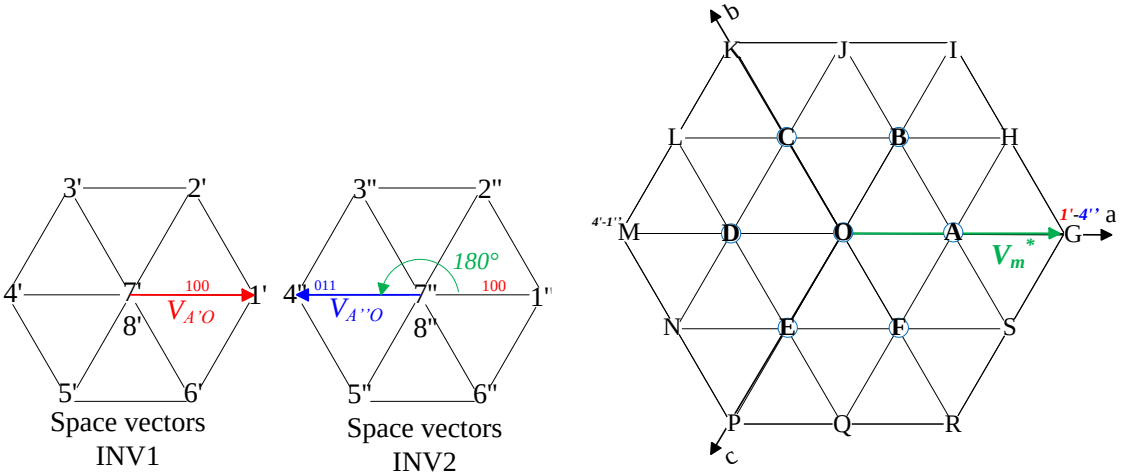


Fig. 2. 9 180° phase shifted PWM

Fig. 2. 10 shows the output phase voltage referred to the mid-point O of a conventional two-level inverter with V_{DC}=600 V, fundamental frequency f_1=50Hz and switching frequency f_{sw}=1kHz. Fig. 2. 11 depicts the phase voltage V_m for a symmetrical open-end winding system with single V_{DC}=600 V, fundamental frequency f_1=50Hz and switching frequency f_{sw}=1kHz. Further, Fig. 2. 12 and Fig. 2. 13 respectively show the harmonic spectra produced by a conventional two-level inverter and a symmetrical dual two-level inverter with single DC-Bus. Thanks to the three voltage levels modulation, the dual two-level inverter features an improved THD and a

doubled switching frequency if compared to the conventional system. Therefore, in order to obtain the same total switching frequency, each inverter of the dual-inverter system must be operated at half the switching frequency of the single inverter of the conventional system, resulting in lower voltage stresses, lower *dv/dt* and lower switching losses.

The main advantage of the symmetrical dual two-level inverter is that only a single power supply is required. However, zero-sequence currents may flow through the common DC-Bus voltage structure. In order to avoid the circulation of zero sequence currents in [32] the voltage reference is synthetized by using only the voltage space phasors H, J, L, N, Q, S, although at the cost of a reduction of the available maximum phase voltage.

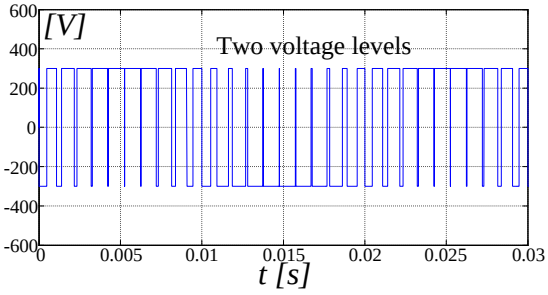


Fig. 2. 10. Phase voltage V_m with single three-phase inverter, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

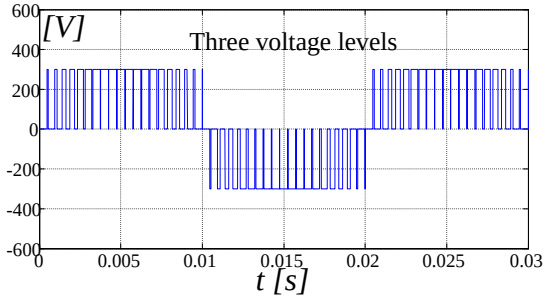


Fig. 2. 11. Phase voltage V_m with symmetrical dual two-level three-phase inverter, V_{DC}= V_{DC}/2=300 V, m=1, f_{sw}=1kHz, f1=50Hz

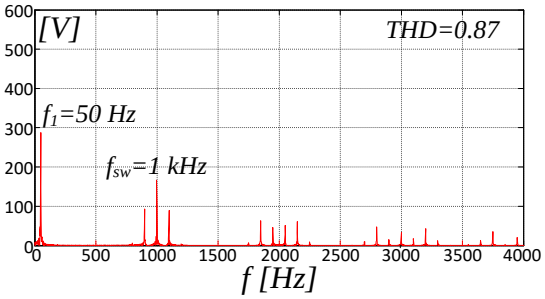


Fig. 2. 12. Harmonic spectrum of V_m with single three-phase inverter, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

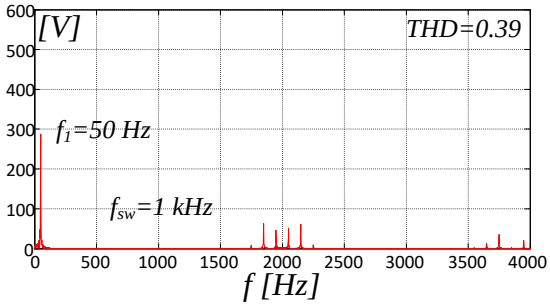


Fig. 2. 13. Harmonic spectrum of V_m with symmetrical dual two-level three-phase inverter, V_{DC}= V_{DC}/2=300 V, m=1, f_{sw}=1kHz, f1=50Hz

2.1.2 Symmetrical Dual Two-Level Inverter with two isolated DC-Buses

As shown in Fig. 2. 14, this configuration encompasses two independent DC-Buses, which are isolated between them by mean of two transformers [1], [3], [5], [6], [8]-[13], [16]-[21], [24]. DC Bus isolation prevents

the circulation of third harmonic currents. As in the symmetrical dual two-level inverter with single power supply: $V_{DC}'=V_{DC}''=V_{DC}/2$.

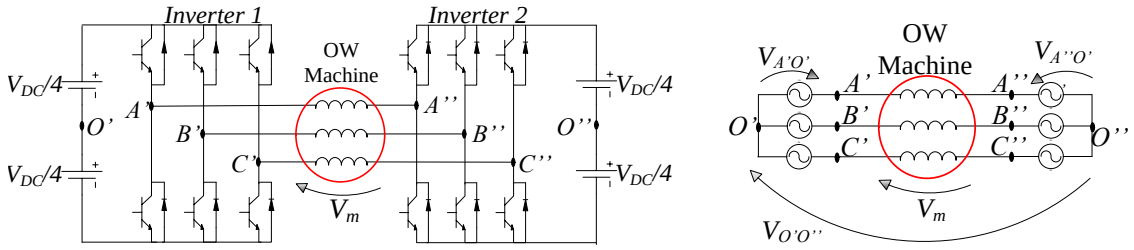


Fig. 2. 14. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with Symmetric and Isolated DC-Links(left). Electrical equivalent circuit(right)

According to Fig. 2. 14, the inverter-1 *a'* leg output voltage, referred to the mid-point O' of the DC-Bus of the inverter-1 is given by:

$$V_{A'O'}=\frac{2l'-1}{4}V_{DC} \qquad l'=0,1 \tag{2.9}$$

This voltage assumes two non-zero voltage levels, namely; $+V_{DC}/4$ and $-V_{DC}/4$. The inverter-2 a'' leg output voltage, referred to the mid-point O'' of the DC-Bus of the inverter-2 is given by:

$$V_{A''O''}=\frac{2l''-1}{4}V_{DC} \qquad l''=0,1 \tag{2.10}$$

Thus, the voltage V_m applied to a phase winding of the OW machine is given by:

$$\begin{aligned} &V_m = V_{A'O'}-V_{A''O''}+V_{O'O''}=\left(\frac{2l'-1}{4}-\frac{2l''-1}{4}\right)V_{DC}+V_{O'O''} \\ &l'=0,1 \\ &l''=0, \end{aligned} \tag{2.11}$$

being $V_{O'O''}$ the voltage between the mid-points O' and O'' of the DC-Buses of the two inverters. It is constant if the two DC-Buses are electrically connected, as for single power supply configuration, or variable if the two DC-Buses are isolated. In this case, $V_{O'O''}$ is given by:

$$V_{O'O''}=\frac{1}{3}\left(V_{A'O'}+V_{B'O'}+V_{C'O'}\right)-\frac{1}{3}\left(V_{A''O''}+V_{B''O''}+V_{C''O''}\right)=V_{CMV1}-V_{CMV2} \tag{2.12}$$

where V_{CMV1} and V_{CMV2} are the common-mode voltages of the inverter-1 and inverter-2, respectively. This quantity is known as differential-mode voltage for an open-end winding system and depends on the switching states of the two inverters [32]. Based on switching state combinations, the differential-mode voltage can assume up to three voltage levels, 0, $+V_{DC}/6$ and $-V_{DC}/6$. The voltage $V_{O'O''}$ must not be confused with common-mode voltage V_{CMV}, which is given by the sum of the common-mode voltages of the two inverters:

$$V_{CMV} = V_{CMV1} + V_{CMV2} = \frac{1}{3}\left(V_{A'O'} + V_{B'O'} + V_{C'O'}\right) + \frac{1}{3}\left(V_{A''O''} + V_{B''O''} + V_{C''O''}\right) \quad (2.13)$$

The common-mode voltage is responsible of the circulation of common-mode and bearing currents in AC motor drives. Table 2.2 summarizes the output voltage levels obtainable with a symmetrical dual-two level inverter with isolated DC-Buses. Fig. 2. 15 shows the phase voltage V_m of a symmetrical open-end winding system with V_{DC}=600 V, f_1=50Hz and f_{sw}=1kHz. Fig. 2. 16 shows the differential mode voltage $V_{O'O''}$ which assumes three voltage levels. Fig. 2. 17 and Fig. 2. 18 show the harmonic spectra of the phase voltage V_m and differential voltage $V_{O'O''}$, respectively. The phase voltage V_m assumes the zero and 8 non-zero levels, resulting in a reduction of the THD from 0.39 to 0.26, if compared with a dual two-level inverter with single DC-Bus. The differential-mode voltage $V_{O'O''}$ encompasses a zero-sequence component, which would cause a zero sequence current on a single DC-Bus system.

Table. 2.2. Space Vector combinations from Symmetrical dual two-level inverter with isolated DC-Buses

$V_{A'O'}$	$V_{A''O''}$	$V_{A'O}$- $V_{A''O''}$	$V_{O'O''}$	V_m=$V_{A'O}$- $V_{A''O''}$+ $V_{O'O''}$
2-levels 1/4V_{DC}, -1/4V_{DC}	2-levels 1/4V_{DC}, -1/4V_{DC}	3-levels 1/2V_{DC}, 0 -1/2V_{DC}	3-levels 1/6V_{DC}, 0 -1/6V_{DC}	9-levels 1/6V_{DC}, -1/6V_{DC},1/3V_{DC},0, 2/3V_{DC},1/2V_{DC},-1/12V_{DC}, -5/12V_{DC},-1/4V_{DC}

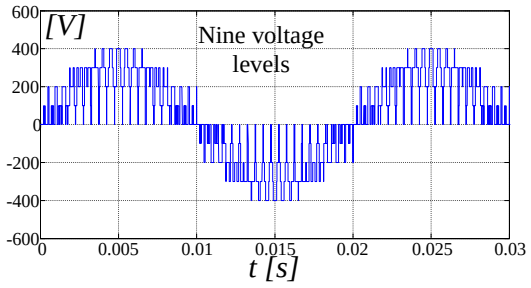


Fig. 2. 15. Phase voltage V_m with two isolated three-phase inverters, V_{DC}=600 V, m=1, f_{sw}=1kHz, f_1=50Hz

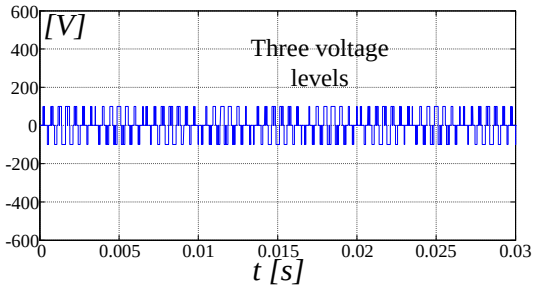


Fig. 2. 16. Voltage $V_{O'O''}$, V_{DC}=600 V, m=1, f_{sw}=1kHz, f_1=50Hz

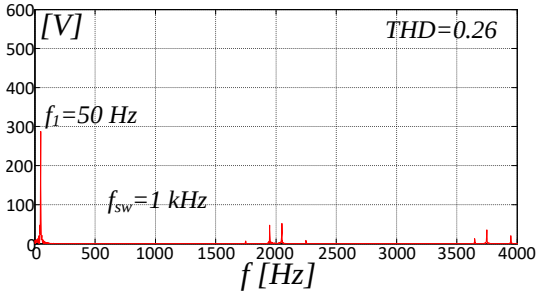


Fig. 2. 17. Harmonic spectrum of V_m with isolated three-phase inverters, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

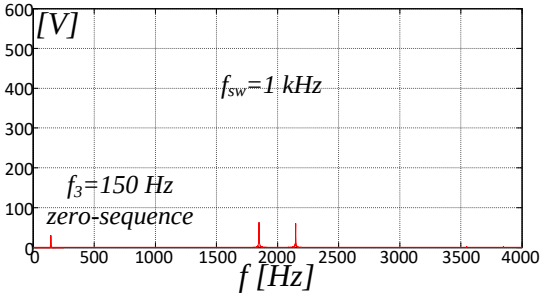


Fig. 2. 18. Harmonic spectrum of $V_{O'O''}$ with isolated three-phase inverters, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

The symmetrical dual two-level inverter is disadvantaged by the need of two isolated power supplies. However, a floating capacitor, Fig. 2. 19, can be used to replace the DC-Bus of one inverter, also preventing the circulation of zero-sequence currents. A suitable floating capacitor voltage control is required, as those proposed in [1] and [33]. The inverter with the floating DC-link capacitor is tasked either to provide reactive power to the system, either to boost the voltage at motor terminals.

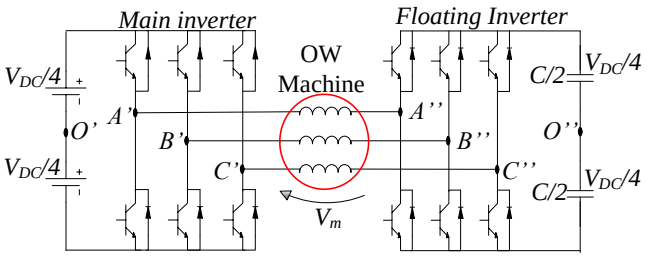


Fig. 2. 19. Dual-Two-Level Inverter circuit feeding Open-End Winding Machine with floating capacitor

2.1.3 Asymmetrical Dual Two-level Inverter with two isolated DC-Buses

A combination of two two-level inverters with $2/3V_{DC}$ and $1/3V_{DC}$ DC-Link voltage gives 64 voltage space phasor combinations in 37 space phasor locations rather than 18 as for a symmetrical dual two-level inverters, as depicted in Fig. 2. 7. According to eqs. (9) - (13), the phase voltage V_m assumes a different waveform compared with a single power supply. It assumes 13 non-zero voltage levels and one zero level, as shown in Fig. 2. 20. The increment of the amount of non-zero voltage levels is due to the larger number of levels of the differential-mode voltage $V_{O'O''}$, Fig. 2. 21. All voltage levels are calculated and summarized in Table 2.3. A reduction of the THD from 0.26 to 0.23 is obtained, as shown in Fig. 2. 22. Differently from what happens on a symmetrical dual two-level inverter, the differential-mode voltage $V_{O'O''}$ shows an harmonic component at the switching frequency, Fig. 2. 23.

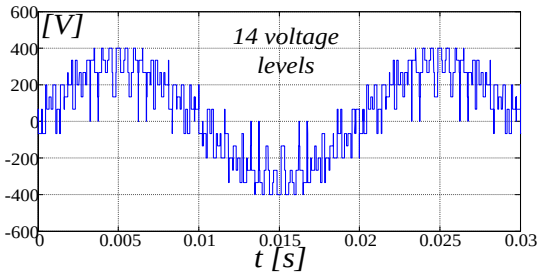


Fig. 2. 20. Phase voltage V_m with two isolated and asymmetrical three-phase inverters, V_{DC}=600 V, m=1,

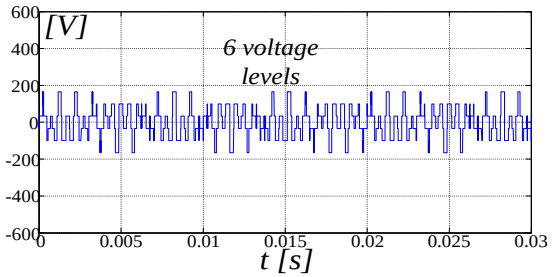


Fig. 2. 21. Voltage $V_{O'O''}$ with two isolated and asymmetrical three-phase inverters, V_{DC}=600 V, m=1,

f_{sw}=1kHz, f_1=50Hz

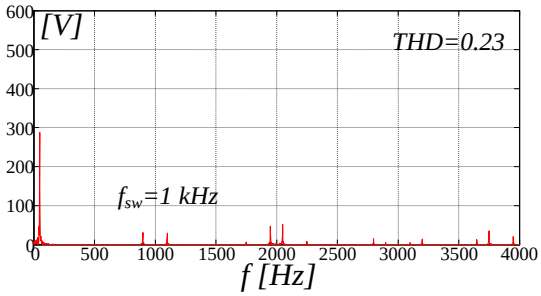


Fig. 2. 22. Harmonic spectrum of V_m with two isolated and asymmetrical three-phase inverters, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

f_{sw}=1kHz, f_1=50Hz

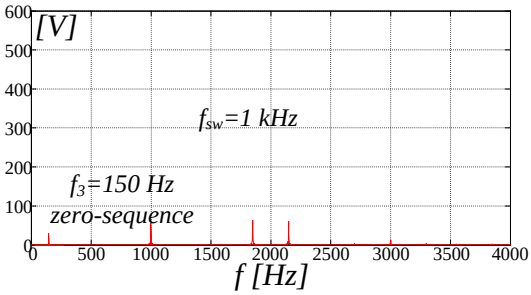


Fig. 2. 23. Harmonic spectrum of $V_{O'O''}$ with two isolated and asymmetrical three-phase inverters, V_{DC}=600 V, m=1, f_{sw}=1kHz, f1=50Hz

Table. 2.3. Space Vector combinations from Asymmetrical dual two-level inverter

$V_{A'O'}$	$V_{A''O''}$	$V_{A'O}$- $V_{A''O''}$	$V_{O'O''}$	V_m=$V_{A'O}$- $V_{A''O''}$+ $V_{O'O''}$
2-levels 1/3V_{DC}, -1/3V_{DC}	2-levels 1/3V_{DC}, -1/3V_{DC}	4-levels 1/6V_{DC}, 1/2V_{DC} -1/6V_{DC}, -1/2V_{DC}	6-levels 1/4V_{DC}, -1/4V_{DC} -1/6V_{DC}, 1/6V_{DC} -1/12V_{DC}, 1/12V_{DC}	14-levels 5/12V_{DC},-1/12V_{DC},1/3V_{DC},0, 1/4V_{DC},1/12V_{DC},3/4V_{DC},2/3V_{DC},7/12V_{DC},3/4V_{DC} -1/4V_{DC},-1/3V_{DC}, -2/3V_{DC},-5/12V_{DC}

2.1.4 Review on Common-Mode Voltage and Zero Sequence Current in a Dual Two-Level inverter fed an Open-end Winding machine

Common-mode voltages (CMV) generated by PWM in AC drives are the cause of shaft voltage buildup, electromagnetic interference issues, bearing and ground currents [34]-[36]. The CMV is the voltage existing between the system and a common reference point, usually the negative rail of the DC-Bus, or the earth.

In a conventional two-level inverter, the CMV features the switching frequency and can be expressed as:

$$V_{CM} = \frac{V_{AO} + V_{BO} + V_{CO}}{3} \tag{2.14}$$

being V_{AO}, V_{BO}, V_{CO} the inverter output voltages, referred to the mid-point O. In a conventional configuration the CMV coincides with the zero sequence voltage ZSV, which causes the flowing of zero sequence currents when suitable paths are provided. Two major common mode coupling paths exist in an electric motor: the stray capacitance between the stator core and the stator winding C_{ws} and the stray capacitance existing between the

stator windings and the rotor iron C_{wr}. Moreover, if the stator and rotor cores are electrically insulated, an air-gap capacitance C_g also exists, that is parallel connected to the bearing impedance. Several solutions have been proposed to reduce common mode voltages, among them, passive and active common-mode filters [37]-[40]. However, the introduction of these devices causes additional costs and major power losses. Thus, PWM methods are preferred for two-level inverters, although they cannot fully eliminate CMV [41]-[42]. In [41], a method is proposed exploiting only odd or even space vector combinations to reduce the CMV from $\pm V_{DC}/2$ to $\pm V_{DC}/6$, without zero vector states, in a conventional two-level inverter. Modulation-based strategies eliminating common-mode voltages by employing only a subset of output voltage space vectors are described in [43] and [44]. However, these techniques are burdened by a reduction of maximum phase voltage available, leading to a poor exploitation of the DC-Bus voltage. Multilevel inverters can provide excellent solutions in reducing the CMV thanks to the high number of space vector combinations available. The CMV per phase equivalent circuit of a Dual-Two-Level Inverter feeding an Open-End Winding Induction Motor is depicted in Fig. 2. 24. $V_{O'}$ and $V_{O''}$ are the common mode voltages generated by the two inverters.

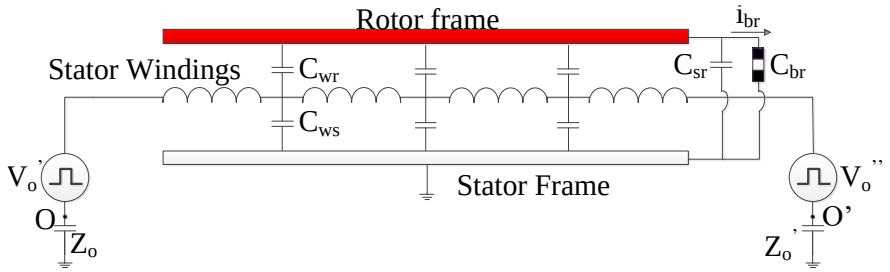


Fig. 2. 24. Common Mode Voltage per phase equivalent circuit for a Dual-Two-Level Inverter circuit feeding Open-End Winding Induction Motor

As mentioned in [45], in a Dual-Two-Level Inverter the equivalent CMV causes the circulation of bearing currents and is given by the sum of the common mode voltages of the two inverters V_{CM1} and V_{CM2}.

$$V_{CM1} = \frac{V_{A'O'} + V_{B'O'} + V_{C'O'}}{3} \qquad V_{CM2} = \frac{V_{A''O''} + V_{B''O''} + V_{C''O''}}{3} \tag{2.15}$$

$$V_{CM} = \frac{V_{A'O'} + V_{B'O'} + V_{C'O'} + V_{A''O''} + V_{B''O''} + V_{C''O''}}{6} = V_{CM1} + V_{CM2} \tag{2.16}$$

being: $V_{A'O'}$, $V_{B'O'}$, $V_{C'O'}$ the inverter-1 output voltage, referred to the mid-point O' and $V_{A''O''}$, $V_{B''O''}$, $V_{C''O''}$ the inverter-2 output voltage, referred to the mid-point O''.

Differently, the ZSV, causing the circulation of the zero-sequence current is given by the difference between the common mode voltages of the two inverters.

$$V_{ZSW} = V_{CM1} - V_{CM2} \quad (2.17)$$

Three dual-two level inverter topologies exist, namely: Symmetrical Isolated DC power supplies, Symmetrical Single DC power supply and Asymmetrical Isolated DC power supplies. According to tables 2.4, 2.5, and 2.6, these topologies generate different CMV and ZSV.

Table. 2.4, Voltage space vector combinations producing zero common-mode voltage in the motor phase windings with symmetrical DC-Buses

Vector	Space phasor combinations	V_{CM1}	V_{CM2}	CMV across machine phase V_{CM1}- V_{CM2}
OS	13’	$V_{DC}/6$	$V_{DC}/6$	0
	64’	$V_{DC}/3$	$V_{DC}/3$	0
OH	15’	$V_{dc}/6$	$V_{dc}/6$	0
	24’	$V_{DC}/3$	$V_{DC}/3$	0
OJ	35’	$V_{DC}/6$	$V_{DC}/6$	0
	26’	$V_{DC}/3$	$V_{DC}/3$	0
OL	31’	$V_{DC}/6$	$V_{DC}/6$	0
	46’	$V_{DC}/3$	$V_{DC}/3$	0
ON	51’	$V_{DC}/6$	$V_{DC}/6$	0
	42’	$V_{DC}/3$	$V_{DC}/3$	0
OQ	53’	$V_{DC}/6$	$V_{DC}/6$	0
	62’	$V_{DC}/3$	$V_{DC}/3$	0
Zero vector at origin	11’, 33’, 55’	$V_{DC}/6$	$V_{DC}/6$	0
	22’, 44’, 66’	$V_{DC}/3$	$V_{DC}/3$	0
	77’	$V_{DC}/2$	$V_{DC}/2$	0
	88’	0	0	0

Table. 2.5, CMV values for dual-two level inverter with symmetrical DC-Buses

Switching states	$V'_1(100)$	$V'_2(110)$	$V'_3(010)$	$V'_4(011)$	$V'_5(001)$	$V'_6(101)$	$V'_7(111)$	$V'_8(000)$
$V''_1(100)$	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$V_{DC}/6$	$-V_{DC}/3$
$V''_2(110)$	0	$V_{DC}/6$	0	$V_{DC}/6$	0	$V_{DC}/6$	$V_{DC}/3$	$-V_{DC}/6$
$V''_3(010)$	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$V_{DC}/6$	$-V_{DC}/3$
$V''_4(011)$	0	$V_{DC}/6$	0	$V_{DC}/6$	0	$V_{DC}/6$	$V_{DC}/3$	$-V_{DC}/6$
$V''_5(001)$	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$-V_{DC}/6$	0	$V_{DC}/6$	$-V_{DC}/3$
$V''_6(101)$	0	$V_{DC}/6$	0	$V_{DC}/6$	0	$V_{DC}/6$	$V_{DC}/3$	$-V_{DC}/6$
$V''_7(111)$	$V_{DC}/6$	$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/3$	$V_{DC}/6$	$V_{DC}/3$	$V_{DC}/2$	0
$V''_8(000)$	$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/3$	$-V_{DC}/6$	$-V_{DC}/3$	$-V_{DC}/6$	0	$-V_{DC}/2$

Table. 2.6, Voltage space vector combinations producing CMV in the motor phase windings in a dual-two level inverter with asymmetrical DC-Buses

Switching states	$V'_1(100)$	$V'_2(110)$	$V'_3(010)$	$V'_4(011)$	$V'_5(001)$	$V'_6(101)$	$V'_7(111)$	$V'_8(000)$
$V''_1(100)$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$V_{DC}/6$	$-5V_{DC}/18$
$V''_2(110)$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$5V_{DC}/18$	$-V_{DC}/6$
$V''_3(010)$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$V_{DC}/6$	$-5V_{DC}/18$
$V''_4(011)$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$5V_{DC}/18$	$-V_{DC}/6$
$V''_5(001)$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/18$	$-V_{DC}/6$	$V_{DC}/6$	$-5V_{DC}/18$
$V''_6(101)$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/6$	$V_{DC}/18$	$V_{DC}/18$	$-V_{DC}/6$
$V''_7(111)$	$-5V_{DC}/18$	$-7V_{DC}/18$	$-5V_{DC}/18$	$-7V_{DC}/18$	$-5V_{DC}/18$	$-7V_{DC}/18$	$-V_{DC}/6$	$-V_{DC}/2$
$V''_8(000)$	$7V_{DC}/18$	$5V_{DC}/18$	$7V_{DC}/18$	$5V_{DC}/18$	$7V_{DC}/18$	$5V_{DC}/18$	$V_{DC}/2$	$V_{DC}/6$

As early mentioned Zero-sequence currents may flow through motor windings when a single DC-Bus is used. In this case, CMV and ZSV can be attenuated using suitable PWM techniques. Differently, zero sequence currents cannot exist on a dual two-level inverter fed by two isolated DC-Buses. However, such a configuration requires two isolated transformers, although a floating DC bus capacitor can be used on one of the two inverters, as shown in Fig. 2. 19. The PWM strategy for a dual-two level inverter with symmetrical and isolated DC-Buses proposed in [8] is based on the Sine-PWM modulation, but the phase voltage provided by inverter-2 is shifted of 180°. Fig. 2. 25 shows the ZSV $V_{O'O''}$, while Fig. 2. 26 shows the phase stator currents, which do not contain a zero-sequence current. Although the zero-sequence current is blocked, the CMV is present and it assumes 7 voltage levels namely: $\pm V_{DC}/2$, $\pm V_{DC}/3$, $\pm V_{DC}/6$ and 0, as depicted in Fig. 2. 27. Fig. 2. 28 shows the *a*-phase voltage and the *a*-phase current obtained with a conventional sine-PWM. A space vector PWM for a dual two-level inverter using two isolated power supplies is shown in [48]. It exploits the PWM technique proposed in [49], which relies on the concept of 'effective voltage'.

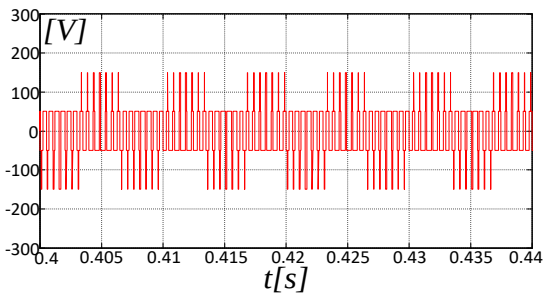


Fig. 2. 25. ZSV $V_{O'O''}$ for Isolated Symmetrical Dual-Two Level Inverter in [8] with Sine-PWM modulation

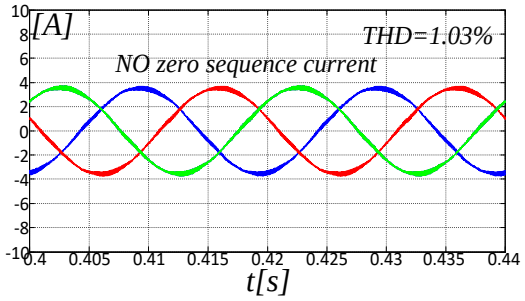


Fig. 2. 26. Phase Currents for Isolated Symmetrical Dual-Two Level Inverter in [8] with Sine-PWM modulation

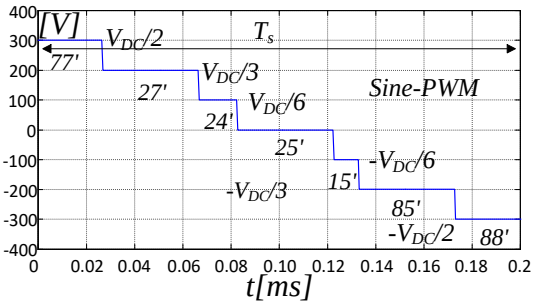


Fig. 2. 27. CMV for a Symmetrical Dual-Two Level Inverter in [8] with Sine-PWM modulation

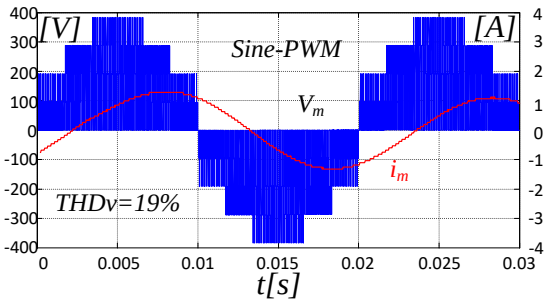


Fig. 2. 28. Phase voltage V_m and phase current i_m for a Symmetrical Dual-Two Level Inverter in [8] with Sine-PWM modulation

Inverter switching times are computed directly from the instantaneous reference voltage, without sector identification, resulting in a 25% reduction of the execution time if compared with traditional Space Vector PWM (SVM) algorithms. Specifically, the entire hexagon is divided into six sub-hexagons with centers in A, B, C, D, E and F and one inner hexagon with center in O, Fig. 2. 29. The voltage reference $\mathbf{OV_s}$ is synthetized as the composition of the vector **OA** (inverter-1 output voltage V_s') and the vector $\mathbf{AV_s}$ (inverter-2 output voltage V_s''). Sector identification is accomplished by hysteresis level comparators. Two main benefits are obtained: no zero sequence currents can occur, owing to the isolated power supplies structure, all space vector combinations are exploited, thus covering the entire available speed range. The maximum amplitude of the fundamental component of the voltage in linear modulation mode is $\frac{2}{3}\frac{\sqrt{3}}{2}V_{DC}$=0.57 V_{DC}. However, bearing currents may circulate, because the CMV assumes the waveform depicted in Fig. 2. 27.

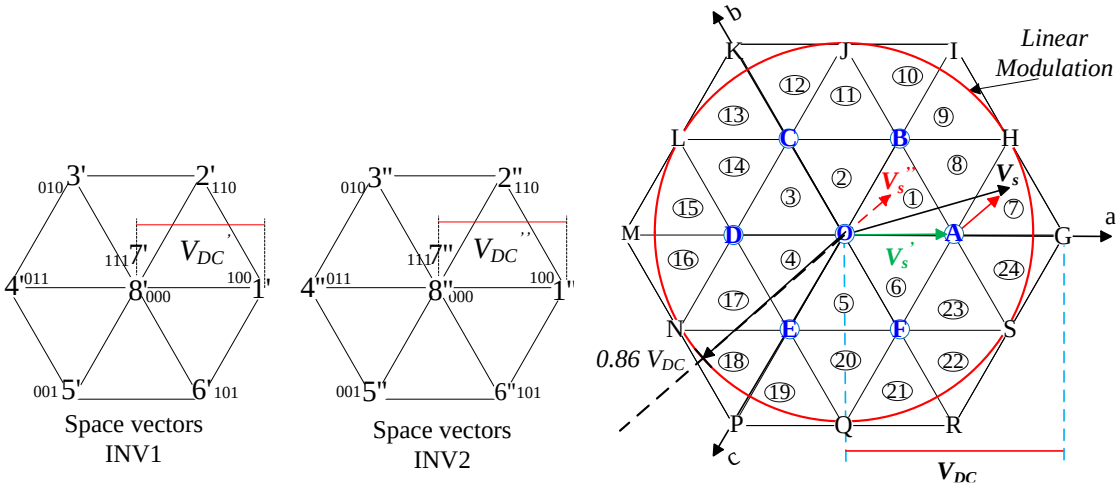


Fig. 2. 29 Space vectors for a dual two-level inverter

In [32] some hybrid PWM methods are proposed in order to reduce the CVM in a symmetrical dual two-level inverter with isolated power supplies. This paper explains that the shaft voltage which causes the bearing

currents is a replica of CMV. As shown in Fig. 2. 27 using a Sine-PWM, the CMV assumes 7 voltage levels.

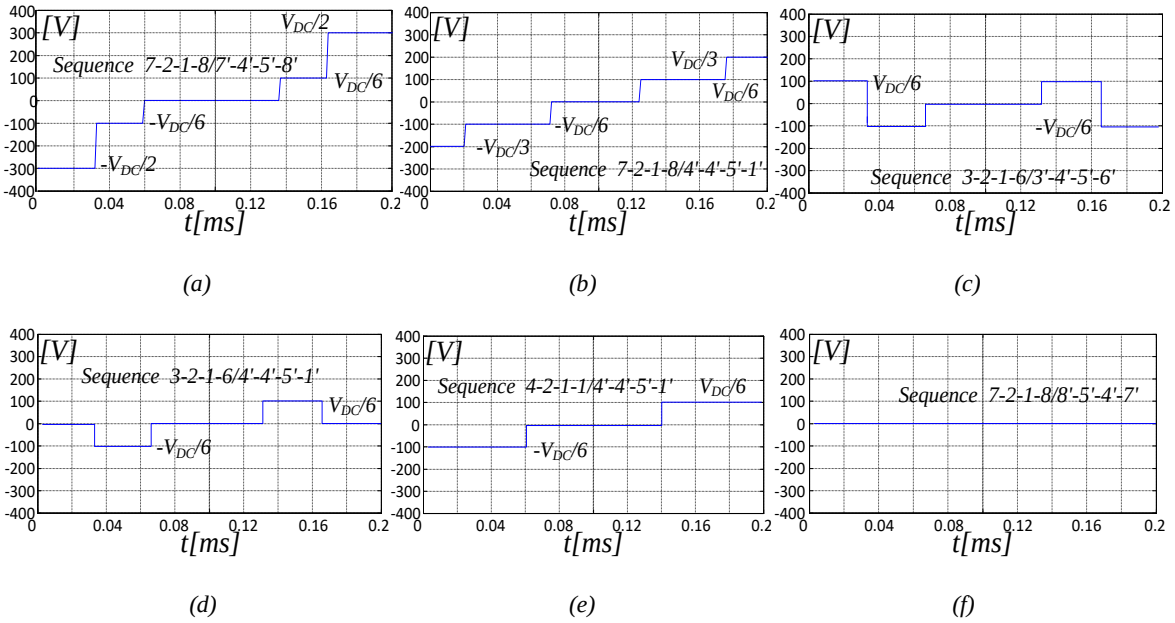


Fig. 2. 30. CMV levels in a Dual-two level Inverter proposed in [32]. a) Sine-PWM. b) PWM2. c) PWM7. d) PWM9. e) PWM15 and f) PWM25

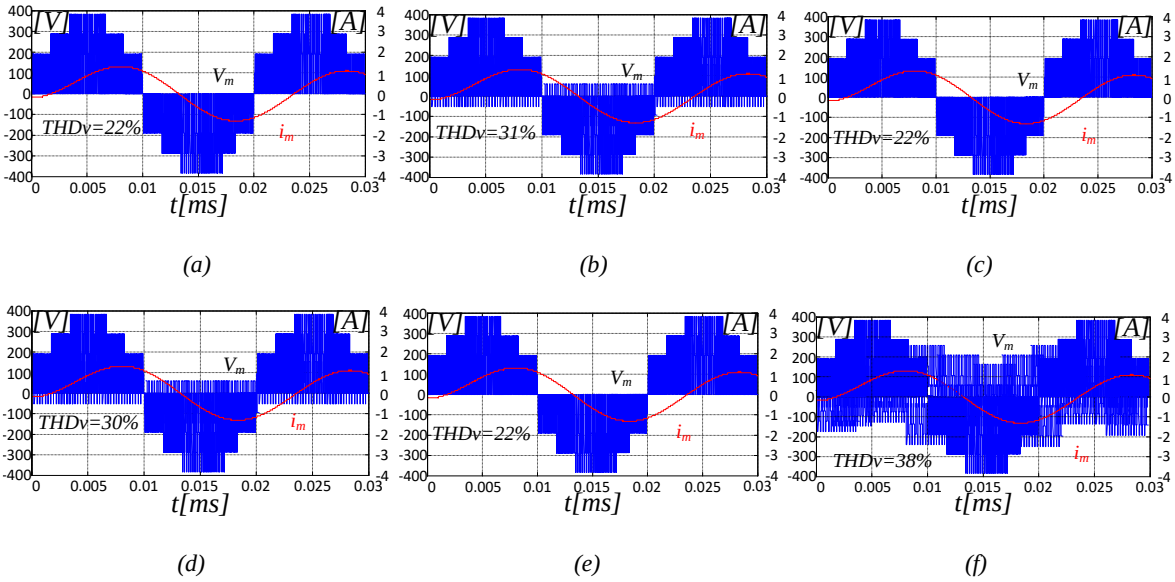


Fig. 2. 31. Phase voltage and phase current in a Dual-two level Inverter proposed in [32]. a) Sine-PWM. b) PWM2. c) PWM7. d) PWM9. e) *PWM15* and f) *PWM25*

Some PWM strategies (PWM2, PWM7, PWM9, PWM15 and PWM25) are proposed in [32]. Fig. 2. 30 and Fig. 2. 31 show CMV, phase voltage and phase current waveforms, obtained using the aforementioned techniques. Output voltages obtained using PWM7 and PWM15 are similar to those generated by SVPWM, but they are preferable because the CMV can assume only three levels, namely: +/-VDC/6 and 0. PWM9 gives lower CMV and shaft voltages, but at the cost of increasing the power losses and THD.

The main drawback of a dual two-level inverter with a with single power supply relies in the circulation of a zero-sequence current in the motor windings that cause a worsening of the THD and additional power losses. In [24], the ZSV is eliminated by exploiting the technique proposed in [41], [42], as shown in Fig. 2. 32, Fig. 2. 33 and Tab. 2.4.

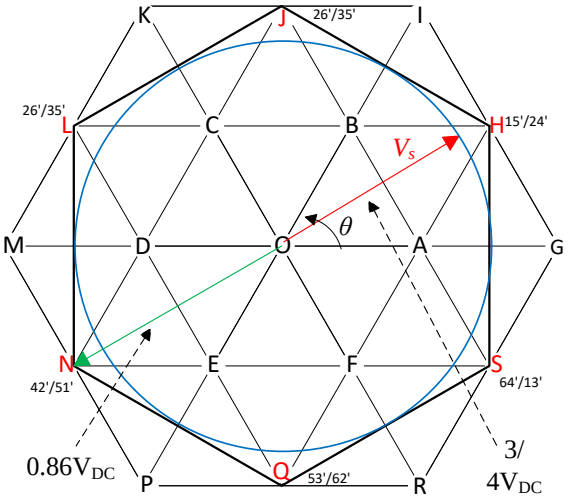


Fig. 2. 32. Sequence Odd or Sequence Even Space Vector Combination with no CMV in Dual-two level inverter in [24]

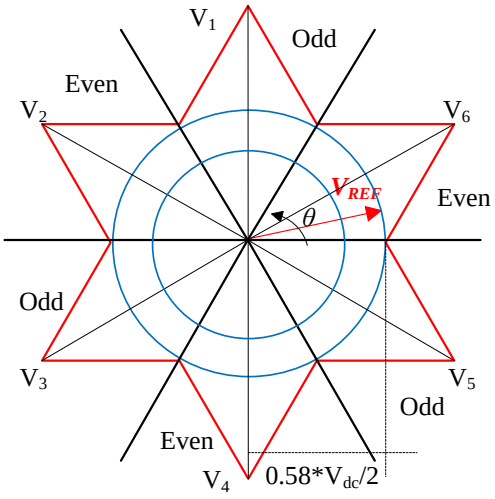


Fig. 2. 33. Only Odd or Only Even Space Vector Combination in [41], [42] in a conventional two level inverter

However, the DC-Bus exploitation is not optimal, as the maximum amplitude of the fundamental voltage component is:

$$V_{m-pk} = \frac{2}{3}V_s = \frac{2}{3}\frac{3}{4}V_{DC} = 0.5V_{DC} \tag{2.18}$$

This is same value obtained with a conventional two-level inverter with Sine-PWM. Hence, it is 15% lower than that obtainable by using all the 64 available space vector combinations, as discussed in [46], [32], [48] and [50]. In order to increase the output voltage range, the addition of a boost converter in the DC-link is suggested in [50].

Fig. 2. 34a and Fig. 2. 34b depict the pole voltage for inverter-1 and inverter-2, respectively. Fig. 2. 34c and Fig. 2. 34d show the phase voltage V_m and the phase current, respectively. The ZSV is made null by using sequences of only odd or only even inverter states, as depicted in Fig. 2. 34e and Fig. 2. 34f. The CMV defined as in [45], is kept constant to $-V_{DC}/6$, avoiding bearing currents. According to this method a single DC-link voltage is used, while, the CMVs for each inverter is held to $\pm V_{DC}/6$ (based on odd or even sequence) using space vector combinations proposed in [41] and [42]. A space vector based PWM switching scheme is proposed in [51] which achieves three-level voltages using all space vector locations with a single DC-Bus voltage. In order to improve the DC-Bus exploitation the authors propose a modification of the reference vector if its tip is located outside the boundary of hexagon HJLNQS, as shown in Fig. 2. 35. Such a scheme [51] reduces the zero-sequence current by dynamically balancing the ZSVs, exploiting a time relocation algorithm.

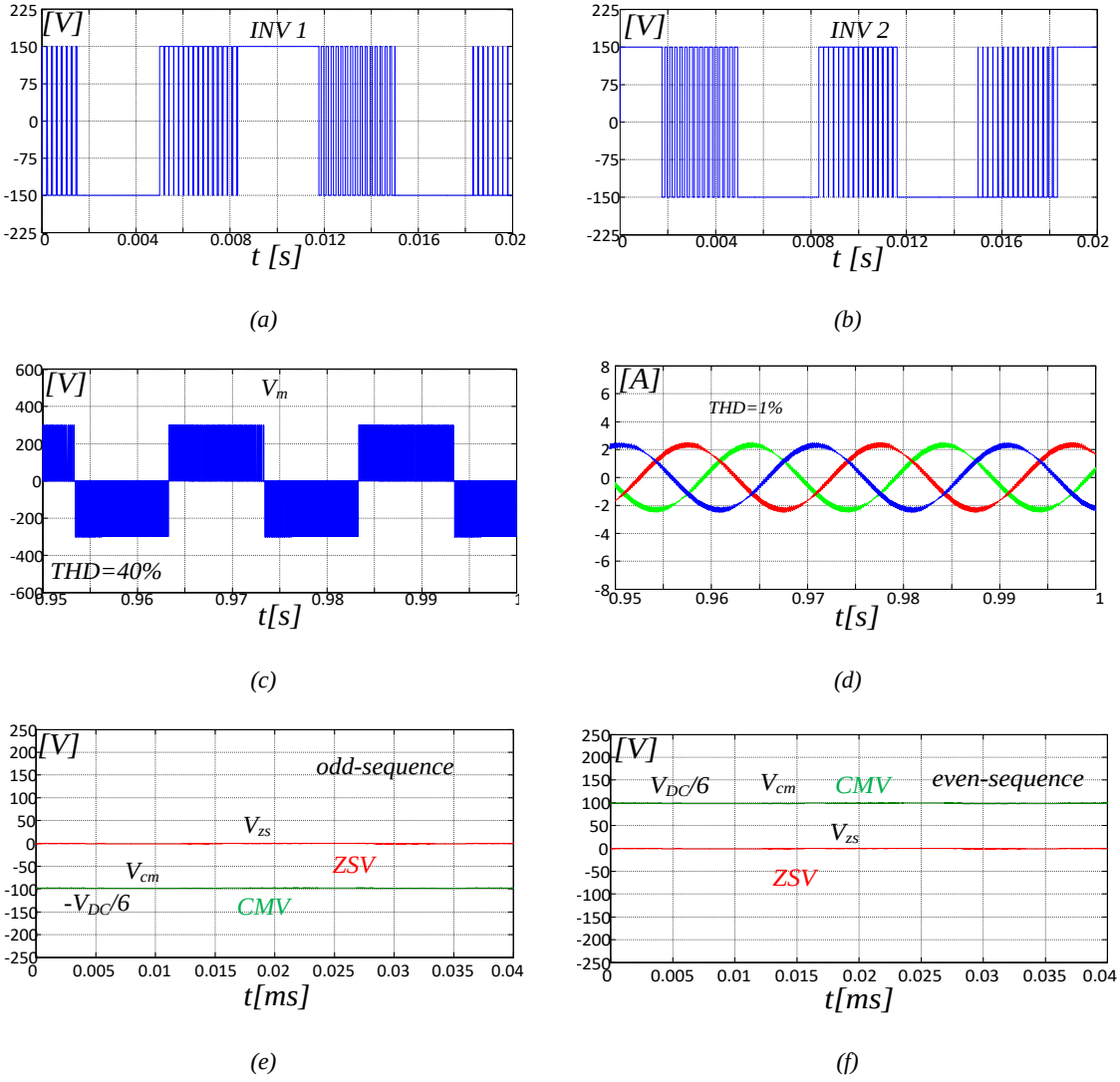


Fig. 2. 34 Simulation results in [24], m=0.2, fsw=4.8KHZ. a) Output voltage of inverter-1. b) Output voltage of inverter-2. c) Phase voltage. d) Phase currents. e) CMV and ZSV with only odd-sequence. f) CMV and ZSV with only even-sequence.

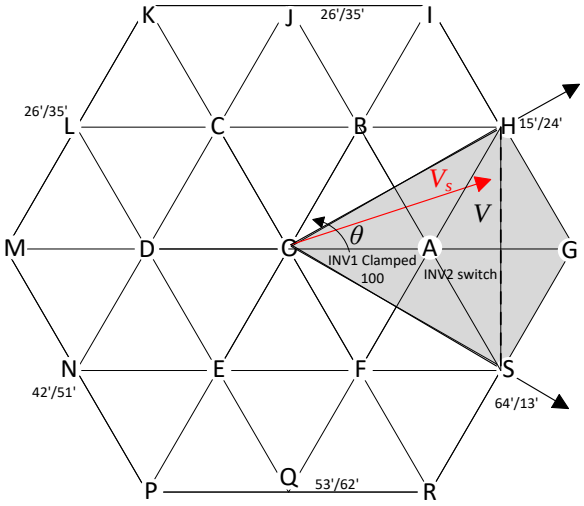


Fig. 2. 35. Principle of alternate sub hexagonal centre proposed in [51]

The basic switching algorithm described in [49] and [54] for a conventional two-level inverter is extended to the dual-two level inverter by suitably computing the switching times. The two inverters operate alternatively, when the inverter-1 is switching, the inverter-2 is clamped and vice versa. Inverter operations are shown in Tab. 2.7.

Table. 2.7, Inverter roles for realizing the reference vector in [51]

NSHC	A	B	C	D	E	F
INV1	100	Switching mode	010	Switching mode	001	Switching mode
INV2	Switching mode	001	Switching mode	100	Switching mode	010

The reference vector **OV** can be split into two components namely **OA**, which is generated by inverter-1, and **AV**, which is generated by inverter-2. Hence, this method refers to six hexagons, namely OBHGSF, OCJIHA, ODLKJD, OENMLC, OFQPND and OASRQE, having respectively centers in A, B, C, D, E and F and called sub-hexagonal centers (SHCs). The SHC, which is situated in the closest proximity to the tip of the reference voltage space vector is called Nearest sub-hexagonal center (NSHC). This is found from the reference voltages as explained in [55]. In contrast with the algorithm proposed in [24], the zero vector time T_0 is dynamically changed without changing the total switching time. Thus, T_0 is redistributed into two unequal time periods, $(1-x)T_0$ and xT_0 ,such that the average of the zero sequence voltage along each switching time is forced to be zero. The largest circle inscribed into the hexagon HJLNQS defines the boundary of linear modulation mode and it is same of space vector schemes proposed in [24], [52] and [53], where, however, the DC-link is underutilized. If ZSV is forced to zero, a non-centre-spaced PWM results in a higher current ripple and consequently a higher THD, as shown in Fig. 2. 36a.

Fig. 2. 36b shows the phase voltage and phase current of an isolated dual-two level inverter when all space

vector combinations are exploited, suppressing the zero-sequence, while Fig. 2. 36c shows the phase voltage and phase current with the method proposed in [55] with a single DC-link.

A PWM switching strategy aimed at the suppression of zero sequence currents is proposed in [56] and [57] using auxiliary bidirectional switching devices, as depicted in Fig. 2. 37. This configuration permits to improve the DC-Bus utilization compared to the dual two-level inverter with a single power supply, which exploits only space vectors with zero ZSV. However, four additional bidirectional power devices are required to isolate both inverters. A suitable trade off must be then found between power losses caused by the additional devices and power losses caused by zero sequence currents.

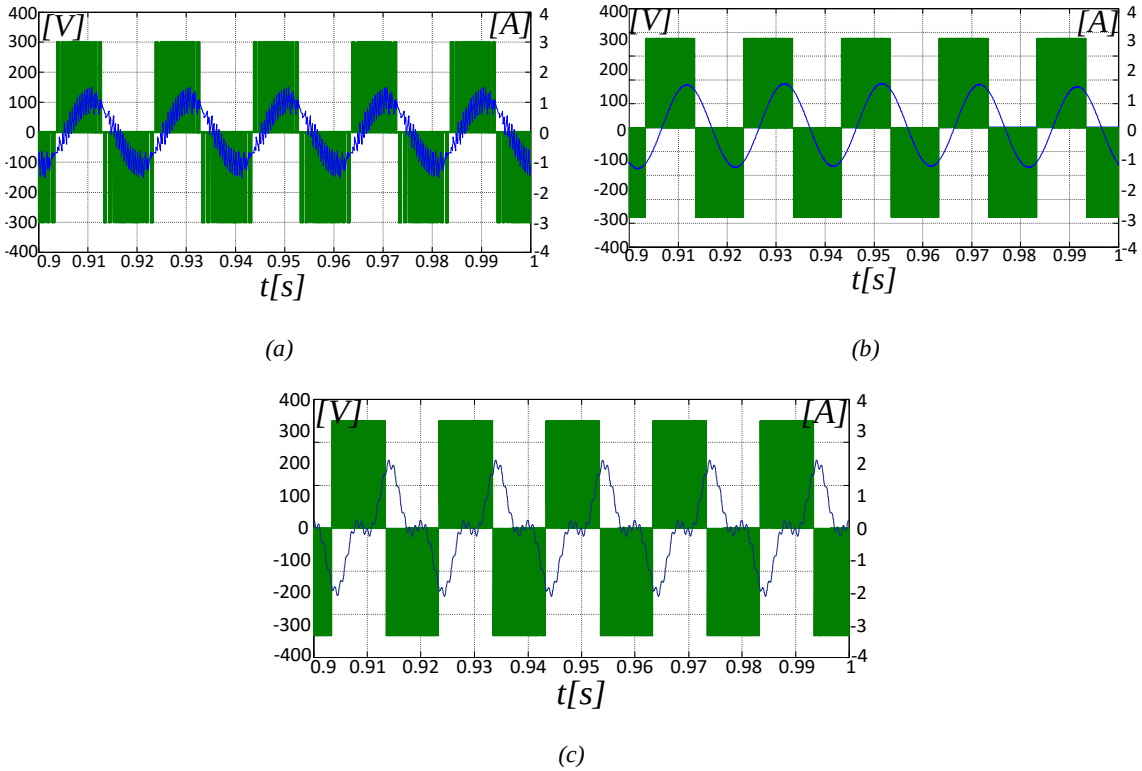


Fig. 2. 36. Phase voltage and phase current. a) Single DC-Bus voltage [51]. b) Isolated DC-Buses. c) Single DC-Bus voltage

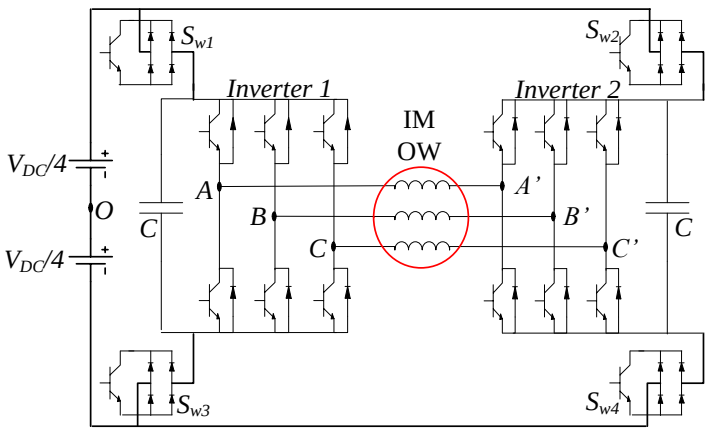
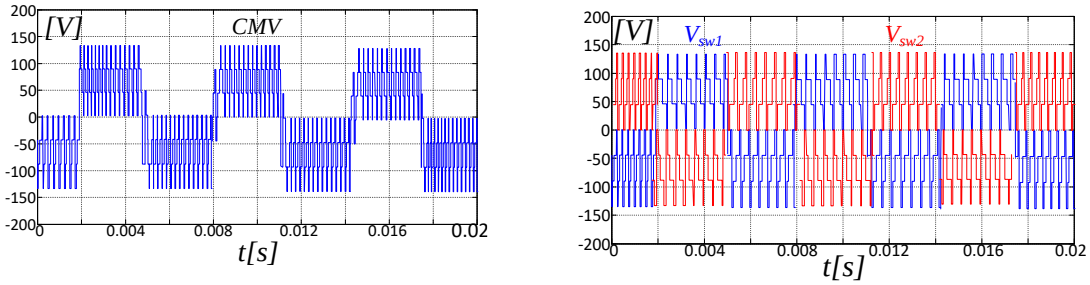


Fig. 2. 37. Dual-Two-Level Inverter circuit feeding Open-End Winding Induction Motor with auxiliary power devices

When space vector combinations S, H, J, L, N, and Q are exploited, the auxiliary switch may be turned on preventing the circulation of the zero-sequence current. When G, I, K, M, P and R combinations are instead used, the zero-sequence current needs to be suppressed. This is done by an auxiliary switch, regaining a 15% DC Bus voltage utilization lost according to methods presented in [24] and [51]. This method requires a sector identification for all 24 sectors as in [51] and the switching algorithm used is the same of that proposed in [49] and [52] for inner sectors and [55] for the outer sectors. Applying the Kirchhoff's voltage law around the loop consisting of the DC power supply, S_{w1}, C_1 and S_{w3}, it is obtained that:

$$V_{sw1} = -V_{sw3} \tag{2.19}$$

where S_{w1} and S_{w3} are the auxiliary switches of inverter-1. Hence, when a given pair of auxiliary switches is turned off, the voltages across these switches have the same amplitude but are of opposite sign (i.e. these voltage waveforms are in anti-phase with respect to each other). Thus, the sum of the instantaneous voltages across that pair of auxiliary switches is always zero. This means that, when a given pair of auxiliary switches is turned off, the waveform of the voltage across one of these switches contains the triple harmonics of the CMV. Fig. 2. 38a shows the CMV, Fig. 2. 38b shows the voltage across S_{w1} and S_{w3}. Since the space vector combinations which give a non-zero CMV are exploited, the last is present in the diagram of Fig. 2. 27. This represents a further disadvantage of the method, in addition to extra switching losses and auxiliary power devices.



(a) *(b)*

Fig. 2. 38. a) CMV in [56], m=0.4, fsw=4.8KHZ. b) Voltage across auxiliary switches in [56], m=0.4, fsw=4.8KHZ

A new decoupled space-vector-based PWM is proposed in [57] to eliminate zero-sequence currents. This technique exploits the dependence of the zero-sequence voltage on the placement of the zero-vector of individual inverters. It is shown, in fact, that the zero-sequence voltage of the dual-inverter system is suppressed by forcing the average zero-sequence voltage of the individual inverters to zero, in each sampling-time interval. Switching times are computed by the algorithm adopted in [12]. This strategy, therefore, achieves a dynamic balancing of the zero-sequence current, it is very easy to implement and doesn't require a sector identification with look up table. The main disadvantage relies in a poor exploitation the of the DC-Bus voltage. Thus, the authors propose

the introduction of an additional boost converter as in [24]. Such a drawback is outweighed by the advantage of operating with a single DC power supply.

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3 Chapter: Overvoltage Phenomena in AC Motor Drives

This chapter deals with several issues associated with Overvoltage Phenomena on AC Motor Drives. First, overvoltage generation on AC Motor is discussed, and suitable mathematical models are presented. The second part deals with overvoltage mitigation techniques proposed in the past and their effectiveness. Finally, an overvoltage suppression method is proposed exploiting an Open-end-Winding AC Motor Drives. Experimental tests are shown in order to verify the consistence of the proposed method.

3.1 Study and presentation of the problem

The development of new power electronic technologies, in particular, has powered a constant increment of the switching frequency in the Variable Frequency Drives (VFD) sector. The first power electronic component has been designed in 1952 by R.N. Hall. It was composed by germanium and had a reverse voltage blocking capability of 200 V, current rating of 35 A and low switching frequency. This power semiconductor was uncontrollable from external signals.

The first semi-controlled power device developed was the thyristor which is able to work with very high voltage level (7kV), high current rating (2kA) but low switching frequency (<100 Hz). Moreover, the thyristor can be controlled only to turn-on while the turn-off depends on the external circuit. The thyristor has been replaced by Gate Turn-Off Thyristors (GTO), which have higher switching frequency(<1kHz) and can be turned off by a suitable gate signal. Very high switching frequencies have been achieved with the Metal Oxide Semiconductor Field Effect Transistor (MOSFET), which is able to switch from 100 kHz to 1MHz but at the cost of a lower reverse voltage blocking capability (<1kV) and lower current rating (<100 A) if compared with GTOs.

The most diffused power device in electric motor drives applications is today the Insulated-Gate Bipolar Transistor (IGBTs). It has completely replaced the bipolar transistor thank to a high breakdown voltage (3kV), high current rating (1kA) and high switching frequency (1kHz to 100kHz). Basically, the IGBT combines the advantages of the GTO, in terms of high breakdown voltage, and of the MOSFET, in terms of high switching frequency. Fig. 3. 1 shows the typical operating ranges of most common power electronic devices and their applications.

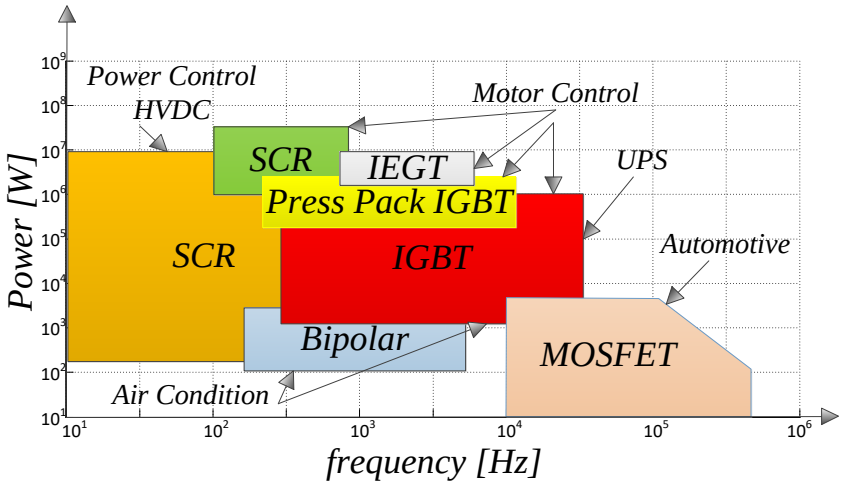


Fig. 3. 1 Power devices and applications

Standard AC Electric Motors are today operated with Pulse Width Modulation (PWM) voltage source inverters from 0.1 to 800 kW using I*GBT*s. These are the preferred semiconductor devices due to their short rise time, ranging from 50 to 400 ns, and the voltage gate control, resulting in simpler and faster driver circuits. PWM operated converters for motor drives applications have become very popular due to:

- High Efficiency (97% to 98%)
- High switching frequency
- Low output current THD
- Low sensitivity to line transients
- Constant high input power factor
- Multi-motor application capability
- Low and zero-speed operations
- Minimum power line notching
- Small size
- Ride-through capability
- Open circuit protection
- Common Bus regeneration
- Wide speed range
- Excellent speed regulation

Furthermore, IGBT inverters feature smaller heat sinks, if compared with GTO inverters, and the higher switching frequency reduce motor noise in the audible range. However, if on one side, the high switching frequency of IGBT based inverters improves the efficiency of the entire system, on the other side, the fast variation of the voltage may produce unintended consequences. Specifically, overvoltages may occur at the stator winding terminals if the machine and the inverter are connected through a long power cable. These overvoltages may produce destructive stresses on the motor insulation [1]. Such a phenomenon is known as'' *Transmission Line Effect*'', ' *'Reflected Wave*'' or ' *'Standing Wave*''[2]-[6].

3.1.1 Transmission Line Theory and Factors affecting the Overvoltage

According to the transmission line theory, a mismatch between the impedance of the motor and the impedance of the cable is able to reflect back inverter generated voltage pulses, when they reach the motor terminals. A graphical analysis is shown in [2] and [7] to describe how the waves are reflected.

Another method called ''Bounce Diagram'' is often exploited to describe the voltage wave propagation through the cable, adopting the Laplace transformation of each wave [8]. Fig. 3. 2 shows a model of a drive system [8], [9] in which the motor cable is modeled as a long transmission line with distributed parameters and length *l*. Its *Characteristic Impedance* is $Z_0 = \sqrt{L/C}$, where L is the cable inductance per unit length and C is the cable capacitance per unit length. The motor stator winding is also modelized as a long transmission line with a *High-Frequency Characteristic Impedance* Z_m.

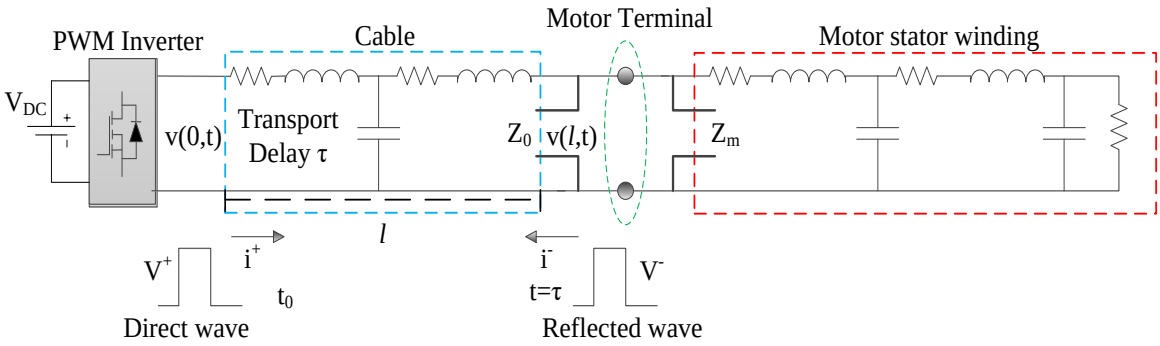


Fig. 3. 2 Model of a drive system with long cable

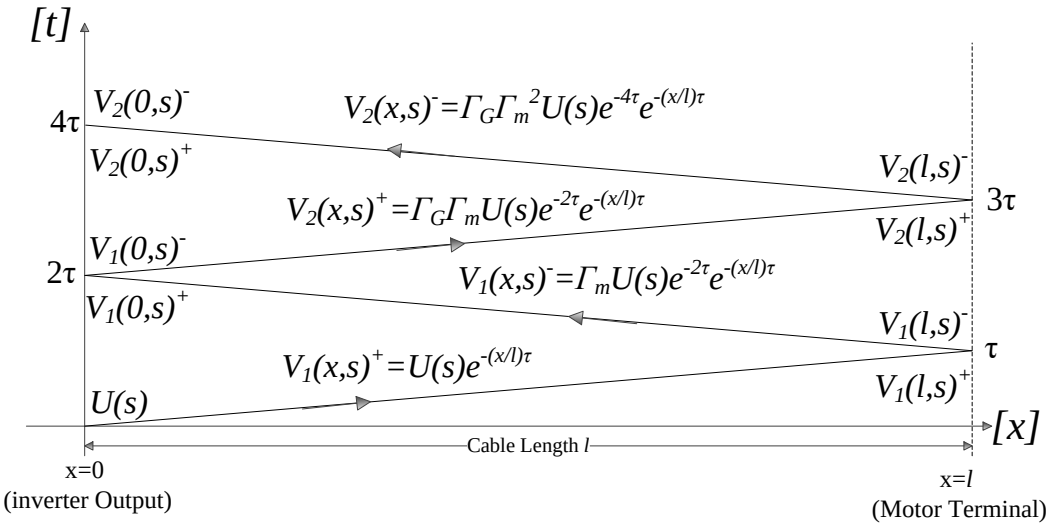


Fig. 3. 3 Bounce Diagram

Fig. 3. 3 shows a bounce diagram in which the progression of the leading edges of the incident and reflected voltage waves are displayed as a function of both time *t* and position *x*. Let's assume that the length of the cable is *l* and the inverter and motor are located at *x=0* and *x=l*, respectively. The PWM voltage generated from the inverter is *u(t)* and its Laplace transformation is *U(s).* When a voltage pulse $V_1(0,0)^+$ of magnitude equal to $u(t)=V_{DC}$, generated at time t_0, is applied to the cable, a current $i(0,0)^+$will circulate:

$$i(0,0)^+=\frac{V(0,0)^+}{Z_0} \tag{3.1}$$

The amplitude of the voltage pulse at a distance *x* from the inverter is $v_1(x,t)^+$. Since *u(t)* is assumed to be delayed by *(x/l)τ*, where *τ* is the *Cable Propagation Time or Transport Delay Time* and depends on cable parameters $\tau = l\sqrt{LC}$, the Laplace Transformation of forward voltage $v_1(x,t)^+$ is given by:

$$V_1(x,s)^+ = U(s)\,e^{-(x/l)\tau s} \tag{3.2}$$

Once that $v_1(x,t)^+$ reaches the motor terminal *x=l* at time t=τ, part of it is reflected back toward the inverter, producing a reflected voltage pulse $v_1(x,t)^-$ and a reflected current $i(x,t)^-$:

$$i(l,\tau)^-=\frac{V(l,\tau)^-}{Z_0} \tag{3.3}$$

The reflected voltage at the motor terminal is due to a mismatch between motor impedance and surge impedance of the cable. To understand the impedance mismatch condition, let's consider the high-frequency characteristic impedance Z_m expressed as:

$$Z_m = \frac{V(x,t)^+ + V(x,t)^-}{i(x,t)^+ + i(x,t)^-} \tag{3.4}$$

Assuming with Γ_m the *reflection coefficient* at the motor terminal as:

$$\Gamma_m = \frac{V(l,t)^-}{V(l,t)^+} \tag{3.5}$$

and taking into account eq. (3.1), (3.3), (3.4) and (3.5), the reflection coefficient Γ_m can be written as a function of motor impedance Z_m and surge impedance of the cable Z_0:

$$\Gamma_m = \frac{Z_m - Z_0}{Z_m + Z_0} \tag{3.6}$$

Thus, the reflected voltage at the motor terminal $x=l$ is $v_1(l,t)^-$ and its Laplace transformation is given by:

$$V_1(l,s)^- = \Gamma_m V_1(x,s)^+ = \Gamma_m U(s) e^{-\tau s} \tag{3.7}$$

The reflected voltage at a distance x from the inverter is:

$$V_1(x,s)^- = \Gamma_m V_1(x,s)^+ = \Gamma_m U(s) e^{-\tau s} e^{-(x/l)\tau s} \tag{3.8}$$

This voltage $v_1(x,t)^-$ reoccurs at the inverter side. The reflection coefficient Γ_G at the inverter terminal is given by:

$$\Gamma_G = \frac{Z_G - Z_0}{Z_G + Z_0} \tag{3.9}$$

being Z_G the inverter impedance. Another reflected voltage at the inverter output $v_2(0,t)^+$ travels to the motor and it is given by:

$$V_2(0,s)^+ = \Gamma_G V_1(0,s)^- = \Gamma_G \Gamma_m U(s) e^{-2\tau s} \tag{3.10}$$

Thus, at position x, eq. (10) becomes:

$$V_2(x,s)^+ = \Gamma_G V_1(x,s)^- = \Gamma_G \Gamma_m U(s) e^{-((2l+x)/l)\tau s} \tag{3.11}$$

Note that when Z_m is much larger than Z_0, Γ_m is close to one and when Z_G is much smaller than Z_m, the reflection coefficient $\Gamma_G=-1$. $\Gamma_m=1$ implies that the wave is fully reflected at the motor terminal without the phase change, while $\Gamma_G=-1$ means that the wave is fully reflected at the inverter output with a 180° phase change. This bouncing process occurs infinitely as shown in Fig. 3. 3. According to the Bounce Diagram, the voltage on

the cable is given by the sum of infinite reflected waves. For simplicity, $V(x,t)^+$ is the sum of forward-traveling voltages and $V(x,t)^-$ is the sum of backward-traveling voltages:

$$V(x,s)^+ = U(s)\left[e^{-(x/l)\tau s} + \Gamma_G\Gamma_m e^{-((2l+x)/l)\tau s} + \Gamma_G^{\,2}\Gamma_m^{\,2} e^{-((4l+x)/l)\tau s} + \ldots\ldots\right] = \frac{U(s)e^{-(x/l)\tau s}}{1-\Gamma_G\Gamma_m e^{-2\tau s}} \tag{3.12}$$

$$V(x,s)^- = U(s)\left[\Gamma_m e^{-((2l+x)/l)\tau s} + \Gamma_G\Gamma_m^{\,2} e^{-((4l+x)/l)\tau s} + \ldots\ldots\right] = \frac{U(s)\Gamma_m e^{-((2l+x)/l)\tau s}}{1-\Gamma_G\Gamma_m e^{-2\tau s}} \tag{3.13}$$

Thus, the Laplace Transformation of the voltage at any point x on the cable is given by:

$$V(x,s) = V(x,s)^+ + V(x,s)^- = U(s)\frac{e^{-(x/l)\tau s} + \Gamma_m e^{-2\tau s} e^{-(x/l)\tau s}}{1-\Gamma_G\Gamma_m e^{-2\tau s}} \tag{3.14}$$

where $0<|\Gamma_m|$ and $|\Gamma_G|<1$.

Replacing $x=l$ into eq. (3.14), the motor terminal voltage is given as a sum of odd transport delayed signals from the inverter to the motor feeding cable:

$$V(l,s) = U(s)\frac{(1+\Gamma_m)e^{-2\tau s}}{1-\Gamma_G\Gamma_m e^{-2\tau s}} \tag{3.15}$$

The result of these reflected voltage at the motor terminal, which travel on the cable from inverter to motor and vice versa, is displayed in Fig. 3. 4.

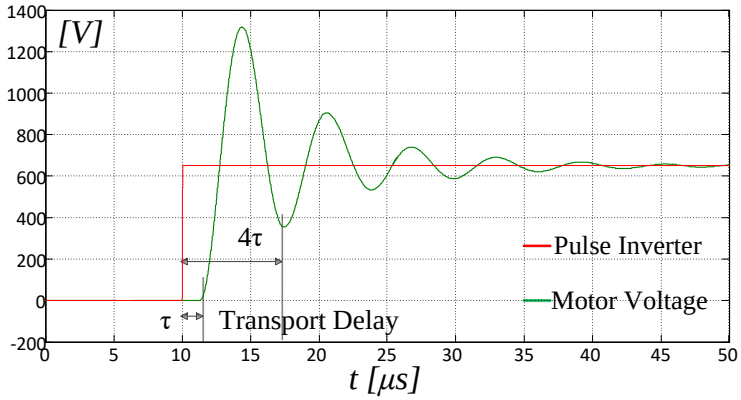


Fig. 3. 4 Motor voltage Waveform as a function of the time, calculated at distance x=l on motor terminals

The pulse travels at the *Wave Propagation Velocity v* and pulse shape is propagated without distortion down to the line. The wave propagation velocity is a function of cable inductance L per unit length and cable

capacitance C per unit length, but it may also be defined using permeability μ, permittivity ε of the dielectric material between conductors and *Speed of Light c* (3.0×10^8 m/s):

$$v = \pm \frac{1}{\sqrt{LC}} = \frac{1}{\sqrt{\mu\varepsilon}} = \frac{c}{\sqrt{\varepsilon_r}} \tag{3.16}$$

The +/- sign means that both forward $V(x,t)^+$ and reverse $V(x,t)^-$ waves travel at the same velocity. If the conductors used are separated, the permittivity ε_r=1 and the wave propagation velocity v=c.

Another parameter that can be introduced to study the overvoltage phenomenon is the *Cable Oscillation Time* T_{cycle}. It is calculated taking into account that the wave must travel four times along the cable to accomplish a full oscillation cycle:

$$T_{cycle} = 4\tau = \frac{4l}{v} = 4l\sqrt{\mathrm{LC}} \tag{3.17}$$

Thus, *Cable Oscillation Frequency* f_0 is inversely proportional to cable length:

$$f_0 = \frac{1}{T_{cycle}} = \frac{1}{4l\sqrt{\mathrm{LC}}} \tag{3.18}$$

From eq. (3.18) it is deduced that high oscillation frequencies occur at short cable lengths and vice versa.

Taking into account eq. (3.15), the maximum value of overvoltage at the motor terminal can be expresses as:

$$V_{m-pk} = (1 + \Gamma_m) V_{DC} \tag{3.19}$$

where V_{DC} is the DC-Bus voltage of the inverter as well as the magnitude of voltage $V(x,t)^+$.

Hence, the amplitude of the voltage pulse $V(x,t)^-$ reflected back toward the inverter, causing overvoltages at the motor terminals, depends on Γ_m. Thus, no reflected voltage occurs if Γ_m =0 and Z_m=Z_0. This is known as M*atched Condition* and is an ideal condition, because normally the value of Z_m is several orders of magnitude greater than Z_0, especially in low-power motors. With Z_m> Z_0, the motor and the cable are operated in a *Mismatched Condition*. For motors less than 5HP, Z_m ranges from 500 to 4000 Ω, while Z_0 with a typically ranges from 30 to 200 Ω. Hence, in a heavy mismatching condition Z_m>> Z_0, the magnitude of reflected voltage pulse $V(x,t)^-$ is about equal to the magnitude of voltage pulse $V(x,t)^+$. This generates at the motor terminals a first voltage oscillation whose amplitude can reach twice that of the inverter output voltage, as shown in eq. (15) and eq. (18). Following oscillations have smaller amplitudes due either to cable resistance damping, or reflection coefficient mismatch occurring at both drive and motor ends.

Factors affecting overvoltage phenomena at the motor terminals are:

1. Cable length

2. Motor load
3. Spacing of the pulses
4. Magnitude of the pulses
5. Rise/fall time of the pulse

According to eq. (3.15) and eq. (3.18), the impedance mismatch between Z_m and Z_0 determinates the overvoltage magnitude, while, the voltage rise/fall time determinates the *Critical Cable Length* l_c. Using PWM inverters with high carrier frequency, the reflected voltage may not fully decay before the generation of the following pulse. In this case, charge trapped on the cable can generate at the motor terminals a voltage greater than twice the inverter output one. In this situation, the system works in the *Pulse-Dropping Region* [10] and the *Cable Oscillation frequency* f_0 plays a fundamental rule.

According to the above discussion, two overvoltage conditions may exists:

1. Motor Overvoltage < 2 DC Bus voltage.
2. Motor Overvoltage > 2 DC Bus voltage.

These two particular cases will be discussed in the next sections.

3.1.2Motor overvoltages < 2 DC Bus voltage

An overvoltage at motor terminals lower than twice the DC Bus voltage occurs when the reflected voltage have fully decayed before the generation of the following pulse, as depicted in Fig. 3. 5. As mentioned earlier, factors contributing to motor over-voltage are cable length and impedance mismatched between cable impedance Z_m and $Z_{0,}$ but in this case, inverter output voltage amplitude and rise/fall time are predominant factors [11], while carrier frequency has a little effect.

Fig. 3. 5 shows a worst case analysis considering a *150 m* of #12 AVG PVC cable, V_{DC}*=650 V* and IGBT rise time of *50ns*. The cable is initially uncharged and a full cable to motor surge impedance mismatch, Γ_m*=1*is considered. The critical cable length l_c is defined as the cable length producing a 2 pu overvoltage, as depicted in Fig. 3. 6. Fig. 3. 7 shows the overvoltage amplitude as function of voltage rise time, taking into account a 150m long cable.

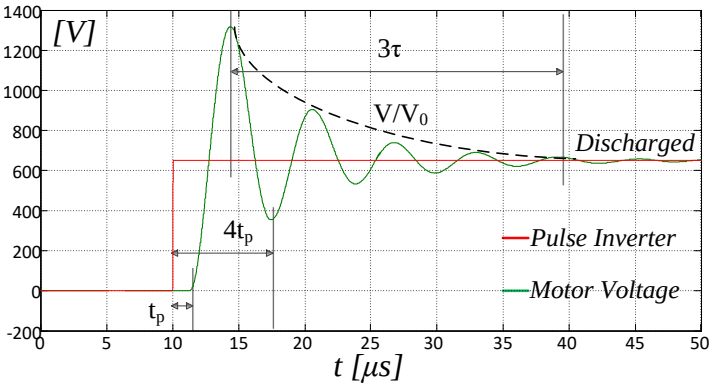


Fig. 3. 5 Motor Overvoltage <2 PU. 150m #12 AWG PVC, V_{DC}=650 V, IGBT rise time 50ns

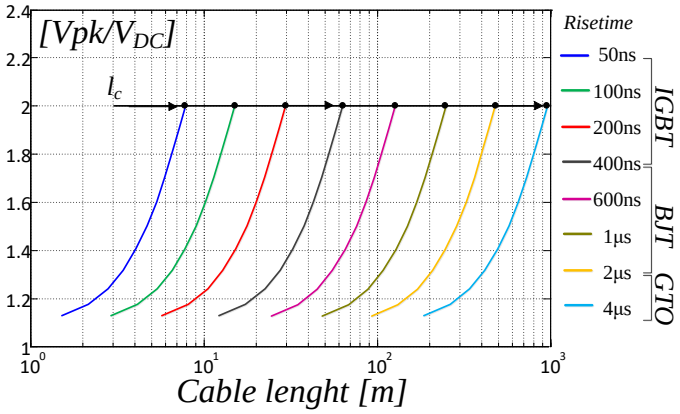


Fig. 3. 6 Critical cable length l_c: Motor Overvoltage <2 PU V.s. Cable length #12 AWG PVC and to varying rise time, V_{DC}=650 V.

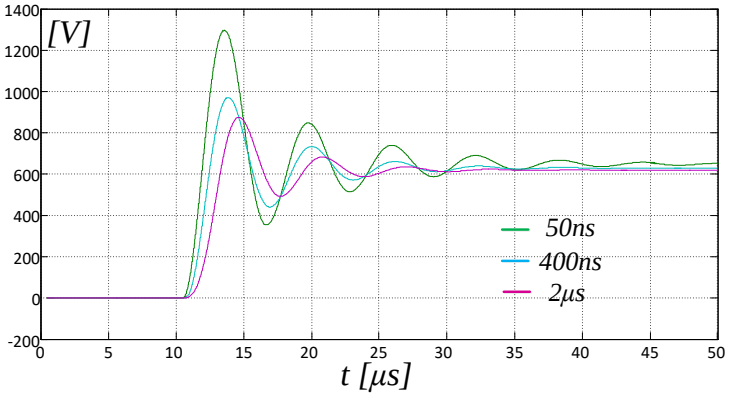


Fig. 3. 7 Motor Overvoltage V.s. Rise time: Cable 150m #12 AWG PVC, V_{DC}=650 V.

3.1.3 Motor overvoltages > 2 DC Bus voltage

When the reflected voltage is not fully decayed before the generation of the following pulse, the overvoltage can reach 2 or 3 times the DC-Bus voltage V_{DC} [10]. This happens because a residual trapped cable charge exists at the beginning of the voltage transient, Fig. 3. 8.

An overvoltage >2 pu has detrimental effects on expected lifetime of the motor isolation system [12]. Carrier switching frequency, modulation technique and cable oscillation frequency have a predominant effect on motor over-voltage in this case due to modulation pulses spacing. Moreover, the cable damping resistance determines how much residual charge is trapped on the cable before the next inverter pulse. According to eq. (3.18), the cable frequency f_0 is inversely proportional to cable length, as depicted in Fig. 3. 9 and Fig. 3. 10.

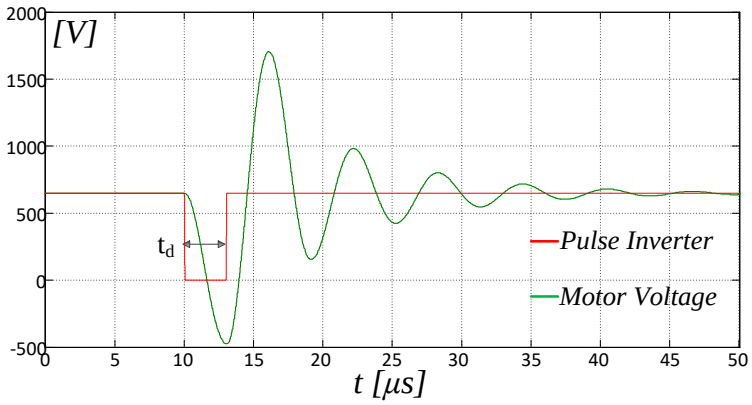


Fig. 3. 8 Motor Overvoltage >2 PU: Effects of Double Pulsing, 150m #12 AWG PVC, V_{DC}=650 V, IGBT rise/fall time 50ns

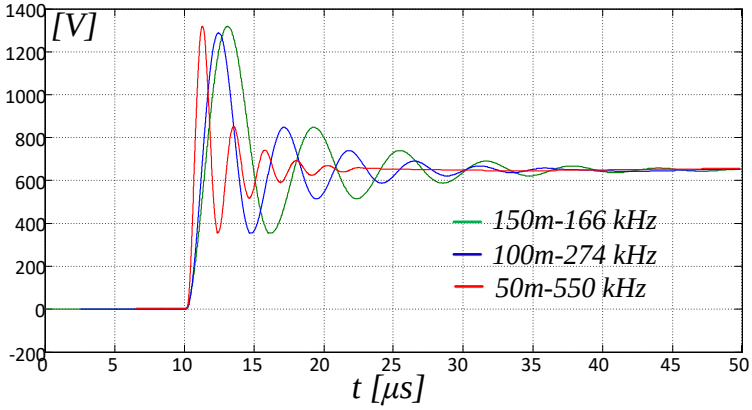


Fig. 3. 9 Motor Overvoltage VS Cable length. Cable #12 AWG, t_{rise}=50ns IGBTs, V_{DC}=650 V.

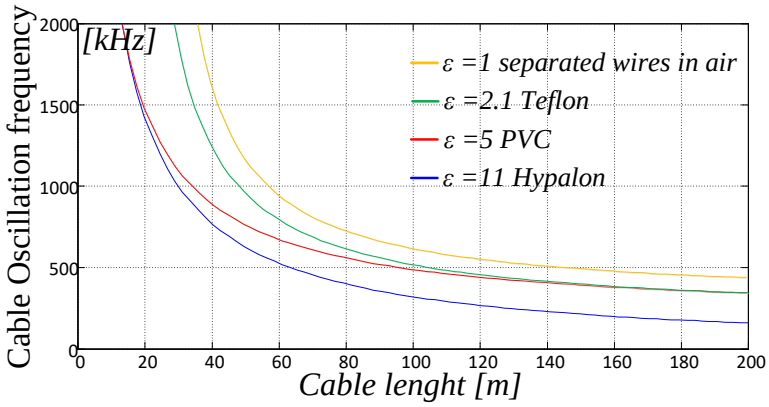


Fig. 3. 10 Cable Oscillation Frequency VS Cable length for different dielectric material. Cable #12 AWG, t_{rise}=50ns IGBTs, V_{DC}=650 V.

The matching between T_{cycle} and t_d is related with the damping time τ_d of reflected waves, that depends by the cable resistance, which in is in turn affected by skin ($K_{skin}(f0)$) and proximity (K_p) effects. The initial output inverter pulse V_0 is exponentially reduced to its final value V, as depicted in Fig. 3. 5, and depends only on cable parameters r_s, Z_0, $K_{skin}(f0)$, K_p and cable distance x travelled:

$$\frac{V}{V_0} = e^{-\left(r_s x/2Z_0\right)} = e^{-\left(K_P K_{skin} r_{dc} x/2Z_0\right)} = e^{-t/\tau_d} \tag{3.20}$$

being $\tau_d = 2L_0/r_s$. The exponential trend of motor voltage oscillation for 150m cable length is depicted in Fig. 3. 11, varying intentionally the cable resistance r_s:

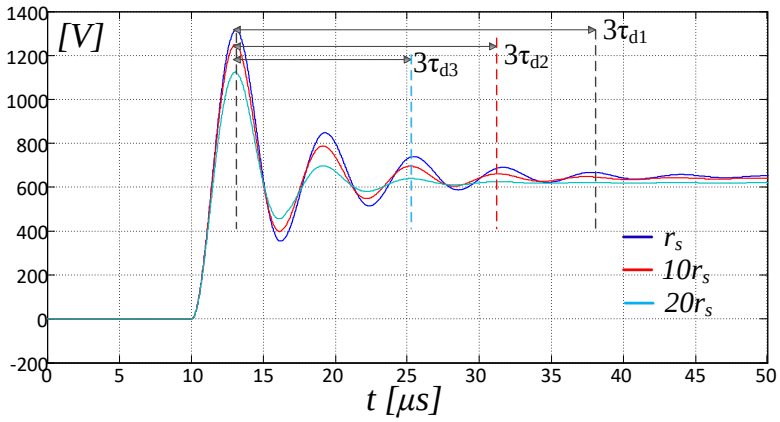


Fig. 3. 11 Damping time effect: cable 150 m #12 AWG PVC, V_{DC}=650 V, IGBT rise time 50ns, r_s=5.4 mΩ/m and Z_0=84Ω

Fig. 3. 12 shows typical $3\tau_d$ damping times. According to these diagrams skin effect has a large influence on damping the reflected wave. Furthermore, the shorter is the cable, the higher is the f_o and the faster is the damping effect caused by the cable resistance. If $t_d > 3\tau_d$, the motor terminal voltage decay before the arrival of the following voltage pulse, avoiding the double pulse effect. This prevents trapped line charge from causing a possible 3 pu overvoltage. Low power drives have a reflection coefficient close to one Γ_m=1 and small wire gauge, so that the predominant voltage decay mechanism is the cable resistance increment due to the skin effect. On the other hand, high power drives needs large cable diameters so they feature a reduced cable to motor reflection coefficient at Γ_m<0.9, while skin effect contribution to voltage decay is minimal, as shown in Fig. 3. 12. The breakpoint between the two different decay modes is somewhere around motor drives using #8 AVG wire.

Another phenomenon is known as *Polarity Reversal* [13]. This mode exposes a motor to tremendous overvoltage, similarly to the Double pulsing. Several factors contribute to the complex interaction of modulators and cables producing a polarity reversal. Major roles are played by carrier frequency, DC-Bus

voltage and modulation technique. Fig. 3. 13 shows a polarity reversal where the overvoltage reaches 2100 V, about 3 times V_{DC}. Polarity reversal occur when the modulating signals are transitioning into and out over-modulation or at the point of intersection of the two modulating waveforms [14], [15].

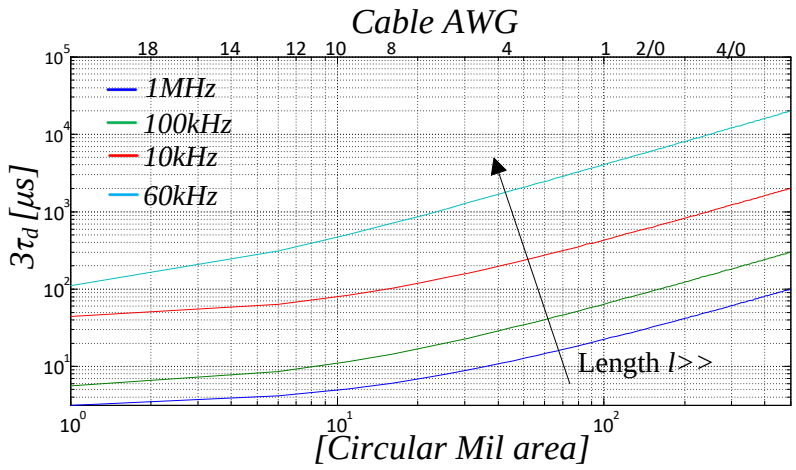


Fig. 3. 12 Damping of reflected wave for PVC bundled conductor cables

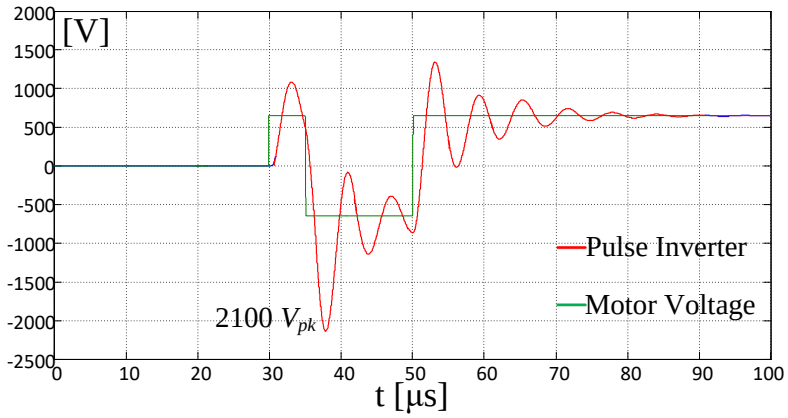


Fig. 3. 13 Motor Overvoltage >2 PU: Effects of Polarity reversal, 150m #12 AWG PVC, V_{DC}=650 V, IGBT rise/fall time 50ns

3.1.4 Overvoltage Mitigation Techniques based on additional passive networks

Effects of overvoltage phenomena can be reduced by acting on the rise/fall time of the voltage pulse, on the mismatch impedance and on the DC-Bus voltage value. Technical solutions able to reduce over-voltages at motor terminals have been widely investigated in prior art and a comprehensive research has been conducted on the modeling and analysis of these phenomena [13]-[21]. In particular, two type of overvoltage mitigation techniques are available: Additional Passive RLC networks and Active Methods which act on the switching modulation. Main passive filter topologies are depicted in Fig. 3. 14. Essentially, they act in two different

ways; the networks placed at the motor terminal act on the impedance matching between motor impedance and cable impedance, while the networks connected at the inverter output act on the rise time of the inverter output voltage. The aim of the first topologies is to obtain a reflection coefficient equal to zero while the goal of the second topologies is to increase the rise time of the inverter output voltage pulse.

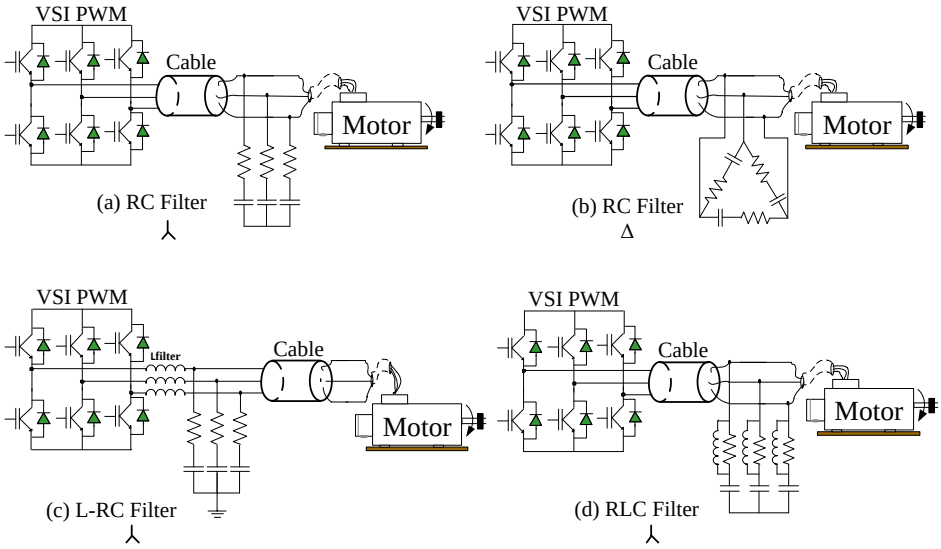


Fig. 3. 14. Passive filter topologies.

3.1.4.1 dv/dt Inverter Output Filters

In order to reduce the value of *dv/dt* at the inverter output, passive RLC filters have been proposed in [7], [22]-[29]. These filters are connected at one end at the inverter terminal and, at the other end, at the power cabl, Fig. 3. 14c. In [26] the authors propose an RL passive filter connected between the inverter output and a seven conductors symmetric cable in order to increase the rise/fall time of the inverter output voltage. Filter design requires a reasonable compromise between overvoltage mitigation and filter cost/volume. Fig. 3. 15 shows the RL network developed in [26] and Fig. 3. 16 shows the overvoltage mitigated. The passive filter acts on the *dv/dt* of the inverter output voltage, increasing the rise time which involves a reduction of peak overvoltage. Fig. 3. 17 shows the maximum overvoltage occurring at the motor terminals as a function of passive RL parameters. Furthermore, additional power losses have been measured resulting in 0.34-0.69% depending from cable length and filter parameters, Table 3.1.

Table. 3.1. Measured Power Losses with carrier frequency 7kHz

R_D	33Ω	47Ω
100 m (L_D= 30μH)	0.34%	0.38%
100 m (L_D = 70μH)	0.59%	0.69%

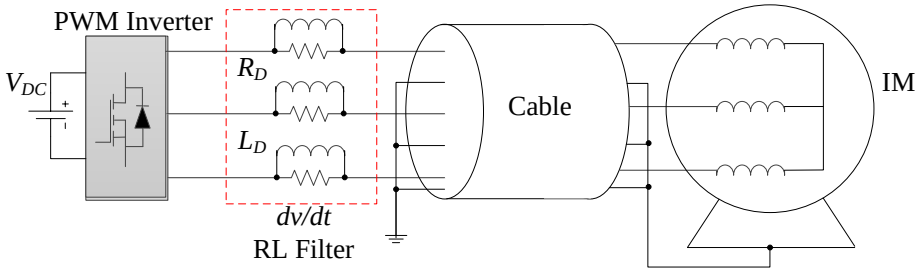


Fig. 3. 15. dv/dt RL series Passive filter proposed in [26]

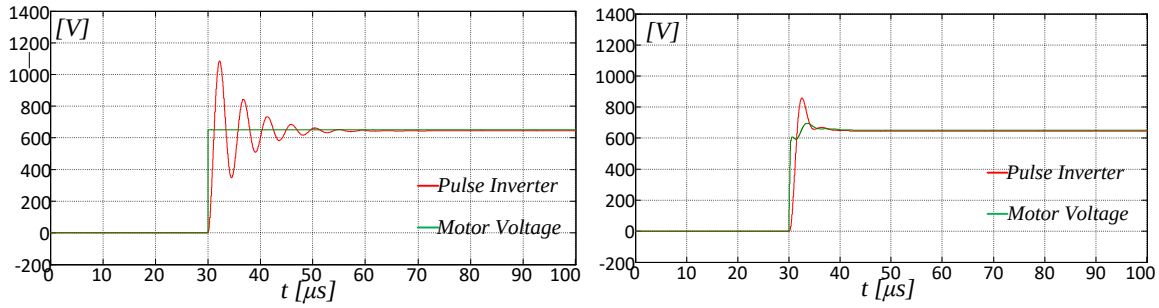


Fig. 3. 16. RL Passive filter on inverter output: Overvoltage occurs at the motor terminal where a 200 m of seven conductors symmetric cable is adopted (left). Overvoltage mitigated thank to RL filter, R_D=33Ω, L_D=150μH (right)

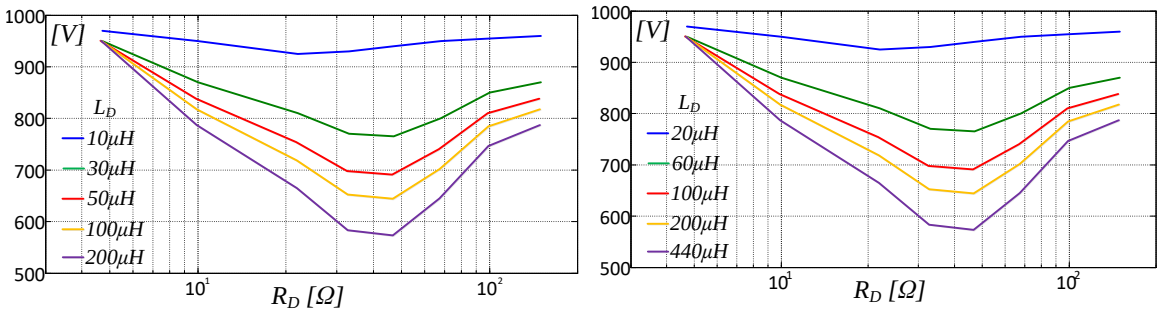


Fig. 3. 17. Max overvoltage with RL Passive filter as a function of filter parameters R_D and L_D and rise time equal to 0.18 *μs: 100 m of cable(left), 200 m of cable(right).*

In [22] a passive filter to mitigate *dv/dt* effects on motor overvoltage is presented. The passive filter consists of three inductors connected in series between the inverter output and the cable and two RC networks connected through two diodes, as depicted in Fig. 3. 18. It reduces both common-mode and differential-mode components. Lower power losses are measured (0.28%), compared with [26], however, the additional RLC networks lead for extra passive components which mean a higher cost.

Another filter has been proposed in [25]. It consists of a LC network, with the capacitor star point clamped to the DC link by mean of two diodes, Fig. 3. 19. When due to an overshoot the voltage between the star point of the capacitors and one of the DC bus rails becomes bigger than $\pm V_{DC}/2$ one of the two diodes turns

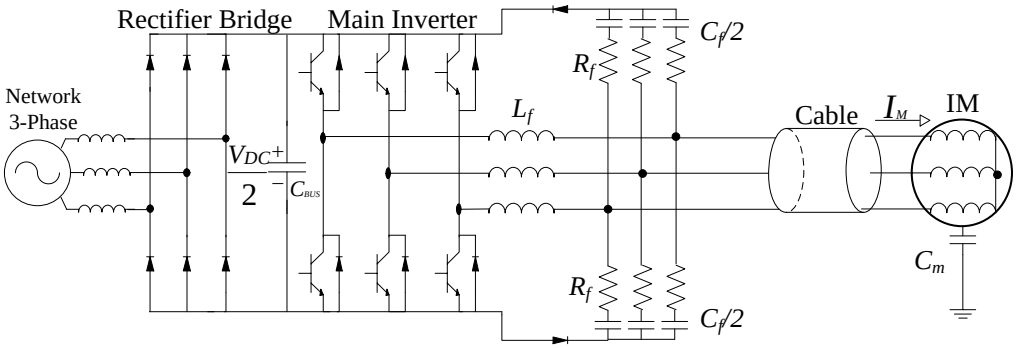


Fig. 3. 18. dv/dt RLC Passive filter proposed in [22]

on, clamping the voltage. The LC filter with differential mode inductors, depicted in Fig. 3. 20, is a widely used output filter topology, where the star point of the capacitors is left floating. This topology, adopted in many commercially available filters, is very simple and relatively cheap. However, some motor over voltages may still occur. The circuit shown in Fig. 3. 21 is aimed to reduce the common-mode voltage. It has two disadvantages; first, it needs a connection to the midpoint of the DC link capacitors, which is not always accessible on commercial inverters, secondly, power losses are about 0.8%.

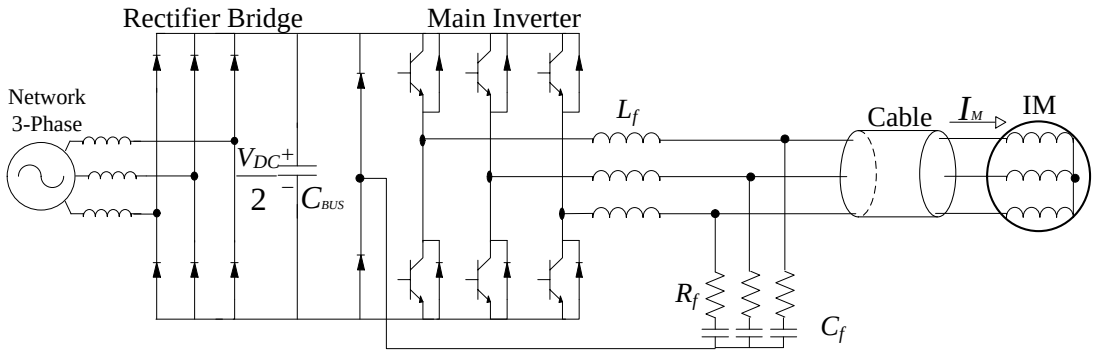


Fig. 3. 19. dv/dt RLC Passive filter proposed in [25]

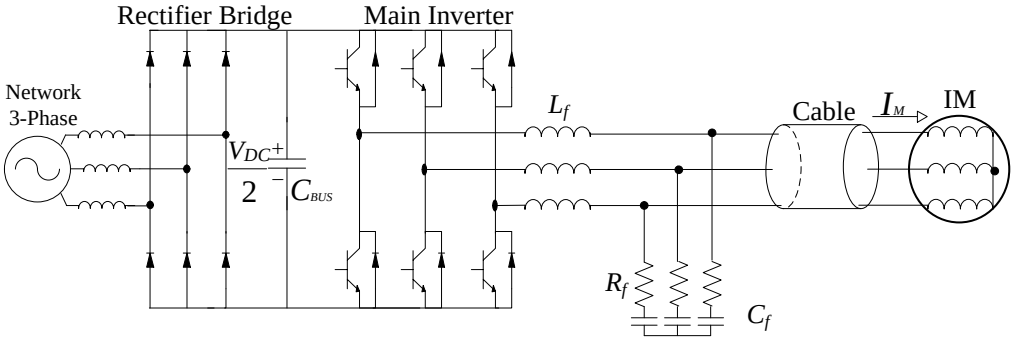


Fig. 3. 20. dv/dt LC Passive filter with star point of the capacitor left floating [25]

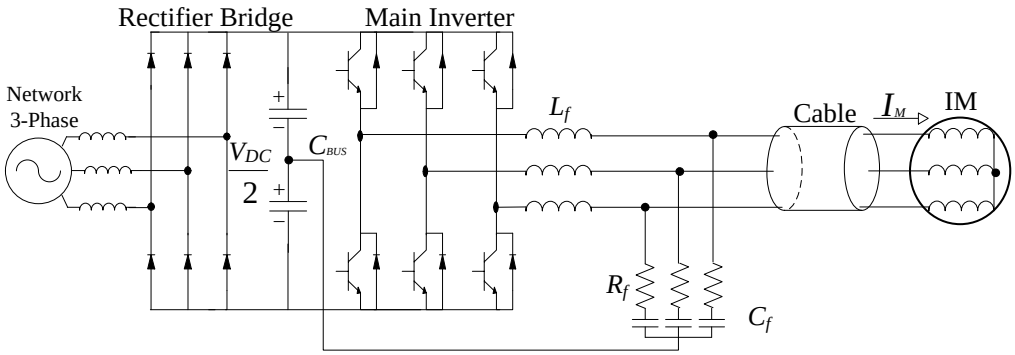


Fig. 3. 21. dv/dt LC Passive filter with star point of the capacitor connect to the middle of the Bus DC voltage [25]

A new *dv/dt* filter is proposed in [28], Fig. 3. 22 to be used on low-power AC drives. This topology is a modified version of RL network proposed in [22] but it is able to mitigate both common and differential mode components.

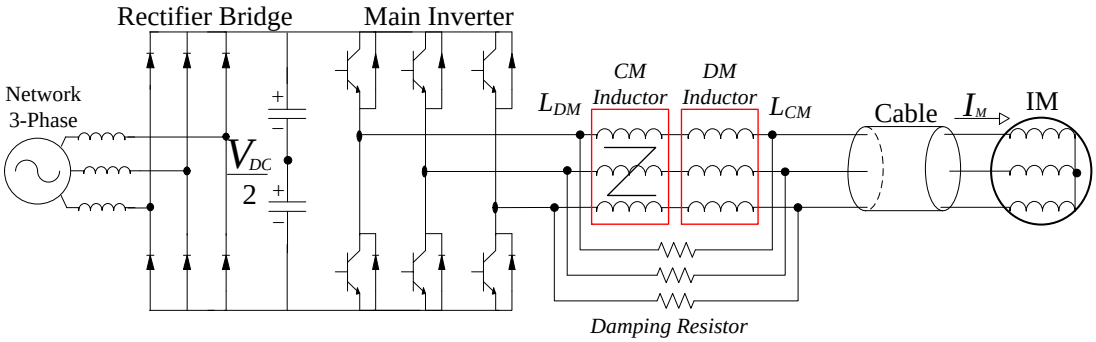


Fig. 3. 22. dv/dt RL differential and common-mode filter proposed in [28]

A further passive LC filter able to limit the rate of rise/fall time of the inverter output voltage is proposed in [23] and depicted in Fig. 3. 23. In typical application where *dv/dt* is limited to 100-500 V/µs, the resonant frequency of the filter is above the switching frequency. A diode bridge must therefore be used to clamp the resonant voltage. Resistors are used to dissipate the energy stored in the resonant circuit. Additional filter losses are around 0.6% of the rated power.

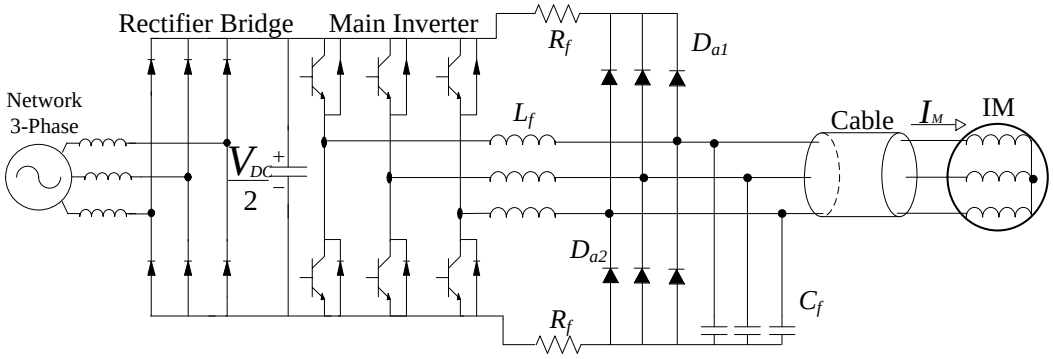


Fig. 3. 23. dv/dt RLC Passive filter proposed in [23]

3.1.4.2 Passive Filters at the Motor terminals

RLC networks placed at the motor terminals in order to mitigate the motor voltage overshoots are known as Line Terminator Networks (LTN). Differently from *dv/dt* networks, these passive filters act on the impedance mismatch between the motor impedance and the surge impedance of the cable.

The main goal is that to mitigate the reflected voltage at the motor terminals, modifying the motor impedance Z_m seen from the cable side, in order to obtain unitary reflection coefficient Γ_m. Operating principles of LTN networks are explained in [7]. Three surge impedance terminators and their losses are discussed. The simplest LTN consists of set of shunt resistors placed in parallel at the motor terminals, Fig. 3. 24. The shunt resistance R_f is selected as:

$$R_f \cong \sqrt{\frac{L}{C}} = Z_0 \tag{3.21}$$

being L and C the inductance per unit length and the capacitance per unit length of the cable, respectively.

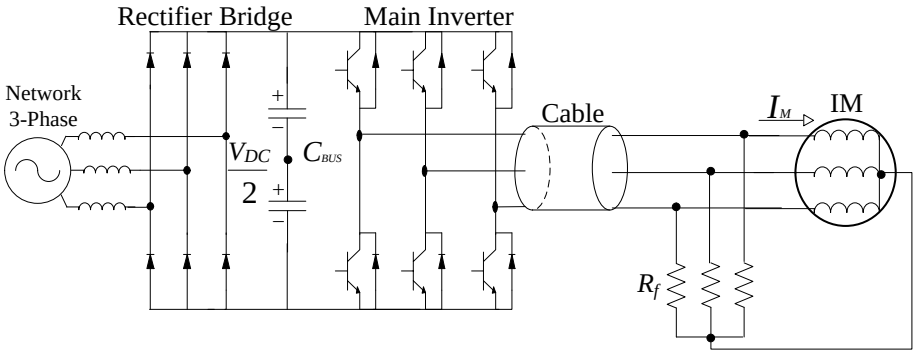


Fig. 3. 24. LTN Parallel resistor terminator proposed in [7]

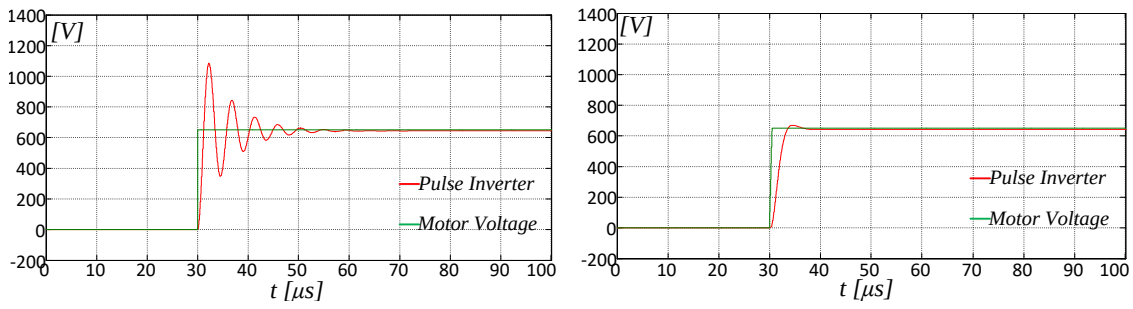


Fig. 3. 25. Parallel Resistor Terminator Passive filter: Overvoltage occurs at the motor terminal where a 200 m of seven conductors symmetric cable is adopted (left). Overvoltage mitigated thank to parallel R filter, R_f=85Ω= Z_0 (right)

Although effective in suppressing the motor overvoltage as shown in Fig. 3. 25, this method is rarely used due to excessive power losses.

A second approach exploits a first-order RC filter to match the surge impedance of the cable and provide the proper level of overvoltage damping, Fig. 3. 26. Each capacitor C_f appears as a short circuit during the rising of the voltage pulse and as an open circuit when it is charged.

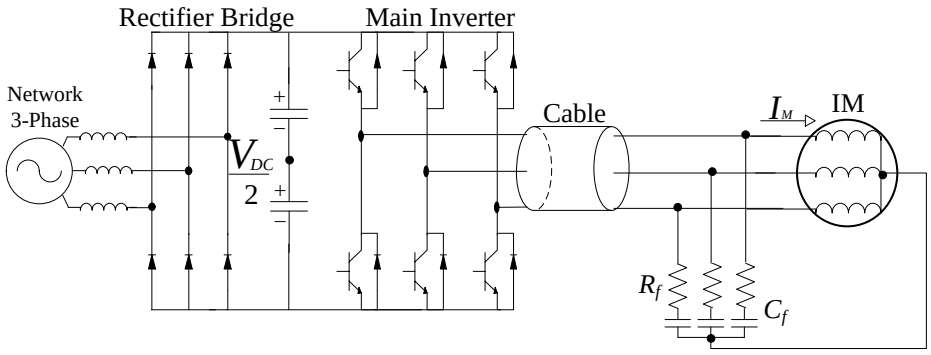


Fig. 3. 26. LTN first-order filter proposed in [7]

The equivalent impedance Z_{eq} of the first-order filter closely matches the cable surge impedance Z_0:

$$Z_{eq} \cong \sqrt{R_f^2 + \left(\frac{1}{j\,\omega_f\,C_f}\right)^2} \cong \sqrt{\frac{L}{C}} = Z_0 \tag{3.22}$$

Thus, the resistance R_f is selected in order to realize an overdamped circuit as:

$$R_f \geq \sqrt{\frac{4L}{C_f}} \tag{3.23}$$

The use of a nonlinear capacitor may further optimize the losses.

A third kind of LTN terminator consists of a second-order filter as depicted in Fig. 3. 27.

The equivalent impedance Z_{eq} of the filter is given by:

$$Z_{eq} \cong \sqrt{\left(\frac{R_f\,\omega_f^2\,L_f^2}{R_f^2 + \omega_f^2\,L_f^2}\right)^2 + \left(\frac{R_f^2\,\omega_f\,L_f}{R_f^2 + \omega_f^2\,L_f^2} - \frac{1}{\omega_f\,C_f}\right)^2} \cong \sqrt{\frac{L}{C}} = Z_0 \tag{3.24}$$

Also in this case, the resistor R_f is designed to result in an overdamped circuit:

$$R_f \leq \frac{\sqrt{L_f\,C_f}}{2\,C_f} \tag{3.25}$$

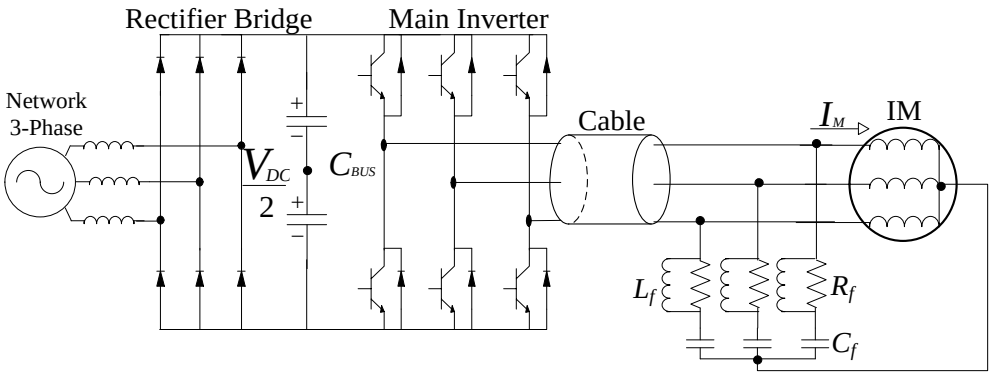


Fig. 3. 27. LTN second-order filter proposed in [7]

The resonant frequency of the filter should be at least five times larger than the switching frequency of the inverter. In order to minimize the voltage overshoot the filter operating frequency must as close as possible to the resonant frequency of the filter. Filter components are generally selected in order to minimize the filter losses.

Table 3.2 shows the power losses of the three considered LTN in the same operating conditions. According to these results it is apparent that LTN are less efficient than *dv/dt* inverter output filters.

Table. 3.2. Power Losses with carrier frequency 7kHz, 100 m of 14 AWG cable

Filter Components	Parallel Resistor	First-order RC	Second-order RLC
R	190Ω	30Ω	32Ω
L		33nF	33nF
C			3.2mH
Tot. Losses	29%	3.9%	4.2%

A delta connected LTN is proposed in [30] and depicted in Fig. 3. 28. Unlike [7] R_f is set to Z_0, while C_f is selected on the basis of inverter pulse rise time, pulse spacing, allowable motor voltage and power losses. Initially, the inverter output voltage is zero and the capacitor is discharged. When a traveling wave arrives at the motor terminals, the RC network charges at V_{DC}.

A design goal is to make the voltage across C_f lower than 10% V_{DC} at the end of t_{rise}. The capacitor voltage V_{cf} is:

$$V_{cf} = 0.1 V_{DC} = V_{DC}\left(1 - e^{-t_{rise}/(R_f C_f)}\right) \tag{3.26}$$

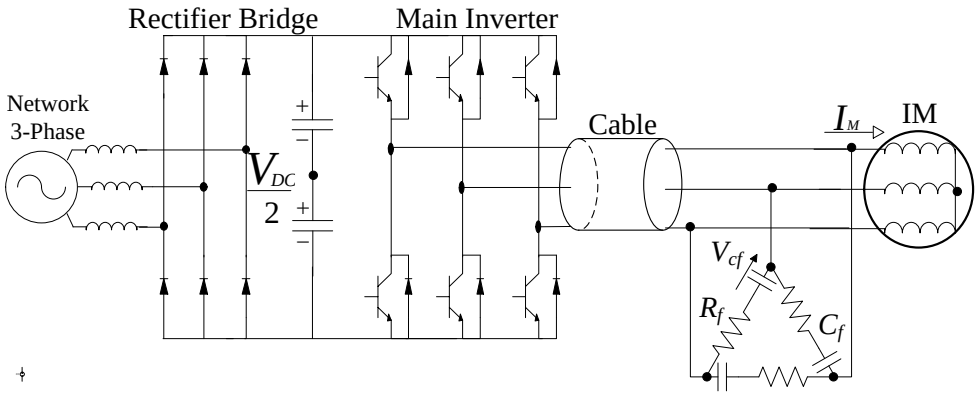


Fig. 3. 28. Delta connection LTN first-order filter proposed in [30]

Hence C_f is given by:

$$C_f = -\frac{\ln(0.9) R_f}{t_{rise}} \tag{3.27}$$

Another constraint on C_f is to obtain $3\tau_d = 3R_f C_f$ shorter than the inverter dwell time t_d, to fully discharge the capacitor before the generation of the following pulse. Power losses on a system featuring a 100 m #14 AWG cable and C_f =10nF, are around 0.15% of the rated power, rising to 0.68% for a 200 m of #14 AWG cable and a 47nF C_f. An active low-loss motor terminal filter for overvoltage mitigation and common-mode current reduction is proposed in [9]. A LTN design is generally dependent from length and parameters of the cable connecting the inverter with the motor, while, according to the proposed approach, the rise time of the voltage pulses at the motor terminal is reduced for any cable length. It consists of three RLC filters connected between the cable and the motor, and of an additional parallel connected RC active network, Fig. 3. 29. The active filter features eight operating modes, Fig. 3. 30.

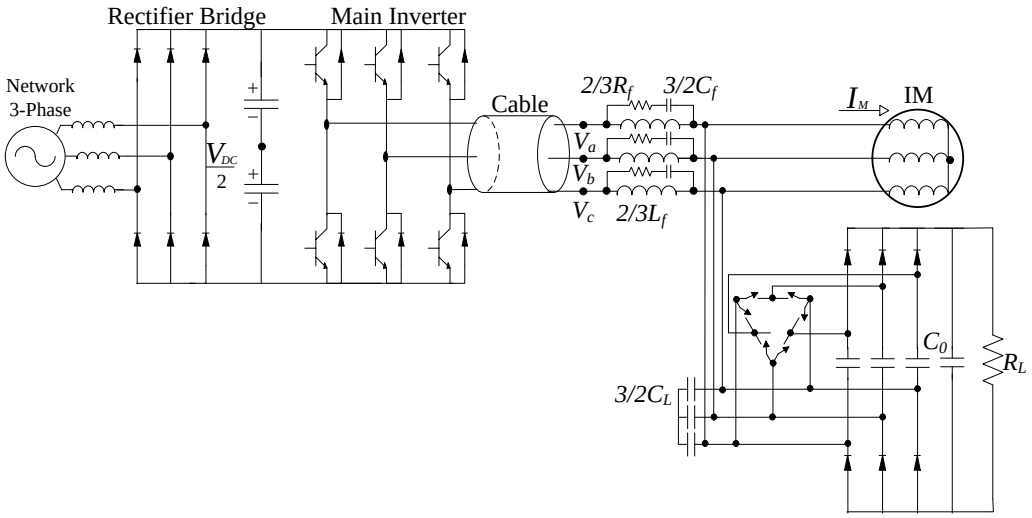


Fig. 3. 29 Active low-loss LTN

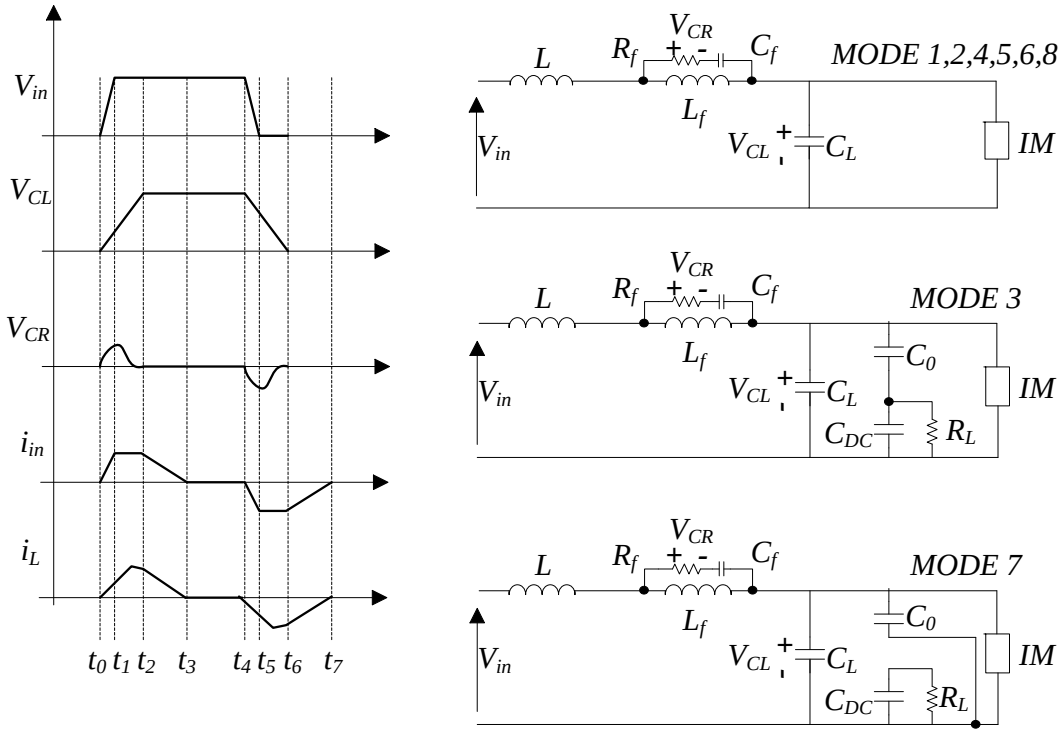


Fig. 3. 30 Circuit operation of Active low-loss LTN: Mode 1[t_0-t_1], Mode 2[t_1-t_2], Mode 4[t_3-t_4], Mode 5[t_4-t_5], Mode 6[t_5-t_6], Mode 8[t_7-t_8], Mode 3[t_2-t_3], Mode 7[t_6-t_7]

Fig. 3. 31 shows the power losses versus the motor terminal voltage for three different filters. With the same voltage overshoot, the power losses of the proposed filters are the lowest among the three filters. The proposed filter is very efficient, moreover, L_f is independent from the cable length, but the large amount of extra components, lead to additional cost and weight.

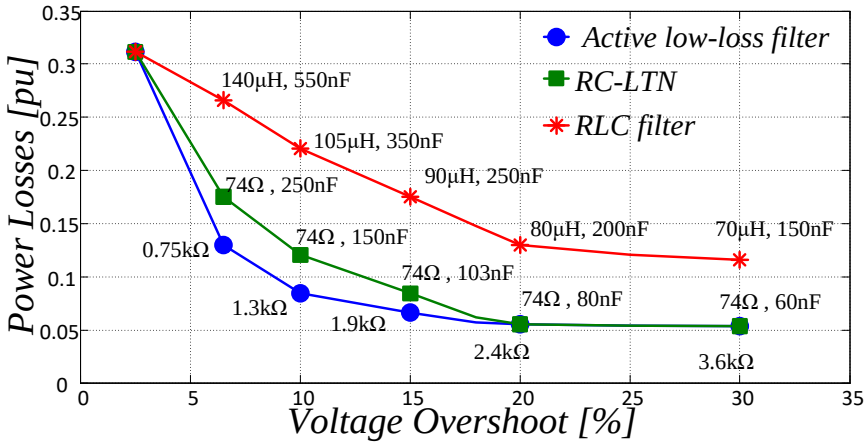


Fig. 3. 31 Filter losses versus motor voltage mitigated for various filter netwiorks:3/2C_f=7nF, 2/3L_f=25µH and 3/2C_L=15nF, 100 m of cable length and 10kHz switching frequency.

3.1.4.3 Comparison between LTN and Inverter output filters

RLC networks at the motor terminals, RC networks at the motor terminals and RLC networks at the inverter output are discussed and compared in [27],[32]. RLC filter placed at the inverter output shows the best combination among overvoltage amplitude, power losses, common-mode current amplitude and voltage distribution in the machine stator winding. The first step in designing an RLC filter at the motor terminals is to determine the filter resistance, [7] in order to match the surge impedance of the cable and the motor impedance. Effects of the capacitor selection in terms of motor voltage and power losses are shown in Fig. 3. 32(left). In order to achieve the best results it is very important to properly pair the inductance with the capacitance [31], exploiting the diagrams shown in Fig. 3. 32(right). RLC filter power losses and motor voltage are shown in Fig. 3. 33(left). The filter resistance is set in order to match the cable characteristic impedance, while optimal pairs of L_f and C_f can be deducted from Fig. 3. 33(left).

The inductance of an RLC filter at inverter output is remarkably lower than the inductance of a RLC filter at the motor terminals.

The selection of the filter type is accomplished on the basis of an analysis of, power losses, common-mode currents circulating in the drive and the voltage distribution along the machine winding. Fig. 3. 34 shows the power losses as a function of the filter capacitance for the three considered filter topologies. A proper choice of the inverter switching frequency may reduce the filter losses. Fig. 3. 35 shows the motor voltage waveform obtained with the considered filters. The best response, in terms of overvoltage reduction, is obtained with the RC filter, but the common-mode current amplitude is higher than that obtained with the RLC inverter output filter.

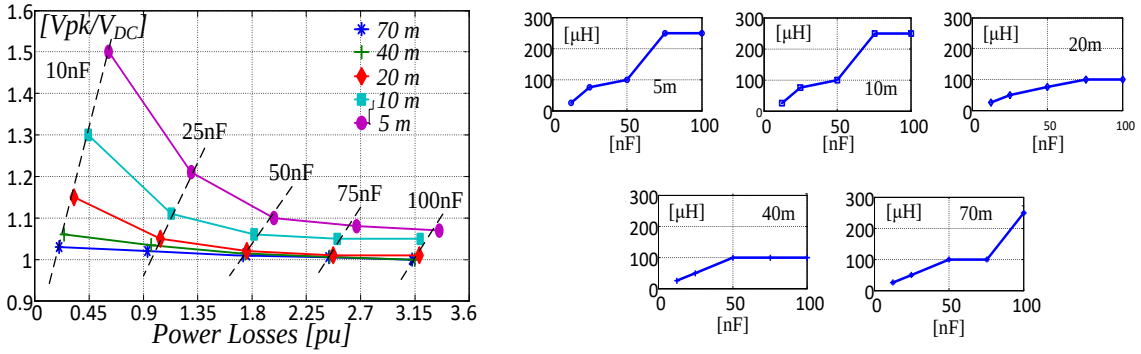


Fig. 3. 32. RLC filter at motor terminals in star connection, 3hp motor: Minimum peak motor voltage Vs Power losses for various number of filter capacitance (left), Suggested pairs for filter inductance L_f and capacitance C_f for various length of cable(right).

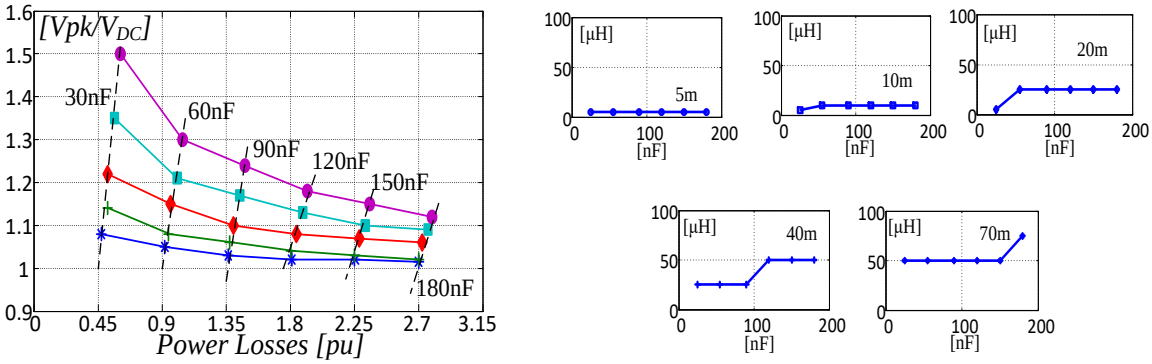


Fig. 3. 33. RLC filter at the inverter output in star connection, 3hp motor: Minimum peak motor voltage Vs Power losses for various number of filter capacitance (left), Suggested pairs for filter inductance L_f and capacitance C_f for various length of cable(right).

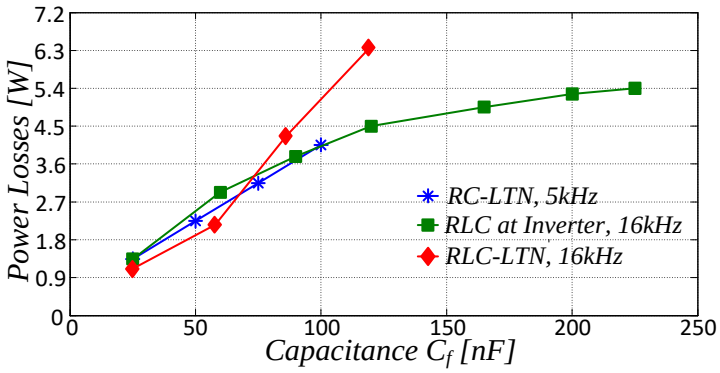


Fig. 3. 34. Filter losses versus filter capacitance, 3hp motor for discussed filter topologies

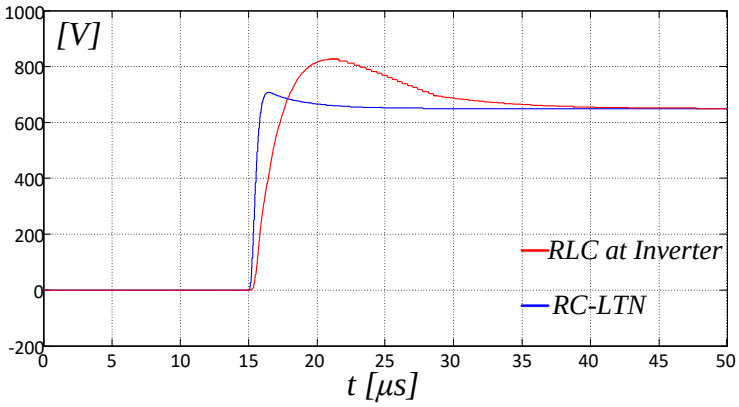


Fig. 3. 35. Motor overvoltage for RLC filter at inverter output and RC filter at the motor terminals, 3hp motor, 70 m of #14 AWG cable.

In conclusion, operating at the highest inverter switching frequency the RLC filters have lower power losses in comparison to the RC filters. The switching frequency is determined by the process requirements and the inverter constraints. From Fig. 3. 34, comes that the RLC filter at the inverter output features the lowest power losses. The RC filter at the motor terminals shows the best waveforms, but it is not able to reduce the high

dv/dt, hence, it is not able to prevent the internal reflections and features higher common-mode currents. The RLC filter decreases the *dv/dt* voltage pulse rate, which may reduce the amplitude of the associated common-mode currents. Therefore, the RLC network at the inverter output is indeed the most interesting solution to mitigate the motor overvoltage adjustable-speed drives with long power cables.

3.1.5 Active Overvoltage Mitigation Techniques

An active overvoltage mitigation approach is described in [8], where a new inverter topology is proposed featuring six additional power devices, Fig. 3. 36.

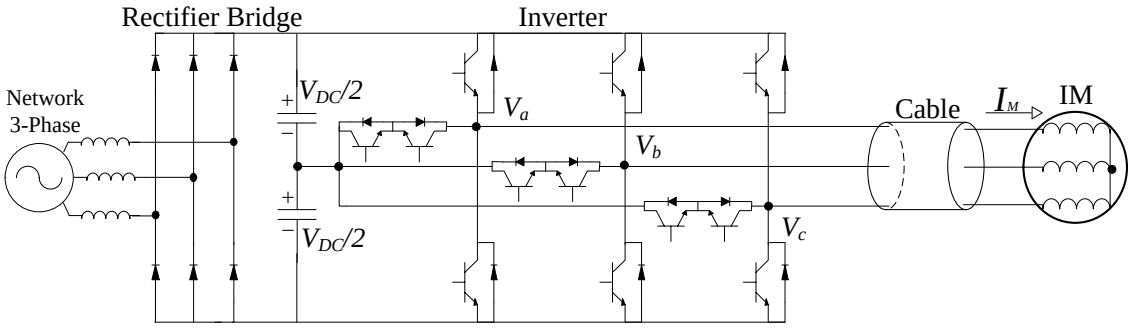


Fig. 3. 36. Inverter structure proposed in [8].

According to the proposed approach the inverter output voltage is clamped at $V_{DC}/2$ during each voltage transition for a time β. Reflected voltages at the motor terminals are cancelled by controlling β. Optimal cancellation is achieved if β is made equal to twice the transport delay τ of the cable, as depicted in Fig. 3. 37.

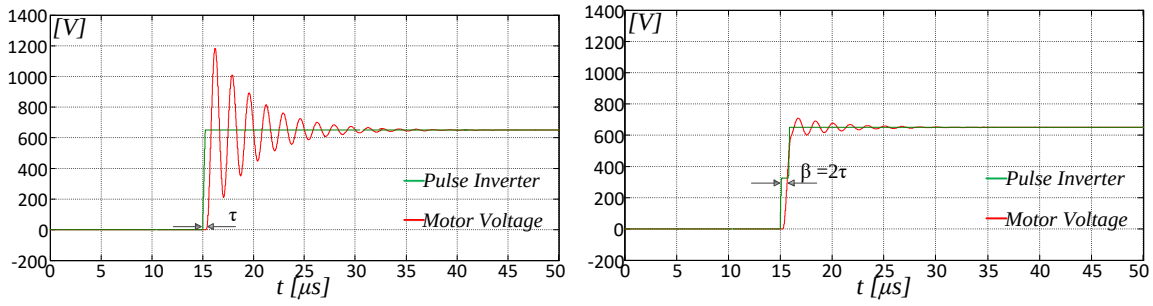


Fig. 3. 37 Overvoltage mitigation method in [8]: Motor voltage without mitigation method(left). Motor voltage with active overvoltage mitigation method(right). 100 m of #14 AWG cable

According to the Laplace transformation, the *a*-phase output voltage of the inverter V_a (at position $x=0$) can be written as a sum of two voltage signals of equal magnitude $V_{DC}/2$ and delayed by β:

$$V_a(0,s) = U_a(0,s) + U_a(0,s)e^{-2\beta s} \tag{3.28}$$

where $U(l,s)=V_{DC}/2$. Fig. 3. 38 shows the two voltage components delayed by β.

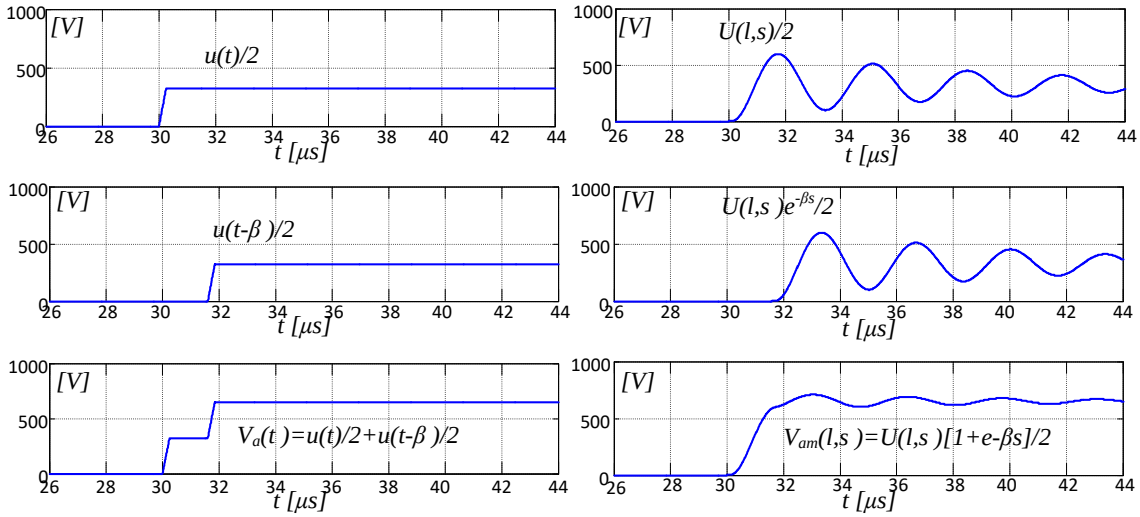


Fig. 3. 38 Voltage decomposition of the inverter output voltages(left) and their resulting voltages at the motor terminals(right)

Exploiting eq. (3.14) and eq. (15) shown in section 3.1.1, the *a*-phase voltage at the motor terminals V_{am} is given by:

$$V_{am}(l,s) = \frac{1+\Gamma_m}{2} \mathrm{U(l,s)} \left[e^{-\tau s} + e^{-(\tau+\beta)s} + \Gamma_m\Gamma_G e^{-3\tau s} + \Gamma_m\Gamma_G e^{-(3\tau+\beta)s} + \Gamma_m{}^2\Gamma_G{}^2 e^{-5\tau s} + \ldots\ldots \right] \tag{3.29}$$

From eq. (3.29), comes that in order to eliminate the reflected voltages, the duration β of $V_{DC}/2$ must be set as twice the transport delay τ of the cable. Thus, replacing $\beta=2\tau$ into eq. (3.29), the *a*-phase voltage at the motor terminals V_{am} becomes:

$$V_{am}(l,s) = \frac{1+\Gamma_m}{2} \mathrm{V_{DC}} \left[e^{-\tau s} + \frac{(1+\Gamma_m\Gamma_G)e^{-3\tau s}}{1-\Gamma_m\Gamma_G e^{-2\tau s}} \right] \tag{3.30}$$

Taking into account that $\Gamma_G \approx -1$ and, $\Gamma_m \approx 1$, the second term in eq. (29) becomes:

$$\frac{(1+\Gamma_m\Gamma_G)e^{-3\tau s}}{1-\Gamma_m\Gamma_G e^{-2\tau s}} \cong 0 \tag{3.31}$$

This means that if β is chosen to be 2τ, almost no voltage overshoot takes place. Hence, the motor terminal voltage is given by:

$$V_{am}(l,s) = V_{DC} e^{-\tau s} \tag{3.32}$$

According to eq. (32), no reflected voltages take place. The overvoltage mitigation can be estimated as:

$$\frac{\Gamma_G \Gamma_m^{\,2} + (2 + \Gamma_G)\Gamma_m}{2} \times 100 \tag{3.33}$$

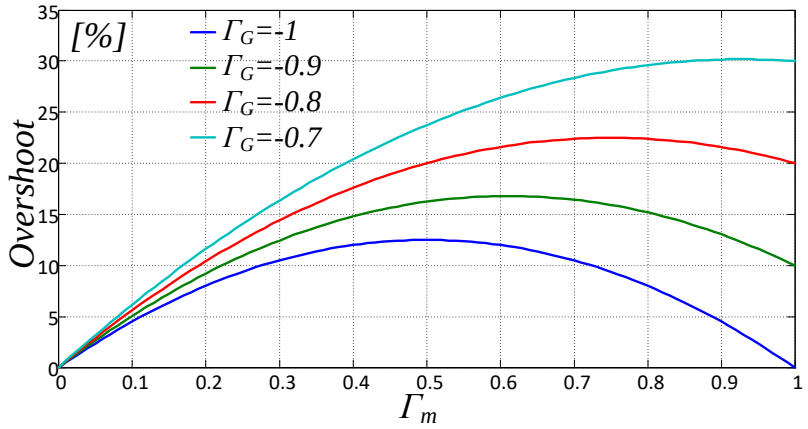


Fig. 3. 39 Percentage overshoot voltage level at the motor terminals for various reflection coefficient Γ_m and Γ_G with $\beta=2\tau$.

Fig. 3. 39 demonstrates that the voltage overshoot at the motor terminals can be attenuated below 15% in most cases.

The method uses additional IGBT devices leading to extra power losses, which, however, are lower than those generated by RLC filters. Moreover, it needs an estimation of the cable transport delay time τ. This can be accomplished on the basis of the length and the characteristic impedance of the cable. Hence, it may be difficult to obtain an accurate transport delay time estimation in many practical cases. Alternatively, it is possible to experimentally adjust the pulse duration of the auxiliary switches until the overvoltage is minimized. These issues are overcome in [33] where the author exploits the same inverter topology adopted in [8], Fig. 3. 36. In addition, an adaptive parameter identification system is developed. This adaptive algorithm determines unknown parameters such as Γ_m and Γ_G in order to perfectly suppress the overvoltage at the motor terminals. Analytically, the transfer function of eq. (2.29) is given by:

$$H(s) = \frac{(1+\Gamma_m)(1-\Gamma_G)}{2}\left[e^{-\tau s} + e^{-(\tau+\beta)s} + \Gamma_m\Gamma_G e^{-3\tau s} + \Gamma_m\Gamma_G e^{-(3\tau+\beta)s} + \Gamma_m^{\,2}\Gamma_G^{\,2} e^{-5\tau s} + \ldots\ldots\right] \tag{3.34}$$

By introducing a new input voltage $V(s)(1+e^{-2\tau s})$ in H(s), the motor voltage becomes:

$$\frac{1+e^{-\tau s}}{2} H(s) = \frac{(1+\Gamma_m)(1-\Gamma_G)}{4}\left[e^{-\tau s} + \left(1+\Gamma_m\Gamma_G\right)e^{-3\tau s} + \Gamma_m\Gamma_G\left(1+\Gamma_m\Gamma_G\right)e^{-5\tau s} + \ldots\ldots\right] \tag{3.35}$$

The percent overvoltage mitigation is given by:

$$\frac{(1+\Gamma_m)(1-\Gamma_G) + (2+\Gamma_G\Gamma_m) - 4}{4} \times 100 \tag{3.36}$$

Compared to the conventional system described in [8] the corrective term introduced in eq. (34) effectively reduces the overshoot at the motor terminals, as depicted in Fig. 3. 40.

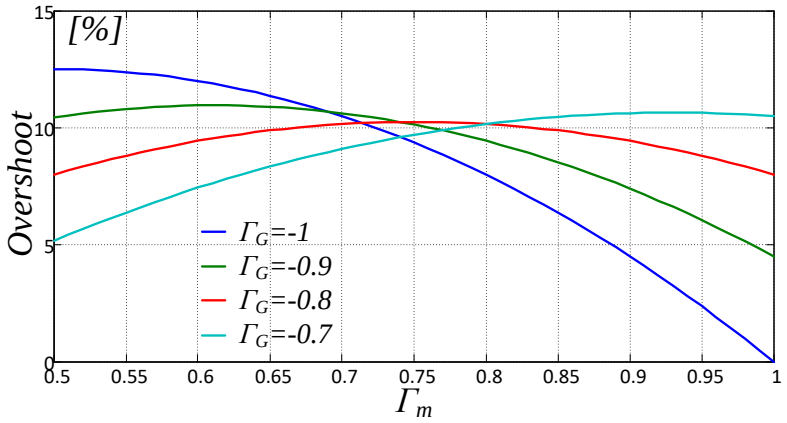


Fig. 3. 40 Percentage overshoot voltage level at the motor terminals for various reflection coefficient Γ_m with suppression scheme proposed in [33].

The control algorithm automatically compares the reference output voltage of the PWM controller $V(t)^*$ with the voltage detected at the motor terminals $V_m(t)$ and generates an output corrective voltage term $V_{corr}(t)$. This is multiplied for the power devices driving signals, in order to calculate the reflection coefficients of the system, Fig. 3. 41.

The adaptive parameter identification is effective only if reflection coefficients are real numbers. Thus, a full oscillation cancellation may not be achieved if reflection coefficients are complex numbers. However, the voltage overshoot at the motor terminals is anyway reduced [8].

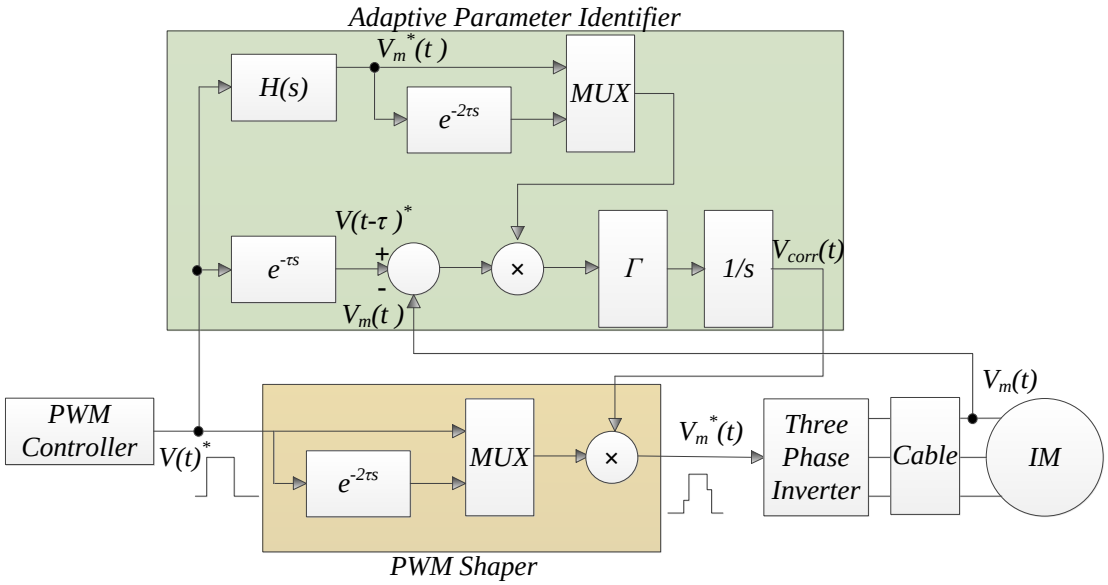


Fig. 3. 41 Adaptive parameter identifier block diagram

A further active method to adjust the PWM pulse pattern in the pulse dropping region is proposed in [10]. It has been shown that if the reflected voltage is not fully decayed before the generation of the following pulse, the magnitude of over-voltage can reach 2 or 3 pu. In this case, the system is working in pulse dropping region. Furthermore, when the modulating signals are transitioning into and out over-modulation or at the point of intersection of the two modulating waveforms [14], [15], a polarity reversal occurs. Fig. 3. 42(left) shows a PWM voltage pulse pattern with pulse dropping and polarity reversal. The resultant motor overvoltage is shown in Fig. 3. 43. To prevent this phenomenon, commonly referred to as double pulsing, the inverter PWM pulse pattern is adjusted to include a certain minimum dwell time t_d and polarity reverse time t_{pi} between switching transitions as shown in Fig. 3. 42(right). The minimum t_d is chosen to limit the motor overvoltage well below the winding insulation voltage rating, up to a certain maximum cable length. The minimum polarity reversal time t_{pi} is set to be equal to the minimum dwell time.

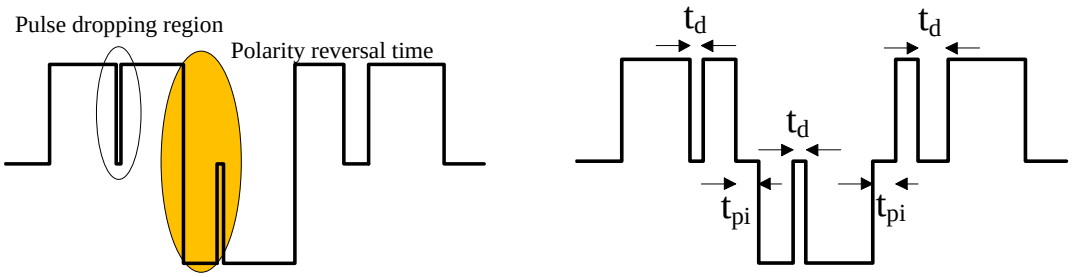


Fig. 3. 42 PWM voltage pulse pattern with pulse dropping region t_d and polarity reversal time t_{pi}

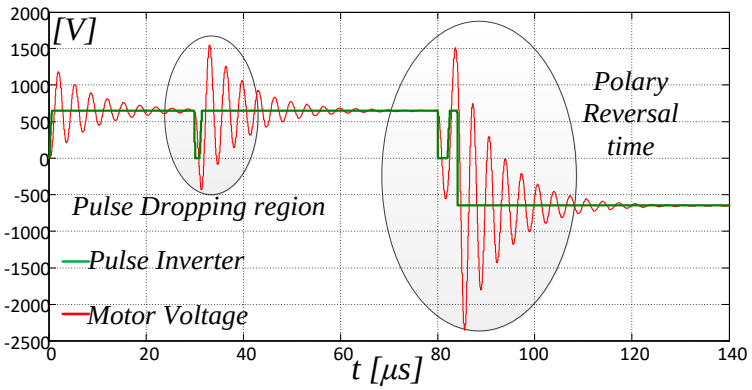


Fig. 3. 43 Motor voltage in dropping region t_d and polarity reversal time t_{pi}

Enforcement of minimum t_d and polarity reversal t_{pi} generates a distortion of the voltage waveforms, especially at high PWM carrier frequencies. To avoid DC offsets and volt-second imbalance, the error in duty cycles must be compensated in the following PWM periods. The method practically limits minimum and maximum values of power switch duty cycle in the linear PWM region, as shown in Fig. 3. 44. When the duty cycle exceeds these limits, pulse dropping occurs. Such a pulse pattern adjustment distorts the motor voltage, hence, a suitable compensation is required to ensure volt-second balance and to prevent DC offsets.

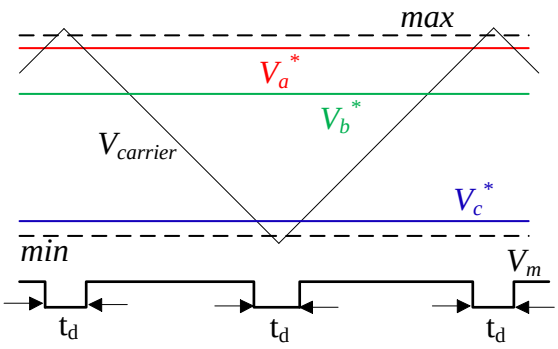


Fig. 3. 44 Method to enforce minimum dwell time and polarity reversal time in the PWM pulse pattern by limiting the minimum and the maximum duty cycles

It has already said in section 3.1.3, that the period of oscillation T_{osc} of the motor voltage is a function of the cable length. To prevent double pulsing the minimum dwell time must be chosen to be 2-3 times greater than the oscillation period.

Denoting the minimum dwell time T_{dwell} and the PWM period as $T_{PWM,}$ maximum and minimum values of the duty cycle must be set as follows:

$$\begin{aligned} \varepsilon &= \frac{T_{dwell}}{T_{PWM}} \\ \max &= 1-\varepsilon \\ \min &= \varepsilon \end{aligned} \tag{3.37}$$

When the instantaneous duty cycle falls outside of these limits, it is clamped to 0 or 1. The resulting error in the duty cycle is accumulated and compensated in the following PWM periods. From Fig. 3. 45(left), comes that if 1.5 T_{osc} =0.5T_{dwell} or 2.5 T_{osc}=0.5 $T_{dwell,,}$ then the peak motor voltage exceeds 2 $V_{DC.}$. Moreover, Fig. 3. 45(right) shows that a voltage in excess of 2 V_{DC} can occur if T_{osc} =0.5T_{dwell} or 2 T_{osc}=0.5 $T_{dwell,.}$ Fig. 3. 46 shows the effectiveness of the proposed method in mitigating the motor overvoltage.

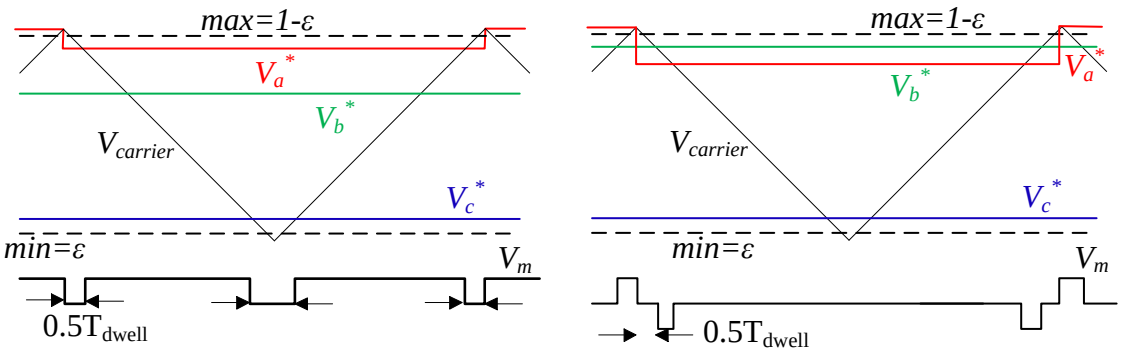


Fig. 3. 45 Reduction in dwell time in the motor voltage during transition to/from the pulse dropping mode(left), Reduction in polarity reversal time during transition to/from the pulse dropping mode(right)

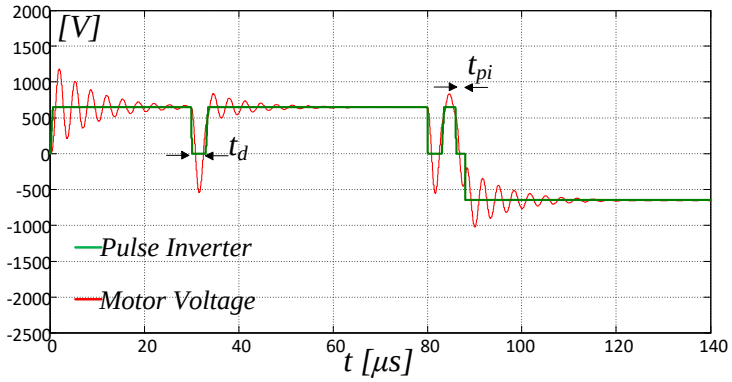


Fig. 3. 46 Motor voltage with proposed modification of dropping region t_d and polarity reversal time t_{pi}

3.2 Proposed overvoltage mitigation on Open-end Winding AC Motor Drive

An overvoltage mitigation approach is presented for an Open-end Winding Electrical Drive (OWED) with long feeders [35]. The conventional Open-end Winding structure is depicted in Fig. 3. 47. The two inverters are electrically isolated in order to avoid the circulation of zero sequence currents.

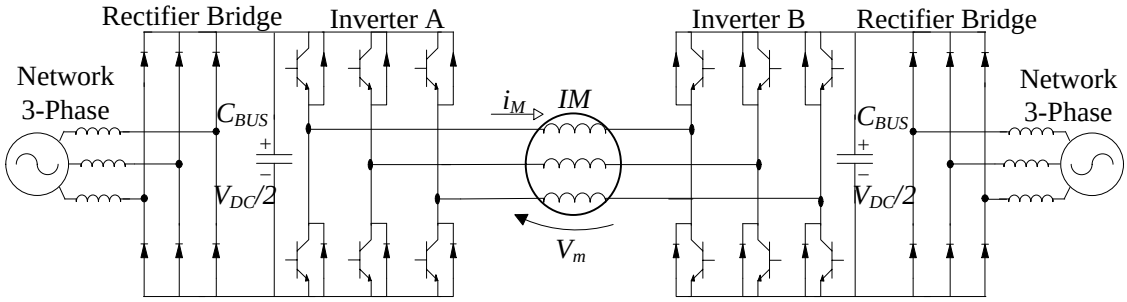


Fig. 3. 47 Conventional Open-end Winding AC motor Drives with two isolated inverters

The configuration system adopted in the proposed overvoltage mitigation technique is shown in Fig. 3. 48. A main three phase two-level inverter feeds the motor through a long electric cable from one side, while, on the other side, a two-level inverter is located close to the motor. The last inverter is equipped with a floating capacitor in order to have a single DC power source. A conventional sine-PWM modulation is adopted in order to eliminate any zero-sequence current. Moreover, in order to hold the voltage V_c across the capacitance of the floating inverter, equal to the DC Bus voltage V_{DC}, the negative DC bus rail of each inverter is connected to the ground. A bipolar, double edge, pulse width modulation strategy is implemented in each motor phase and it is explained in Fig. 3. 49.

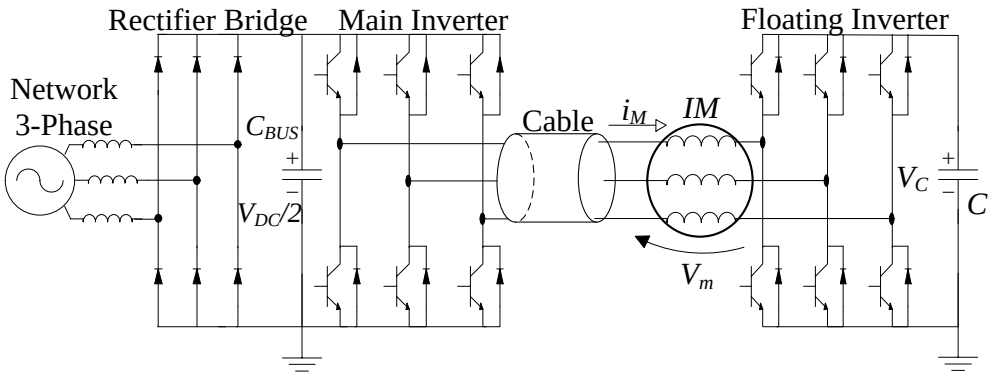


Fig. 3. 48 Proposed Open-end Winding AC motor Drives with two non-isolated inverters and floating capacitor

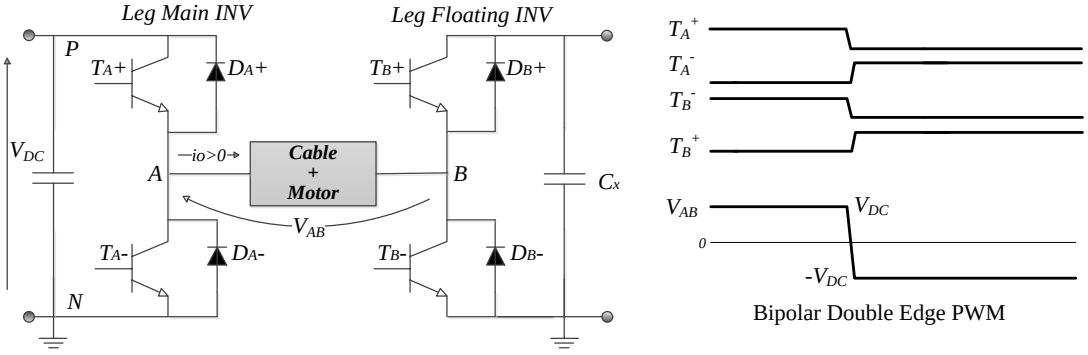


Fig. 3. 49 Single phase representation of Fig. 48

Power devices T_A^+ and T_B^- are driven by the same gate signal, that is inverted to drive T_A^- and T_B^+. Thus, when T_A^+ is turned on, also T_B^- is turned on while T_A^- and T_B^+ are turned off and vice versa. This is equivalent to shift the output voltage of the floating inverter by 180° from the output voltage of the main inverter.

During normal operation, with a bipolar double edge PWM, the phase voltage measured at the motor terminals can double the DC link voltage V_{DC} as depicted in Fig. 3. 50.

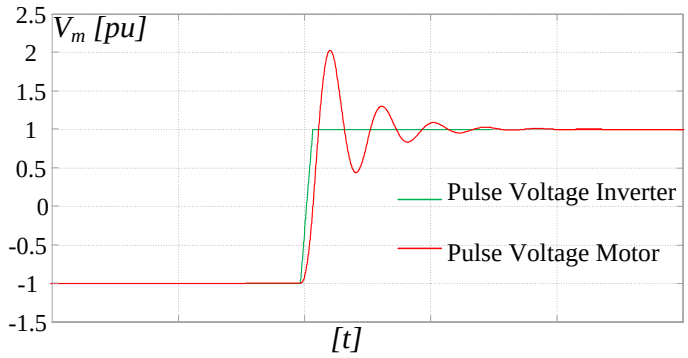


Fig. 3. 50 Motor Voltage wave in an Open-end Winding AC motor

The proposed overvoltage mitigation approach acts on the switching patterns of the power devices and it is very simple in principle. More precisely, a dwell time T_{dw} is introduced either between switching times of devices

T_B^+ and T_A^-, either between switching times of T_A^+ and T_B^-. This principle is the same to that proposed in [8], where six additional power devices are introduced in a conventional wye-connected AC motor. Fig. 3. 51 shows the motor voltage waveform when the proposed approach is adopted. Along T_{dw}, T_A^+ and T_B^+ are turned on and the voltage V_{AB} across the load is equal to zero, as explained in eq. (3.31). Therefore, the voltage variation is equal to V_{DC} rather than 2 V_{DC} and the over-voltage is reduced consequently.

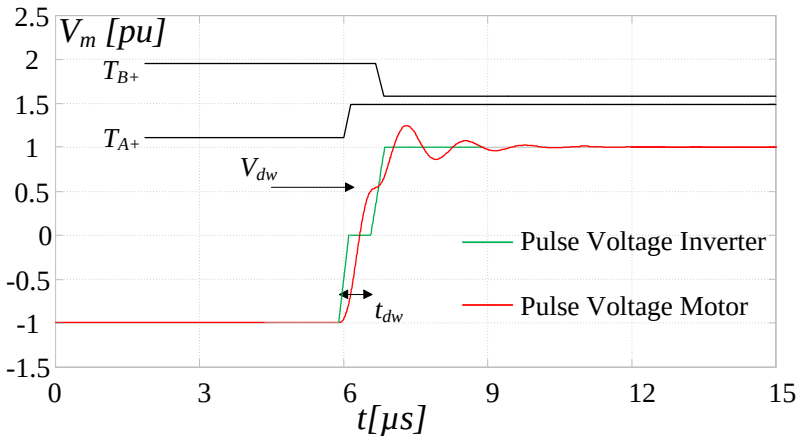


Fig. 3. 51 Motor Voltage Wave in an Open Winding AC motor drive with Dwell Time T_{dw}.

The proposed overvoltage mitigation technique has been evaluated through simulations exploiting high frequency mathematical models of the power cable and the AC motor. Main parameters of the considered system are listed in Table 3.3 and Table 3.4. Lumped parameters equivalent circuits of the cable and motor are respectively shown in Fig. 3. 52 and Fig. 3. 53. A 3Hp-50Hz-380V induction machine and a one hundred nodes high-frequency model of a100 meters long 12 AWG PVC cable are considered. Moreover, the main inverter input voltage and switching frequency are respectively 570V and 10kHz. Finally, a 3kV/μs voltage gradient is assumed. Time diagrams shown in Fig. 3. 54 deal with the phase voltage at the motor terminals obtained with different values of the dwell time T_{dw}. As shown in Fig. 3. 54b the minimum peak over-voltage is obtained when the dwell time is made equal to one fourth of the voltage oscillation period T_{cycle} which is to say T_{dw}=2τ, being τ the transport delay of the transmission line. Moreover, the worst condition occurs when T_{dw} =0.75 T_{cycle} in this case the sum of the two voltage components, directed and reflected wave, does not result equal to 0, as given by Fig. 3. 38. It is easy to observe that the optimal value of T_{dw} depends on the natural frequency f_0 of the cable, and it is strictly related to its length as well as to *R*, *L* and *C* values. Fig. 3. 55 shows the results of simulations taking into account 14 AWG PVC 2.5 mm^2 cables of different lengths. As it is possible to observe, when increasing the cable length, it is necessary to increase the dwell time to obtain even the same peak voltage (695V with a 570V DC bus voltage). This is in agreement with the transmission line theory, as the natural frequency of voltage oscillation f_o at the motor terminals is inversely proportional to the cable length eq. (3.18). Therefore,

increasing the cable length, the natural oscillation frequency of the voltage decreases, while the period increases, leading to a longer T_{dw} to obtain the maximum over-voltage attenuation. Fig. 3. 56 shows the voltage at the motor terminals V_m when 14 AWG wires with different lengths are considered. A constant 0.78μs dwell time is applied, giving a maximum overvoltage attenuation when a 25m long cable is considered. Keeping constant the dwell time, a progressively smaller reduction of the overvoltage is obtained when the cable length is increased. Diagrams of Fig. 3. 57 and Fig. 3. 58 deal with the variation of the optimal T_{dw} as a function of the cable length for different wire sizes (# 8, # 10, # 12 and # 14 AWG) and for different values of voltage attenuation. From eq. (3.18), comes that the frequency f_0 is also inversely proportional to cable inductance L and capacitance C per unit length. When considering different types of cables, the product LC varies, leading to different values of f_0. Higher f_0 require lower T_{dw} for a given over-voltage attenuation. Diagrams move down if the attenuation of the desired voltage decreases and vice versa.

Table. 3.3. Parameters of the HF motor model.

Ratings [Hp]	Cg [pF]	Rg [Ω]	Ld [mH]	Re [kΩ]	Ct [pF]	Lt [mH]	Rt [kΩ]
3	314	35.5	4.0	5.6	31.4	2.7	1.15

Table. 3.4. Parameters of the HF cable model.

Cable Gauge	Rs [mΩ]	Ls [μH]	Rp1 [MΩ]	Rp2 [kΩ]	Cp1 [pF]	Cp2 [pF]
8	6.0	0.20	262.1	21.2	119.7	15.3
10	7.0	0.28	221.7	18.9	125.4	17.7
12	7.5	0.26	218.8	22.8	104.7	16.8
14	16.0	0.29	265.7	25.4	93.9	16.8

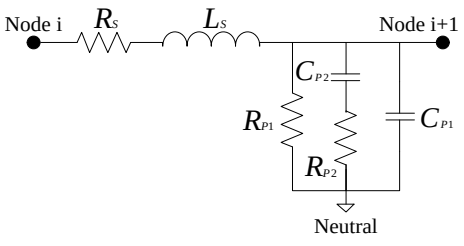


Fig. 3. 52. Per-phase high-frequency model of the power cable per-unit length.

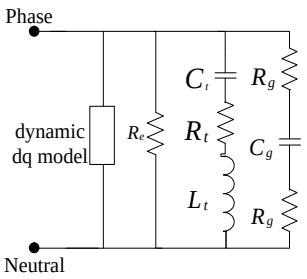


Fig. 3. 53. Per-phase high-frequency model of the motor per-unit length

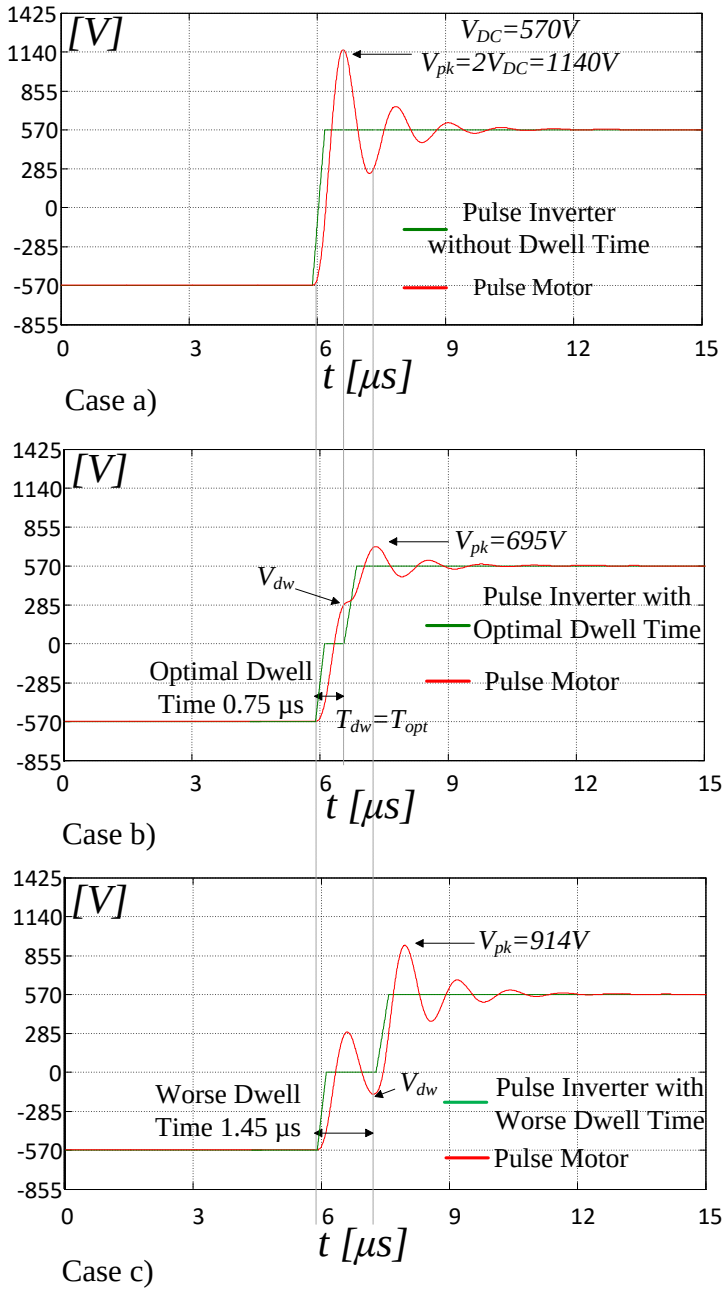


Fig. 3. 54. Voltage at motor terminals with different dwell time: Cable 12 AVG PVC, 3Hp Motor, trise=0.4μs, 10kHz

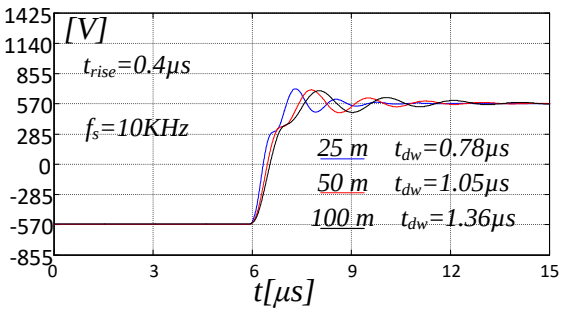


Fig. 3. 55. Phase motor voltage:Optimal dwell times for14 AWG cables of different lengths, 3Hp motor.

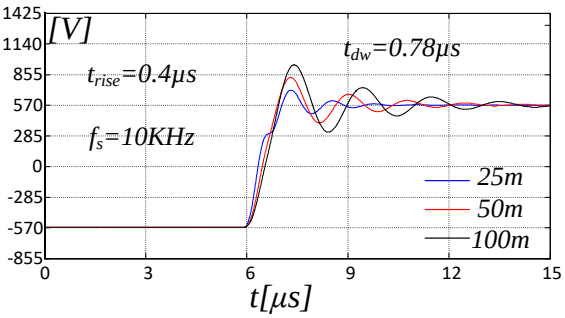


Fig. 3. 56. Voltage at motor terminals with T_{dw} =0.78 μs and cables of different lengths.

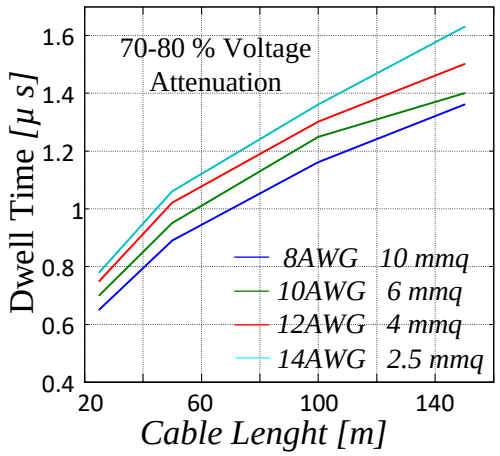


Fig. 3. 57. Dwell times required to obtain a 70-80 % overvoltage attenuation.

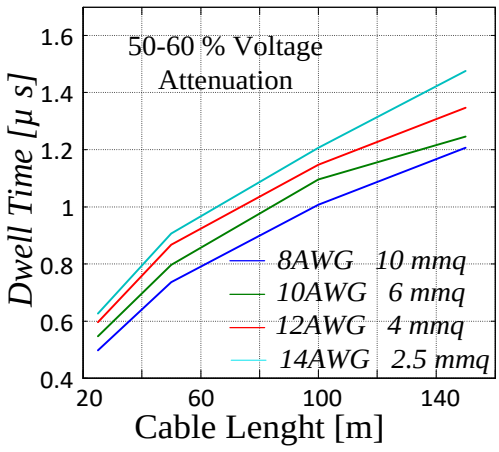
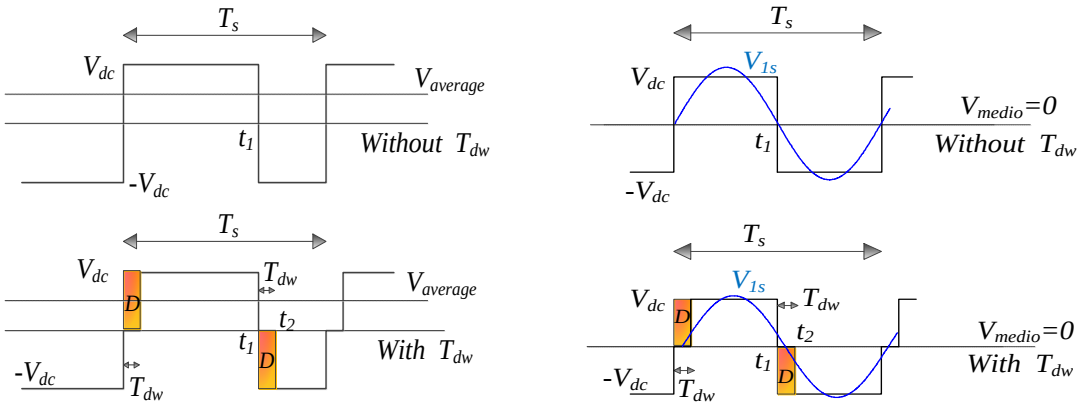


Fig. 3. 58. Dwell times required to obtain a 50-60 % overvoltage attenuation.

A dead time is normally introduced in PWM voltage source inverters to prevent transient short circuits through devices of the same legs. It varies from 500ns up to a few microseconds, depending on technical features of inverter power devices. Differently, the value of the dwell time T_{dw} is only related to cable characteristics, cable length and desired level of attenuation. According to the obtained results, the dwell time T_{dw} is comparable and even smaller than the dead time normally introduced on inverters of the tested drives.

3.2.1 Dwell Time impact on Inverter output voltage

The introduction of the dwell time does not impact the RMS value of the fundamental voltage component. In fact, as shown in Fig. 3. 59a, in a switching period T_s, the area D is equally subtracted on the positive and negative half wave of V_m.



(a) (b)

Fig. 3. 59. Effects of T_{dw} on the average voltage (a) null average voltage (b)

Thus the average voltage $V_{average}$ is unchanged, as the RMS value. However, the introduction of the dwell time T_{dw} has effects on the harmonic spectrum of the motor phase voltage. As shown in Fig. 3. 59b, the introduction of T_{dw} generates an additional zero voltage level, thus a three levels voltage modulation is accomplished, rather than a two levels one. The high frequency harmonic content of the motor phase voltage can be characterized through the coefficients of the decomposition in Fourier series of the waveform eq. (3.38) and eq. (3.39), where $T_s = 1/f_s$. The Fourier series coefficients are function of the dead time T_d and of the dwell time T_{dw}:

$$V_{AB}(t) = \frac{a_0}{2} + \sum_{h=1,2\ldots\infty} \sin(ht)a_h + \cos(ht)a_h$$

$$a_h = \frac{2}{T_S}\int_0^{T_S} V(t)\sin(h\omega t)dt = \frac{2}{T_S}\int_{T_{dw}}^{T_{off}+T_d} V_{dc}\sin(h\omega t) +$$

$$+\frac{2}{T_S}\int_{T_{dw}+T_d+T_{off}}^{T_S} -V_{dc}\sin(h\omega t) = \frac{2V_{dc}}{h\omega T_S}\left[\cos(h\omega T_S(1-\delta)+h\omega T_d) + \right.$$

$$\left. -\cos(h\omega T_{dw}) - \cos(h\omega T_S) + \cos(h\omega T_S(1-\delta)+h\omega(T_{dw}+T_d))\right] \quad (3.38)$$

$$b_h = \frac{2}{T_S}\int_0^{T_S} V(t)\cos(h\omega t)dt = \frac{2V_{dc}}{h\omega T_S}\left[-\sin(h\omega T_S(1-\delta)+h\omega T_d) + \right.$$

$$\left. +\sin(h\omega T_{dw}) + \sin(h\omega T_S) - \sin(h\omega T_S(1-\delta)+h\omega(T_{dw}+T_d))\right]$$

The *rms* value of the *h* harmonic is given by:

$$C_h = \sqrt{a_h^2 + b_h^2} \quad (3.39)$$

Fig. 3. 60, shows the trend of the amplitude of the main odd harmonics as a function of T_{dw}, for a 0.5 duty cycle. Moreover, a dwell time of 1μs is considered and a dead time lower than T_{dw}. Fig. 3. 61 shows the amplitude of main even harmonics. These are computed taking into account one period T_s of the high-frequency voltage waveform and are independent from drive operative conditions. The amplitude C_1 of the fundamental voltage V_{1m}, at the switching frequency remains almost constant, while the amplitude of all other harmonics decreases when T_{dw} increases from 0 to 4 μs.

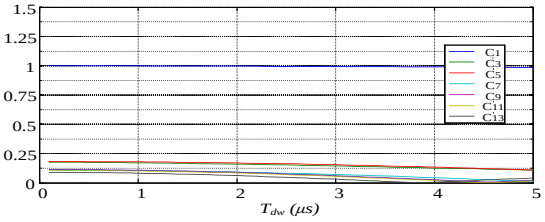


Fig. 3. 60 Odd harmonics amplitude vs. T_{dw}.

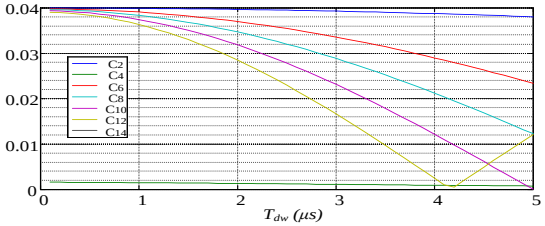


Fig. 3. 61 Even harmonics amplitude vs. T_{dw}.

3.2.2 Dwell Time Adaptation

In order to properly establish the optimal dwell time, an adaptive algorithm has been developed. It starts from a measurement of the motor peak phase voltage through the circuit shown in Fig. 3. 62. It encompasses two small resistances R_1, R_2 and a capacitor C. Moreover, two switches are present, alternatively driven at a low frequency (<1Hz).

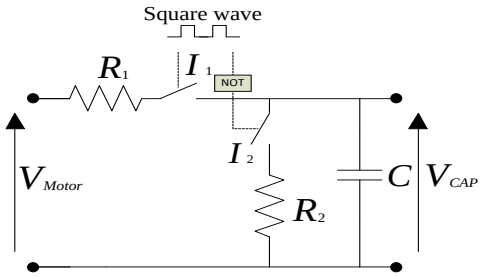


Fig. 3. 62 Circuit used to detect the peak phase voltage.

When I_1 is turned on and I_2 is turned off, R_1 is exploited to charge the capacitor C to the maximum phase voltage V_{pk}. The voltage is acquired and stored in the control unit. After that I_1 is turned off and I_2 is turned on, then the capacitor C is discharged through the resistor R_2. By comparing two consecutive samples the peak voltage gradient is detected and the dwell time is accordingly modified. Hence, if V_n is the voltage across the capacitance at time t_n and V_{n-1} is the voltage across the capacitance at time t_{n-1}, the dwell time is increased whenever $V_n < V_{n-1}$ while if $V_n > V_{n-1}$the dwell time is decreased, Fig. 3. 63. The voltage V_{CAP} is the input of the tracking algorithm developed through the Matlab/Simulink software, Fig. 3. 64. Such an algorithm stores the amplitude of V_{CAP} in t_{n-1} V_{CAP}(n-1) and compares this value with the actual value V_{CAP}(n), the dwell time is then increased or decreased. Fig. 3. 65 shows the operation of the tracking minimizing the peak phase voltage of the motor. Even the dwell time is updated at a low frequency, the peak overvoltage is quickly reduced to half of the initial value. Moreover, exploiting the developed dwell time adaptation algorithm the proposed method is made independent from cable, converter and motor parameters.

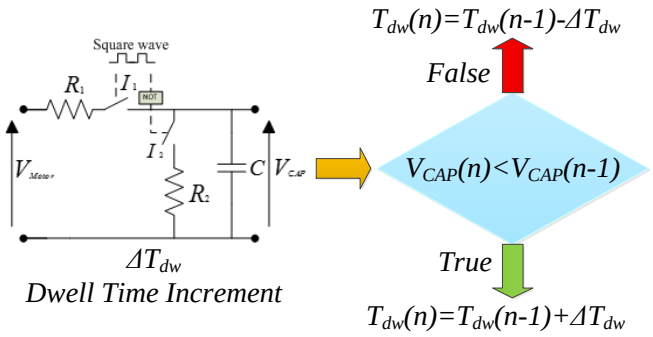


Fig. 3. 63 Logic scheme of tracking of T_{dw}.

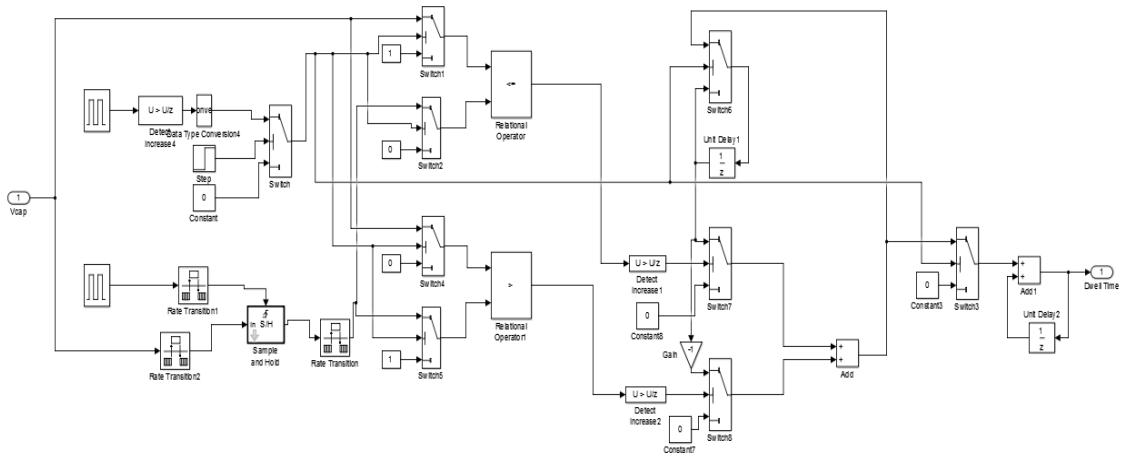


Fig. 3. 64 Matlab/Simulink blocks of tracking of T_{dw}.

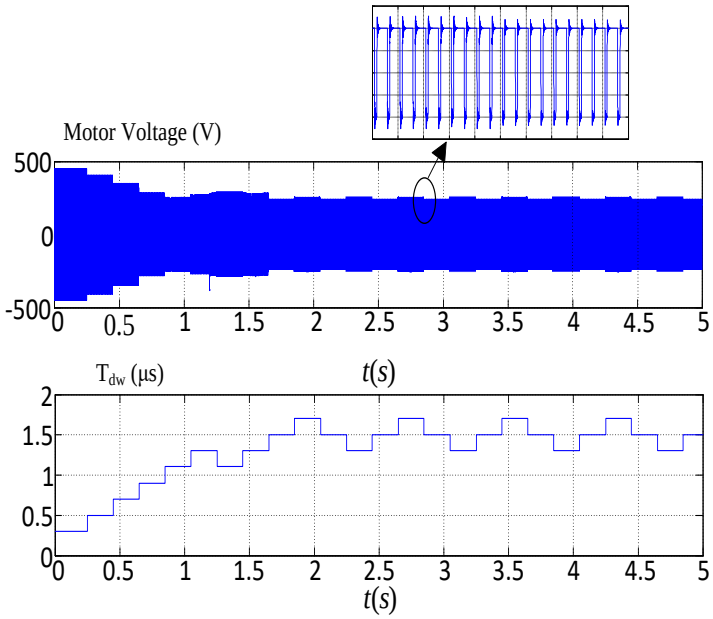


Fig. 3. 65 Adaptation of T_{dw}

3.2.3 Experimental Validation

Experimental tests have been carried out in order to verify the ability of the proposed method in mitigating motor overvoltages. The test bench consists of a 1.2kW, 380V, 50Hz open-end winding AC motor drive, a 50m power cable featuring a 2mm^2 cross sectional area. The parameters of the cable have been measured through a RLC power analyzer, as recommended in [30] giving: C_o=314 pF and L_o=0.8 mH. The DC-Bus voltage of the floating inverter is rated at 400V, while a 3.3mF, DC-Bus capacitor is used. A bipolar PWM is implemented on the two inverters, featuring a 10kHz switching frequency. Fig. 3. 66 shows the *a*-phase inverter output voltage

without dwell time, while Fig. 3. 67 depicts the same inverter output voltage with correct T_{dw}=1.1μs. The resulting motor voltage waveforms for different value of dwell time is shown in Fig. 3. 68. The corrected T_{dw}=1.1μ gives rise a peak value of overvoltage equal to 210 V. As mentioned earlier, the percent motor voltage attenuation *A* is strictly related with the value of dwell time, as depicted in Fig. 3. 69. In particular, the trend of the voltage attenuation *A* follows the trend of the motor voltage oscillation.

Fig. 3. 70a shows V_m, V_{CAP}, i_m and the ground current i_G without dwell time, Fig. 3. 70b shows the same signals with a different time scale, in order to highlight that the ground current i_G consists only of high frequency components. Fig. 3. 71a shows how the introduction of a proper T_{dw} reduces the peak overvoltage from $2V_{DC}$ to zero. In Fig. 3. 71b a different time scale is used to highlight the absence of low order ground current harmonics.

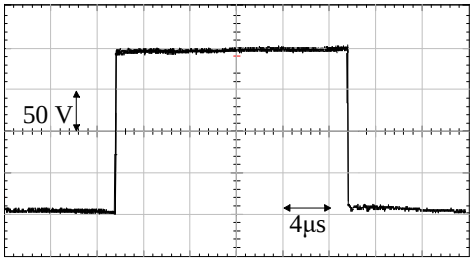


Fig. 3. 66 Inverter Output Voltage Waveform without dwell time

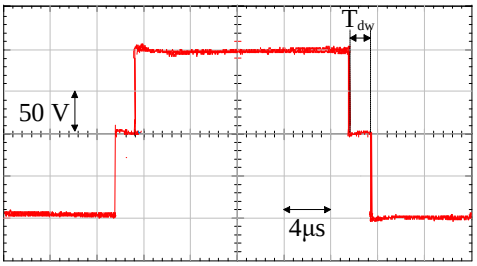


Fig. 3. 67 Inverter Output Voltage Waveform with dwell time

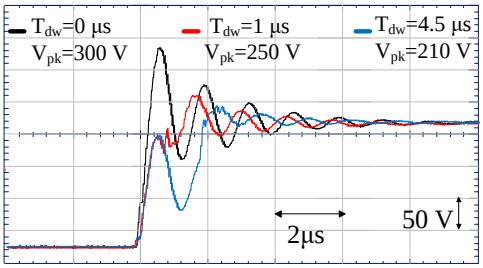


Fig. 3. 68 Overvoltage for different Dwell time

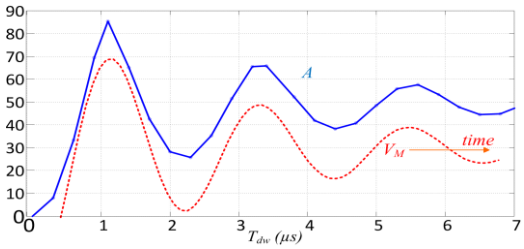
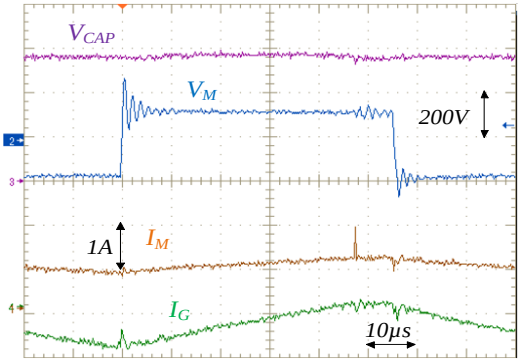
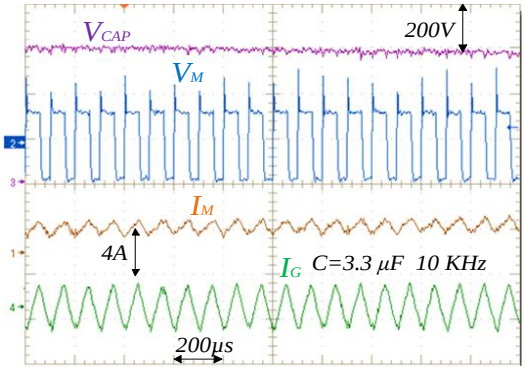


Fig. 3. 69 Peak voltage (%V_{pkmax}) vs.T_{dw}

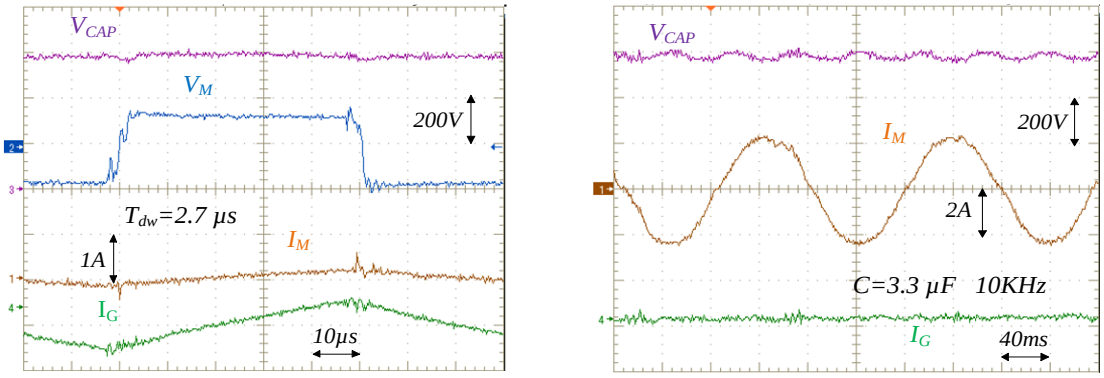


(a)



(b)

Fig. 3. 70 Motor Voltage without Dwell Time



(a) *(b)*

Fig. 3. 71 Motor Voltage with correct Dwell Time

3.2.4 Proposed RC Passive Filter on Open-end Winding AC Motor Drive

Two LTNs RC passive filters are proposed exploiting an Open-end Winding system. First, a RC network is connected in parallel to each phase winding connected in open-end configuration, as depicted in Fig. 3. 72. Secondly, a delta connected RC filter is installed at the motor terminals, Fig. 3. 73.

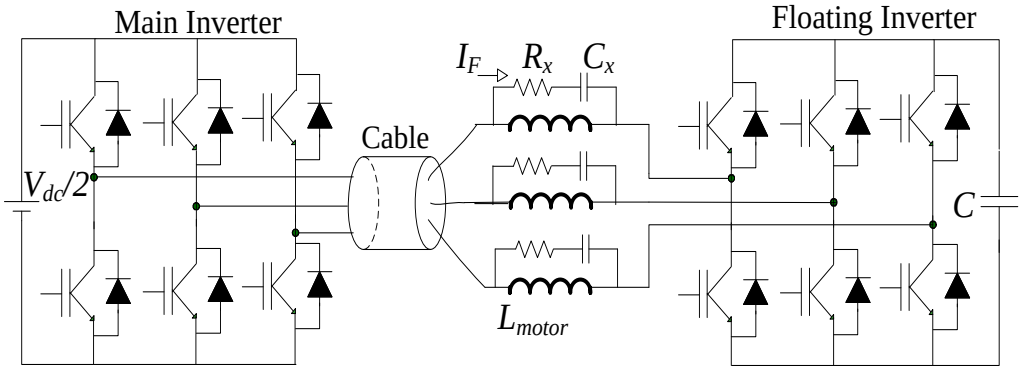


Fig. 3. 72. Open-end Winding System with parallel passive RC filter.

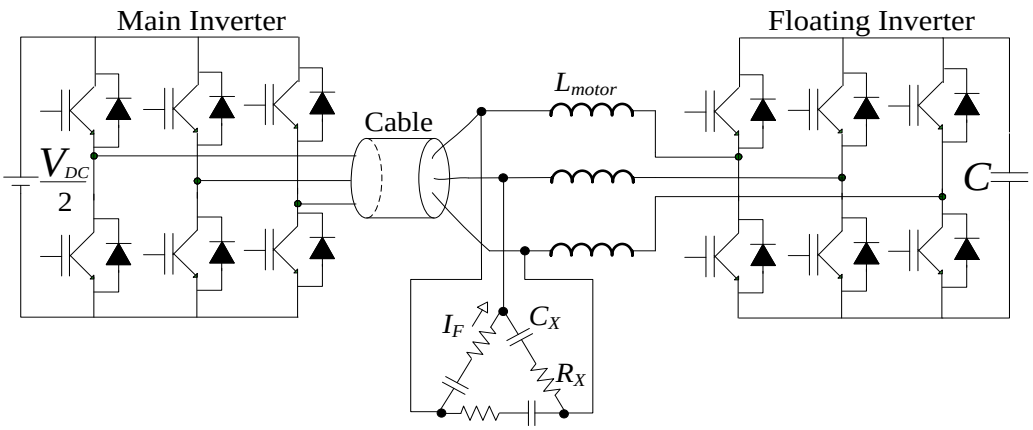


Fig. 3. 73. Open-end Winding System with delta connection passive RC filter.

In this case the two inverters are not connected to the ground and a suitable control strategy is implemented to control the voltage of the DC-Bus of the floating inverter [34]. Moreover, a standard unipolar PWM modulation has been used instead of the bipolar one. Parameters R_x and C_x are determined as in [30], by supposing the voltage across the filter capacitor C_x lower than 10%V_{DC} at the end of the voltage rise time (t_{rise}=*500ns*). Finally, the resistance of the filter R_x is made equal to the cable natural frequency Z_0=61Ω.

$$V_{CAPx} = (0.1)V_{DC} = V_{DC}\left(1 - e^{-t_{rise}/(R_x C_x)}\right) \tag{3.40}$$

The natural impedance Z_0 of the cable is identified as in [30] using an LRC analyzer. Cable and filter parameters are respectively shown in Table 3.5 and Table 3.6.

Table. 3.5. Cable parameters.

L_0[μH]	C_0[pF]	Z_0[Ω]
0.8	314	61

Table. 3.6. Filter parameters.

R_x[Ω]	C_x[pF]
61	80

The voltage at the motor terminals without passive filter is shown in Fig. 3. 74. Fig. 3. 75 shows the effect of a parallel passive RC filter, with C_x=80nF and R_x=Z_0=61Ω where V_{CAP} is the voltage across the capacitance of the floating inverter, V_M is the motor voltage and I_F is the current of the RC filter, while Fig. 3. 76 depicts the motor voltage with a delta connected RC filter. In both cases, the value of the capacitor C_x is obtained by eq. (3.40). Furthermore, with the delta connection, each RC network is fed by line to line voltage and so a larger capacitance C_x=400nF should be adopted if compared with the parallel RC filter C_x=80nF. Thus, the parallel RC filter is more effective than the delta-configuration, moreover, the RC network is subjected to the phase voltage, while in the delta-configuration network is subjected to the line to line voltage, resulting in extra power losses.

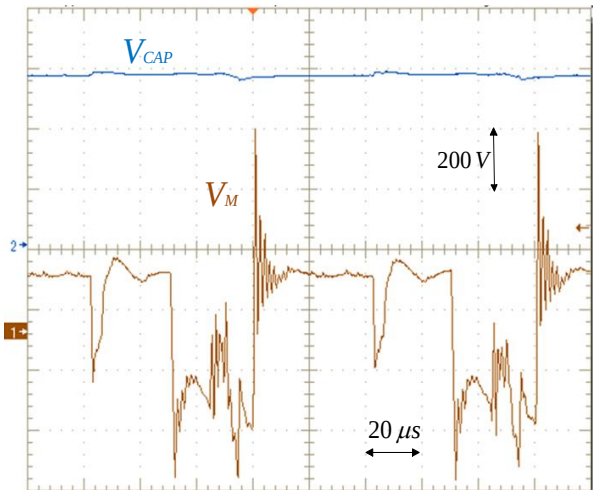


Fig. 3. 74. Motor Voltage without any passive RC filter

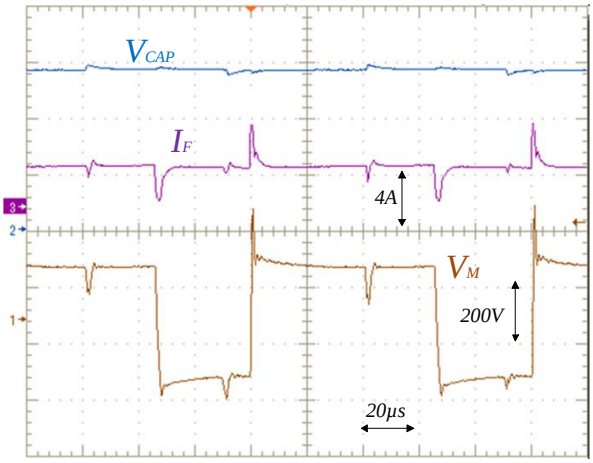


Fig. 3. 75. Parallel passive filter RC (Cx=80 nF)

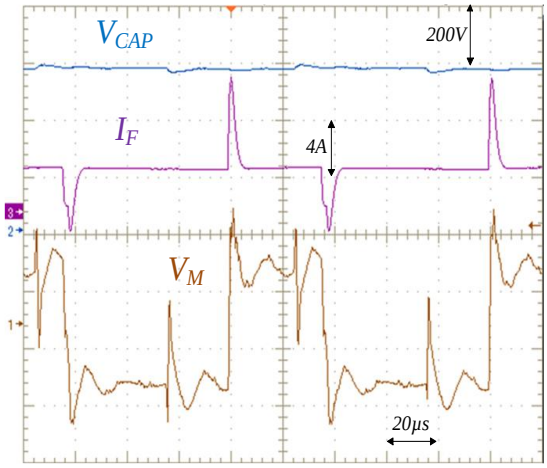


Fig. 3. 76. Delta passive filter RC (Cx=22 nF)

As shown in Table 3.7 the proposed approach performs better than the two passive filters in mitigating the over-voltage at motor terminals. In the considered operating conditions, the dwell time approach scores an 85% peak voltage attenuation, versus a 53% and a 34% respectively obtained with the parallel and the delta connected RC filter. Moreover, no additional losses are generated, while Joule power losses are caused in the damping resistance and inductance parasitic resistance of the passive filters, do not mentioning inductance core losses. Under this point of view, the parallel RC filter is advantaged over the delta connected one by a lower peak current.

Table. 3.7. Cable parameters

Method	*A* [%]	I_{Fpk} [A]	*Losses[%]*
Proposed T_{dw}	85	0	0
Parallel RC Filter	53	3.8	0.31
Delta RC Filter	34	7.5	0.6

Furthermore, the proposed parallel RC filter is more efficiency of RC networks in [7] and [30] depicted in Table 3.1 installed on a conventional wye-connected and delta-connected AC motor.

3.3 References of Chapter 3

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4 Chapter: Asymmetrical Hybrid Multi-Level Inverter (AHMLI)

An Asymmetrical Hybrid Multilevel Inverter (AHMLI) has been developed for applications in AC motor drives, generation systems, STATCOM systems, Photovoltaic and Wind generators [21]. The idea is that to exploit either the benefits of a Multi-level inverter, either those of an Open-end Winding system (OWS). As shown in

Fig. 4. 1, the standard OWS scheme is obtained by splitting the neutral connection of an AC machine and connecting each end-phase of the winding to a two three phase two-level inverters. Based on the ratio between the two DC-Bus voltages, this configuration may feature a three-level or a four-level voltage modulation while achieving several other benefits as redundancy of the space-vector combinations, absence of neutral point fluctuations, reduction of the phase current ripple and increment of the maximum allowable stator voltage amplitude.

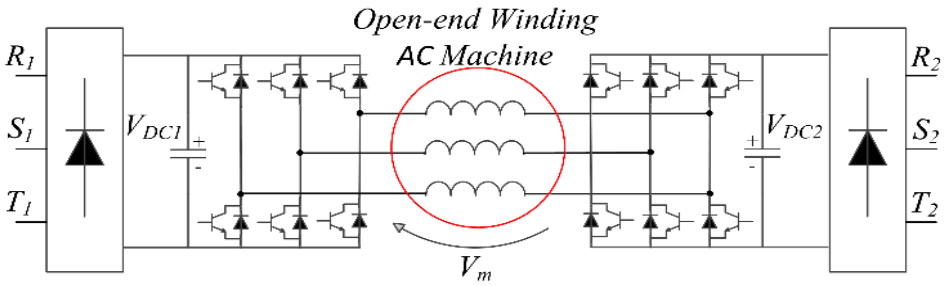


Fig. 4. 1 Standard Multilevel inverter

According to the basic OWS configuration the active power demanded by the AC machine is shared between the two inverters, consequently they are generally of the same, or similar, size and are supplied by two separated power sources [17]-[19]. Differently, according to the proposed AHMLI approach, a main MLI supplies the whole active power, while a smaller auxiliary TLI acts as an active filter. Providing a zero-average active power, the latter can be supplied through a floating capacitor, not requiring an additional independent power source. A staircase voltage modulation technique is adopted in MLI in order to minimize switching losses, while the TLI exploits a high frequency PWM strategy in order to accurately shape the output current. In order to obtain sinusoidal motor phase currents, the output voltage of the auxiliary inverter must be equal to the difference between the sinusoidal reference signal and the staircase waveform generated by the MLI. If compared with a conventional drive encompassing a low frequency switching MLI the proposed solution produces a minimal

current distortion, thus preventing the occurrence of the torque ripple in AC Motor Drive applications. On the other hand, if compared with PWM operated MLI, the proposed solution generates lower conversion power losses. A key feature of the proposed approach consists in the possibility to use different kinds of power devices to optimally cope with the specific requirements of the two inverters. More precisely, as the MLI switches at low frequency it allows the utilization of power devices featuring very low conduction losses as, for example, GTOs or high current IGBTs. Differently, the TLI operating at low voltage levels and high switching frequency needs low voltage, low switching losses power devices such as fast IGBTs or even Power MOSFETs.

4.1 Proposed AHMLI configuration

The proposed asymmetrical hybrid multilevel inverter configuration is shown in Fig. 4. 2 Asymmetrical Hybrid Multilevel Inverter (AHMLI) It includes a MLI as main power unit and an auxiliary TLI acting as an active power filter (MLI+TLI). A neutral point clamped NPC or a flying converter FC can be adopted as multilevel inverter topology.

As discussed in chapter 3, an increment of the amount of inverter voltage levels is advantageous in terms of load current THD. It is here obtained by using two inverters with isolated DC-Buses, which permits also to prevent the occurrence of zero sequence currents. Normally, an OWS with two isolated DC-Buses needs of two isolated power supplies. On the contrary, as the TLI ideally supplies the OW machine with zero average active power, it can be fed by a floating capacitor making a second independent power source redundant.

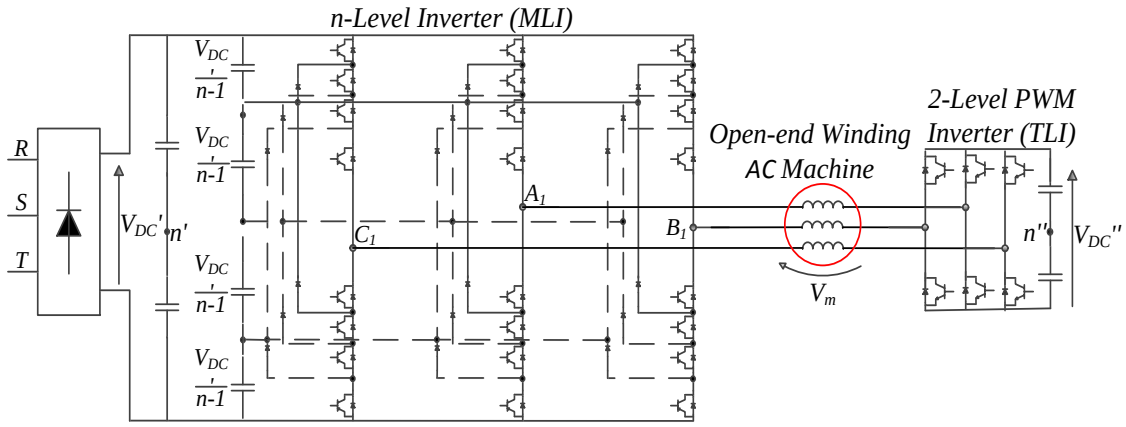


Fig. 4. 2 Asymmetrical Hybrid Multilevel Inverter (AHMLI)

4.1.1 Space vector combinations of AHMLI

The motor phase voltage must be considered in order to compare the performance of the proposed solution with conventional ones, because on an OWS the MLI line-to-line voltage does not univocally define the motor phase voltage. In a generic *n*-level MLI, the DC-Bus is composed of *n*-1 series connected capacitors. In order to investigate the AHMLI output voltage waveform, Fig. 4. 3 and Fig. 4. 4 are considered.

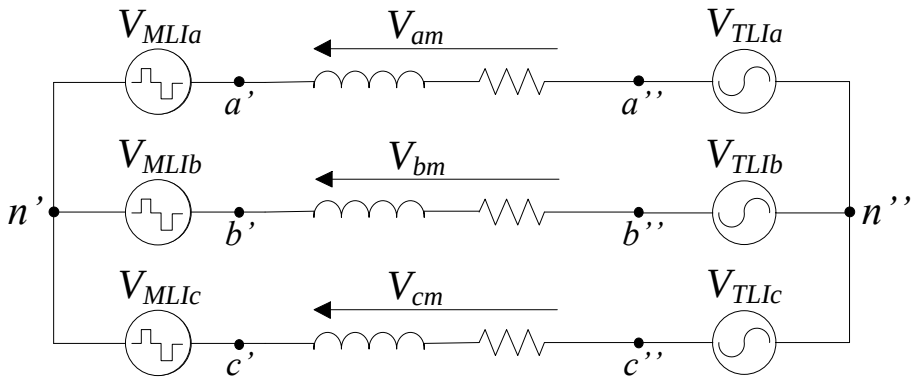


Fig. 4. 3 Equivalent circuit of a AHMLI configuration

The inverter "*a*" leg output voltage V_{MLIa}, referred to the mid-point *n´* of the DC-Bus, is:

$$V_{MLIa} = \frac{2l'-n+1}{2(n-1)} V_{DC}' \qquad l' = 0,1,2 \ldots n-1 \tag{4.1}$$

being V_{DC}' the MLI DC-Bus voltage. Assuming, as shown in Fig. 4. 4 that the inverter supplies a wye connected induction machine, the motor "*a*" phase voltage V_{aMLIO}, i.e. the voltage between the inverter "*a*" phase terminal and the stator winding neutral point O is:

$$V_{mMLIa} = \frac{2l'-n+1}{2(n-1)} V_{DC}' - V_O \qquad l' = 0,1,2 \ldots n-1 \tag{4.2}$$

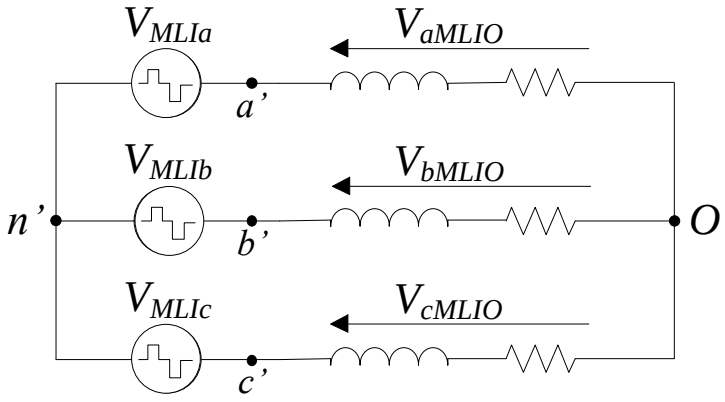


Fig. 4. 4 Equivalent circuit of wye-connected machine

where V_O is given by:

$$V_O = \frac{1}{3}\left(V_{MLIa} + V_{MLIb} + V_{MLIc}\right) \tag{4.3}$$

The latest quantity is known as Common-Mode Voltage (CMV), as discussed in chapter 2.

Taking into account eq. (4.1) and eq. (4.3), being *n* an odd number, a motor phase voltage can assume *4(n-1)* different non-zero voltage levels and the zero one. The amount of the power switches required by an *n*-level NPC or FC MLI is:

$$n_{psMLI} = 2p(n-1) \tag{4.4}$$

being *p* the number of inverter legs.

The same calculation can be performed for a standard three-phase two-level inverter TLI. The *a*-leg phase output voltage referred to the mid-point *n´´* of the TLI DC-Bus $V_{DC}^{''}$ is:

$$V_{TLIa} = \frac{2l''-1}{2} V_{DC}^{''} \qquad l'' = 0,1 \tag{4.5}$$

Assuming that the TLI inverter supplies a wye connected induction machine, the motor phase voltage V_{mTLIa} is:

$$V_{mTLIa} = \frac{2l''-1}{2} V_{DC}^{''} - V_O \qquad l'' = 0,1 \tag{4.6}$$

where, V_O it is given by eq. (4.3). Therefore, the motor phase voltage can assume one of four possible non-zero voltage levels, namely: $2V_{DC}^{''}/3$, $V_{DC}^{''}/3$, $-V_{DC}^{''}/3$ and $-2V_{DC}^{''}/3$, or the zero level. The amount of power switches in a TLI is:

$$n_{psTLI} = 2p \tag{4.7}$$

As mentioned in chapter 2, the concept of CMV in an OWS with two isolated DC-Buses differs from the concept of CMV of a standard converter configuration. Specifically, the voltage $V_{n'n''}$, is considered in an OW configuration, as depicted in Fig. 4. 3:

$$V_{n'n''} = \frac{1}{3}\left(V_{MLIa} + V_{MLIb} + V_{MLIc}\right) - \frac{1}{3}\left(V_{2LIa} + V_{2LIb} + V_{2LIc}\right) \tag{4.8}$$

This is constant if the two DC-Buses are electrically connected, or variable, as in the present case, if the DC-Bus capacitor of the TLI is floating.

According to the proposed AHMLI configuration, assuming that two independent DC voltage sources $V_{DC}^{'}$ and $V_{DC}^{''}$ supply the two inverters, the voltage V_{am} applied to *a*-phase winding of the OW machine is:

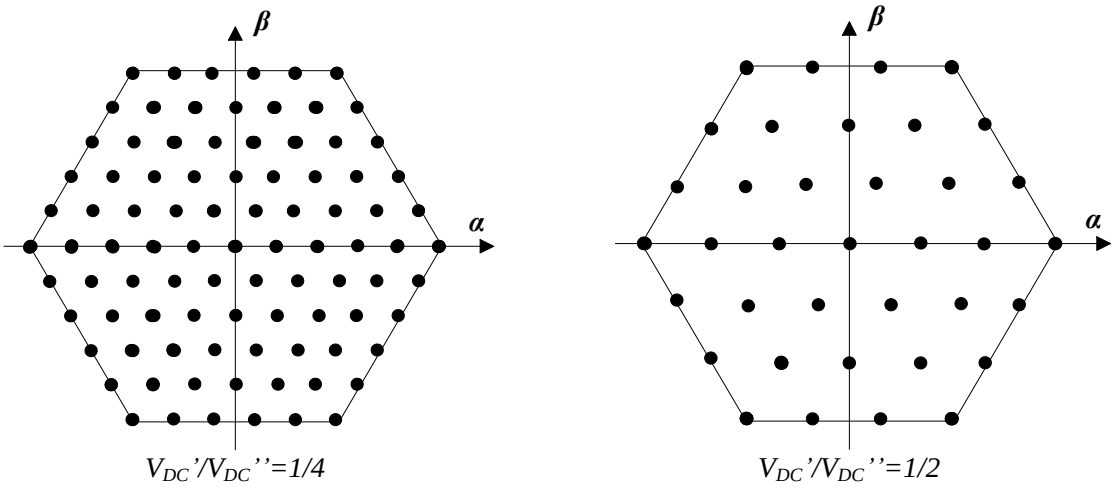
$$V_{am} = V_{MLIa} - V_{TLIa} = \frac{2l'-n+1}{2(n-1)} V_{DC}' - (2l''-1) V_{DC}''/2 - V_{n'n''} \qquad (4.9)$$

$$l' = 0,1,2 \ldots n-1 \qquad l'' = 0,1$$

The amount of required power switches n_{ps} is:

$$n_{psT} = 2pn \qquad (4.10)$$

Eq. (4.9) is an important result for understanding that the AHMLI output voltage waveform depends on the values of DC-Buses voltage V_{DC}' and V_{DC}''. The space vector combinations and the output voltage levels, in fact, are as a function of the voltage ratio V_{DC}'/V_{DC}''. Fig. 4. 5 shows the voltage vector plots for an AHMLI encompassing a three-level inverter, for two different DC voltage ratio. When the voltage ratio is set to $V_{DC}''=V_{DC}'/4$, the space phasors appears as that of a six-level inverter, while if $V_{DC}'' = V_{DC}'/2$, the vector plots are that of a four-level inverter. These last results are calculated in Tab. 4.1, where the term $V_{n'n''}$ is not considered. In general, if $V_{DC}'' = V_{DC}'/[2(n-1)]$, the space vector combinations are that of a *2n*-levels inverter, while if $V_{DC}'' = V_{DC}'/[(n-1)]$, the AHMLI works with lower space vector combinations. The AHMLI works as a *2n*-levels inverter also for $V_{DC}'' < V_{DC}'/[2(n-1)]$, but how it will be demonstrated in the following, the harmonic suppression method is less effective.



$V_{DC}'/V_{DC}''=1/4$ $V_{DC}'/V_{DC}''=1/2$

Fig. 4. 5 AHMLI Vector plots

Tab. 4.1 AHMLI output voltage levels when $V_{n'n''}$ is not considered

Voltage ratio V_{DC}'/V_{DC}''	3LI Output voltage levels V_{MLI}	TLI Output voltage levels V_{TLI}	AHMLI Output voltage levels $V_m = V_{MLI} - V_{TLI}$
1/4	V_{DC}', $V_{DC}'/2$, 0	$V_{DC}'/4$, 0	$3V_{DC}'/4$, V_{DC}', $V_{DC}'/4$, $V_{DC}'/2$, $-V_{DC}'/4$, 0
1/2	V_{DC}', $V_{DC}'/2$, 0	$V_{DC}'/2$, 0	$V_{DC}'/2$, V_{DC}', 0, $-V_{DC}'/2$
1/[2(n-1)]	*eq. 4.1*	*eq. 4.5*	*2n*
1/[(n-1)]	*eq. 4.1*	*eq. 4.5*	*3(n-1)/2*

In terms of phase voltage levels, taking into account $V_{n'n''}$, the proposed AHMLI configuration is equivalent to a conventional NPC or FC multilevel inverter with a larger amount of power devices. This is summarized in in Tab. 4.2, where it is assumed that $V_{DC}'' = V_{DC}'/[2(n-1)]$. Therefore, a lower phase voltage THD is obtained with the same number of switches. As an example, a system adopting the proposed configuration and a three-level inverter, features a 17 levels phase voltage, as a standard five-level inverter (5LI), but requiring 18 power devices, instead of 24.

Tab. 4.2 Comparison between standard MLI and the MLI+2LI configuration.

MLI	**Standard MLI** *(NPC or FC)*		**MLI+2LI** $V_{DC}'' = V_{DC}'/[2(n-1)]$			
	Power Switches	**Phase voltage levels**	**Power Switches**			**Phase voltage levels**
			MLI	**2LI**	**MLI+2LI**	
3-L	***12***	***9***	*12*	*6*	***18***	***17***
5-L	***24***	***17***	*24*	*6*	***30***	***25***
7-L	***36***	***25***	*36*	*6*	***42***	***33***
9-L	***48***	***33***	*48*	*6*	***54***	***41***
n-L	***2p(n-1)***	***4(n-1)+1***	*2p(n-1)*	*2p*	***2p(n-1)+6***	***4(n+1)+1***

4.1.2 Low-frequency modulation in MLI

The main feature of the AHMLI is that the MLI exploits a conventional quarter-wave symmetric step modulation strategy, or low-frequency modulation, in order to minimize switching power losses. Differently, the TLI is PWM modulated.

As discussed in section 1.1.5, the amplitude of the staircase output phase voltage V_{MLI} is controlled by acting on *(n-1)/2* switching angles $\theta_1, \theta_2, ..., \theta_{(n-1)/2}$ ($0 \leq \theta_1 < \theta_2 < \theta_{(n-1)/2} \leq \pi/2$) [20], [21]-[22], as shown in Fig. 4. 6.

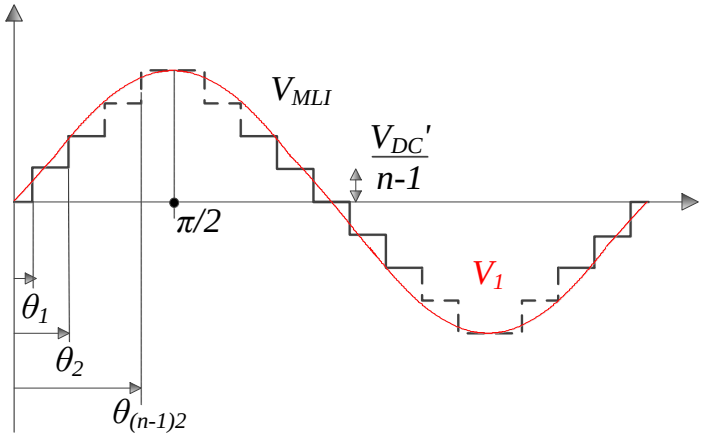


Fig. 4. 6 MLI staircase output phase voltage

By applying the Fourier series analysis, the amplitude of an odd harmonic of the stepped waveform can be expressed as:

$$V_n = \frac{4}{n\pi} \sum_{k=1}^{(n-1)/2} V_k \cos(n\,\theta_k) \tag{4.11}$$

where V_k is the k^{th} level of DC voltage, n is the (odd) harmonic order and θ_k is the k^{th} switching angle. More specifically, switching angles are selected in order to obtain the required fundamental voltage reference V_1, by eliminating from the harmonic content of the output voltage, *n-1* of the lowest odd, non-triple harmonics. Therefore, θ_1, θ_2,..., θ_m, are computed by solving the following set of *(n-1)/2* non-linear transcendental equations:

$$\begin{aligned} &\cos\theta_1 - \cos\theta_2 + ... + \cos\theta_{(n-1)/2} = m \\ &\cos 5\theta_1 - \cos 5\theta_2 + ... + \cos 5\theta_{(n-1)/2} = 0 \\ &..... \\ &\cos k\theta_1 - \cos k\theta_2 + ... + \cos k\theta_{(n-1)/2} = 0 \end{aligned} \tag{4.12}$$

where k is the order of the highest harmonic that has to be eliminated and m is the modulation index defined as:

$$m = \frac{\pi}{4} \frac{V^*}{V_{DC}'} \tag{4.13}$$

As an example, since a system adopting a three-level inverter exploits only one switching angle, this last is able to control the required fundamental voltage reference V_1, while suppressing a single undesired low order harmonic component. Eq. (4.12) becomes:

$$\cos\theta_1 = m \tag{4.14}$$

If the 5th harmonic component has to be eliminated, the switching angle should be set to $\theta_1=\pi/10$. Replacing this value into eq. (4.14), a 0.95 modulation index is obtained. Fig. 4. 7 shows the output phase voltage V_{MLI} for m= 0.95 and its harmonic spectrum, when the 5th-harmonic component is eliminated, while Fig. 4. 8 shows the same content for m=0.86, when the 3th-harmonic component is compensated. Fig. 4. 9 shows the switching angles as a function of the modulation index, for a 3LI and a 5LI. A minimum value of switching angles is chosen slightly greater than 0, in order to prevent the occurrence of overvoltage at the motor terminals.

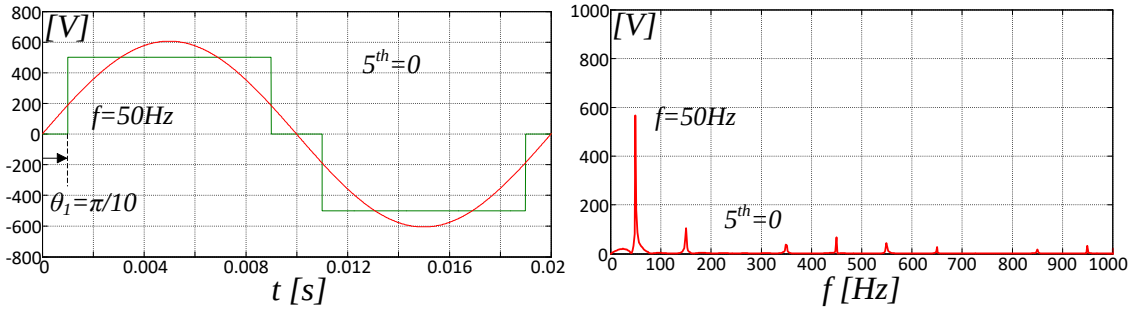


Fig. 4. 7 MLI staircase output phase voltage V_{MLI}(left). Harmonic spectrum of V_{MLI}, with 5th-harmonic component suppressed $\theta_1=\pi/10$, m=0.95

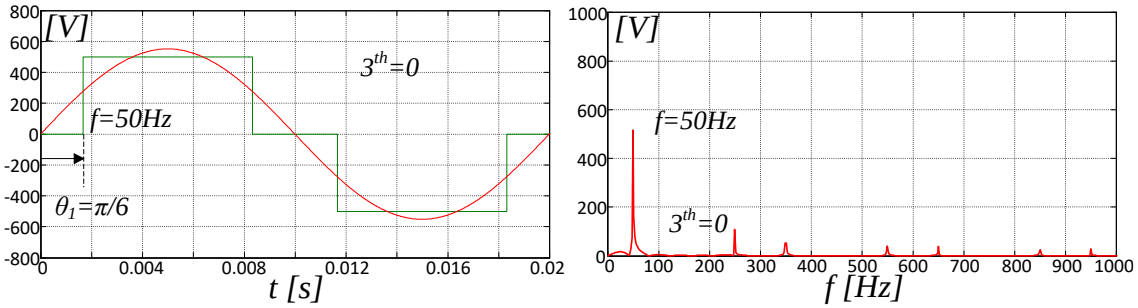


Fig. 4. 8 MLI staircase output phase voltage V_{MLI}(left). Harmonic spectrum of V_{MLI}, with 3th-harmonic component suppressed $\theta_1=\pi/6$, m=0.86

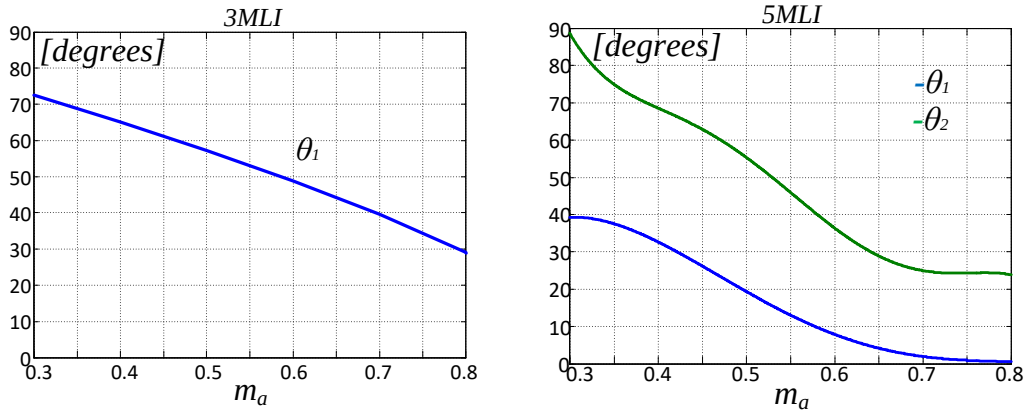


Fig. 4. 9 Switching angles vs. modulation index for a 3LI (left) and a 5LI (right).

4.1.3 Active harmonic elimination method

The MLI staircase output phase voltage V_{MLI} consists of the desired fundamental harmonic V^* and some odd, non-triple, harmonics V_j, as given by:

$$V_{MLI} = V^* + \sum V_j \qquad \text{j(odd, non - triple)} > \text{k} \tag{4.15}$$

Stator phase voltage harmonics are responsible of torque ripple and of additional (stray) power losses in the electrical machine and in the static converter. According to the proposed AHMLI configuration, the harmonic content of the machine phase voltage V_m is improved by exploiting the auxiliary PWM TLI. The resultant phase voltage V_m, in fact, is equal to the difference between the MLI staircase output phase voltage V_{MLI} and the phase output voltage V_{TLI} of the TLI.

In order to eliminate low-order voltage harmonics V_j, i.e. to obtain $V_m \approx V^*$, the reference voltage V_{TLI}^* of the two-level inverter must be set to:

$$V_{TLI}^* = \sum V_j / k_V = V_{MLI} - V^* \qquad \text{j(odd, non - triple)} > \text{k} \tag{4.16}$$

being k_v the TLI voltage gain. Actual values of staircase phase voltage V_{MLI} are computed according to eq. (4.1) as:

$$V_{MLI} = \frac{2l' - n + 1}{2(n-1)} V_{DC}'$$

$$\begin{cases} l' = 0 & \text{if } 0 \le \theta < \theta_1 \text{ or } 2\pi - \theta_1 \le \theta < 2\pi \\ l' = 1 & \text{if } \theta_1 \le \theta < \theta_2 \text{ or } 2\pi - \theta_2 \le \theta < 2\pi - \theta_1 \\ \\ l' = n-1 & \text{if } \theta_{(n-1)/2} \le \theta < \pi \text{ or } \pi \le \theta < 2\pi - \theta_{(n-1)/2} \end{cases} \tag{4.17}$$

Fig. 4. 10 shows the voltage control strategy developed to manage the two inverters. Since the auxiliary TLI works as an active power filter, it exchanges a zero-average power with the machine, thus, the DC-Bus supply can be realized by a floating capacitor. Hence, the voltage V_{DC}'' is ideally constant. However, inverter power losses cause a progressive discharge of the TLI DC-bus capacitor. Since the latter is floating, it can be charged only by establishing a controlled active power stream between the two inverters. Thus, an additional corrective term V_{cap} is then introduced into V_{TLI}^*, being the output of a closed loop V_{DC}'' regulator, as shown in Fig. 4. 10. Further insights on the V_{DC}'' control algorithm will be discussed in the following.

A generic *n*-level V_{MLI} waveform and the associated TLI reference voltage V_{TLI}* are shown in Fig. 4. 11. According to Fig. 4. 12, the auxiliary inverter needs a DC-Bus voltage $V_{DC}'' = V_{DC}'/[2(n-1)]$, to generate the required V_{TLI}^* waveform in the entire operating range of the drive; therefore, it can be equipped with power devices with half the rated voltage of those of the MLI. Moreover, by increasing the number of MLI voltage levels the required minimum value of V_{DC}'' is reduced.

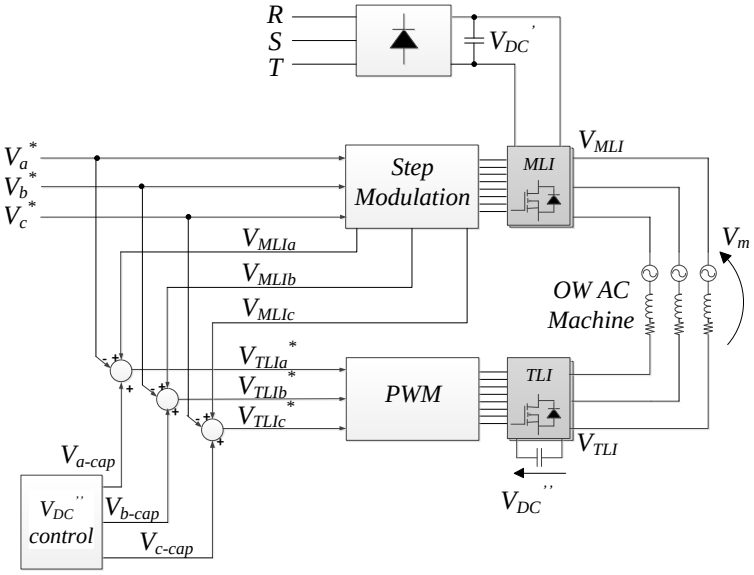


Fig. 4. 10 AHMLI voltage control scheme

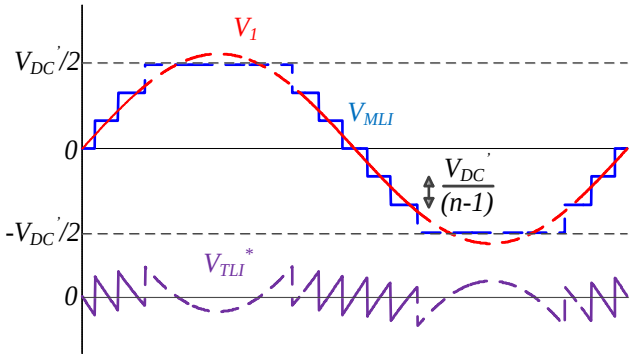


Fig. 4. 11 V_{MLI}, V_m and V_{TLI} waveforms.*

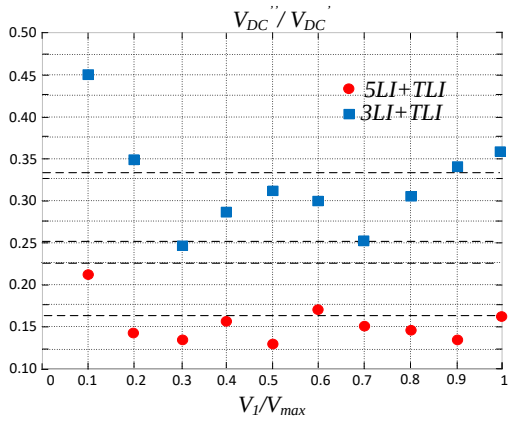


Fig. 4. 12 Fig. 7. Minimum V_{DC}'' amplitude vs. V_1 in case of 5LI+TLI and 3LI+TLI.

4.1.4 Simulation results of the harmonic suppression method: THD and Power Losses

In order to investigate the effectiveness of the method in improving the THD, the TLI DC-Bus voltage is initially considered as supplied by an ideal voltage generator. The TLI synthetizes the reference voltage V_{TLI}^{*} by exploiting an Adjacent State Space Vector Modulation strategy. As an example, an AHMLI composed of a 3LI and a PWM two-level inverter (3LI+TLI) switching at 5 kHz has been considered. According to Tab. 4.2 it includes in total 18 switches. The optima DC-Bus voltage of the TLI is set to $V_{DC}'' = V_{DC}'/4$.

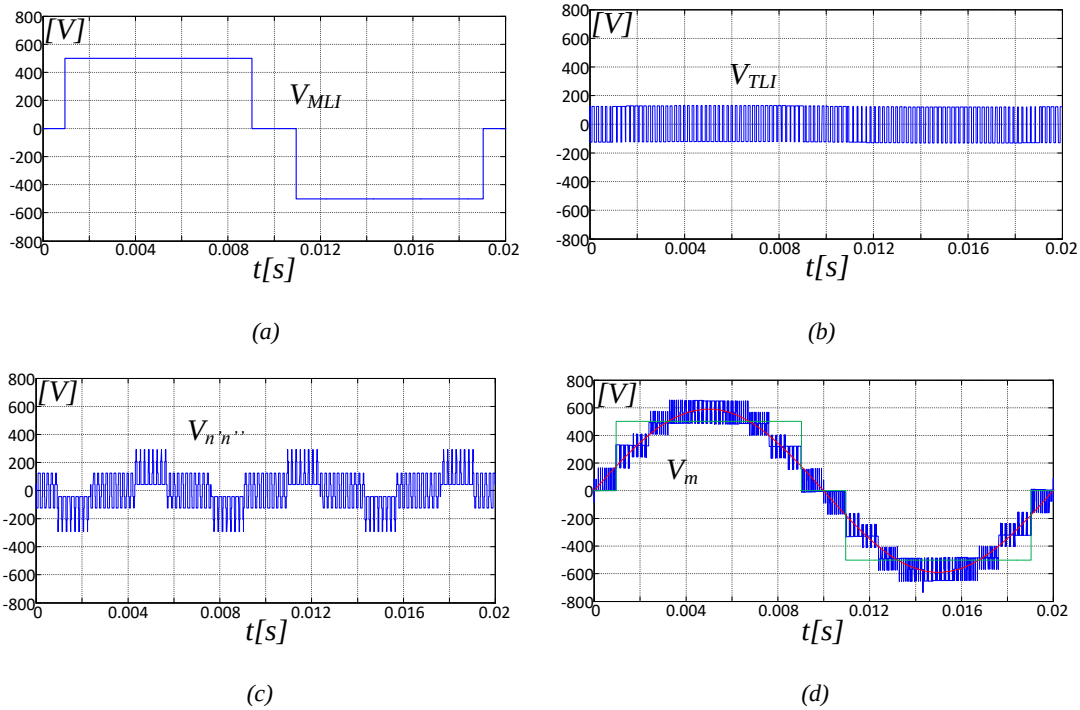


Fig. 4. 13. 3LI+TLI with $V_{DC}'' = V_{DC}'/4$*:* V_{MLI} *(a),* V_{TLI} *(b), differential-mode voltage* $V_{n'n''}$ *(c), motor phase voltage* V_m *(d).*

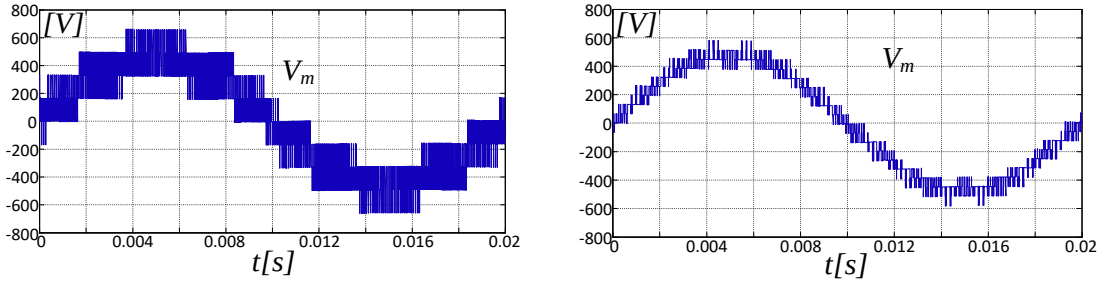


Fig. 4. 14. Motor phase voltage V_m*: three-level PWM inverter (left), five-level PWM inverter (right).*

Fig. 4. 13 shows 3LI and TLI output phase voltages, as well as the motor phase voltage V_m and the voltage across the midpoints of the two DC-buses $V_{n'n''}$, obtained for m=0.8. For the sake of comparison, motor phase voltages

generated by a five-level-24 switches inverter and a three-level-12 switches inverter, both PWM operated at 5 kHz, are shown in Fig. 4. 14.

Simulations of the three aforementioned topologies applied to an Open-end Winding AC Motor drive (OWMD), operating at 70% of the rated power with different values of the modulation index, have been accomplished. The voltage THD, up to the 90th harmonic, is given by:

$$THD = \frac{\sum_{i=2}^{90} V_i^2}{V_1} \tag{4.18}$$

where V_i represents the low-order voltage harmonics and V_1 is the fundamental phase voltage. Inverter power losses have been also estimated where the MLI is equipped with high-voltage IGBTs and the TLI exploits low-voltage high-frequency MOSFETs. Main technical specifications of the induction motor and switches are respectively summarized in Tab. 4.3, Tab. 4.4 and Tab. 4.5. The inverter power losses are calculated as the sum of the switching losses and conduction losses. The switching losses P_{sw} depend mainly on switching frequency f_{sw} and can be calculated as follow:

$$P_{SW} = \frac{1}{2} v_{CE} i_m f_{SW} \left(t_{ON} + t_{OFF}\right) \tag{4.19}$$

being t_{on}, t_{off} and v_{ce} switch parameters depicted in Tab. 4.3, Tab. 4.4, for IGBTs and MOSFETs respectively. In the contrary, the conduction losses are differently evaluated for IGBTs and MOSFETs. The IGBTs conduction losses are given by:

$$P_{C\_IGBT} = v_{ON} i_{ON} \delta \tag{4.20}$$

where V_{on} and i_{on} are the voltage across the switches during the on-state and the current that is passing thought it, respectively, while δ is the duty cycle. Unlike IGBTs, the MOSFETs conduction losses depend on the Drain-Source On-State Resistance $R_{DS(on)}$:

$$P_{C\_MOSF} = R_{DS} i_{ON}^{\ 2} \tag{4.21}$$

Hence, the total inverter power losses are given by:

$$P_{INV} = P_{SW} + P_C \tag{4.22}$$

The voltage THD and the estimated inverter power losses, are shown in Fig. 4. 15. The 3LI+TLI configuration features a THD fairly equivalent to that of a conventional 5-level NPC inverter operating at the same switching frequency (5 kHz), and requires only 75% of the power devices. Moreover, cumulative power losses of the

3LI+TLI configuration are remarkably lower than those of a 5-level PWM inverter and only slightly higher than those of a 3-level PWM inverter. Advantages in exploiting the proposed approach are also clear in Fig. 4. 16, dealing with a comparison in terms of THD and power losses among a 5LI+TLI configuration, a step operated five-level NPC inverter, a five level PWM NPC inverter and a seven-level PWM NPC inverter.

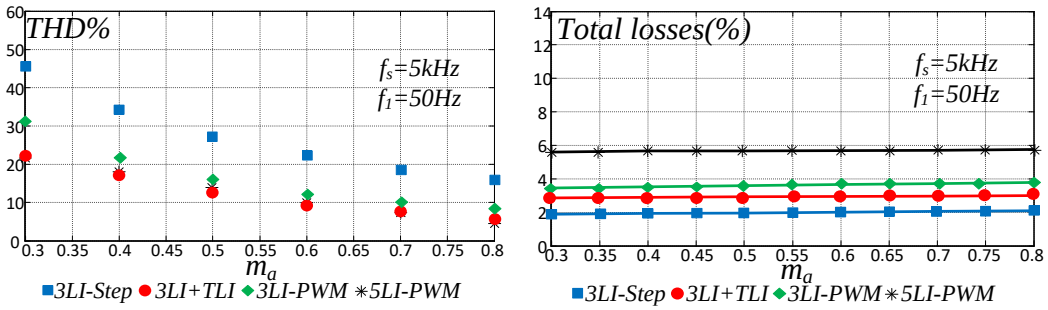


Fig. 4. 15 3MLI: THDv to the 90th harmonic (left) and estimated inverter power losses (right) at 70% of the rated power.

Tab. 4.3 Induction Machine data.

P_n [kW]	I_n [A]	R_s [Ω]	R_r [Ω]	L_{ls} [H]	L_{lr} [H]	L_m [H]	n [g/min]
2	5	9.2	7.24	0.025	0.025	0.535	1500

Tab. 4.4 F3L150R07W2E3 IGBT data.

T_j [C°]	v_{ceo} [V]	r_{ce} [mΩ]	v_{feo} [mΩ]	r_{fe} [mΩ]	t_{ont} [ns]	t_{offT} [ns]	t_{offD} [ns]
150	0.75	6.3	0.9	3.8	60	131	53

Tab. 4.5 TH40J60U MOSFET data.

R_{DS} [Ω]	V_{DS} [V]	t_{offT} [ns]	t_{offD} [ns]
0.065	3	180	173

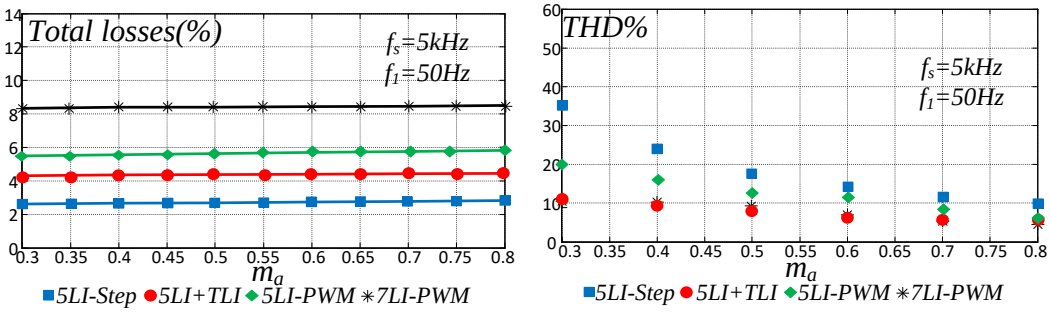


Fig. 4. 16 5MLI: THDv to the 90th harmonic (left) and estimated inverter power losses (right) at 70% of the rated power.

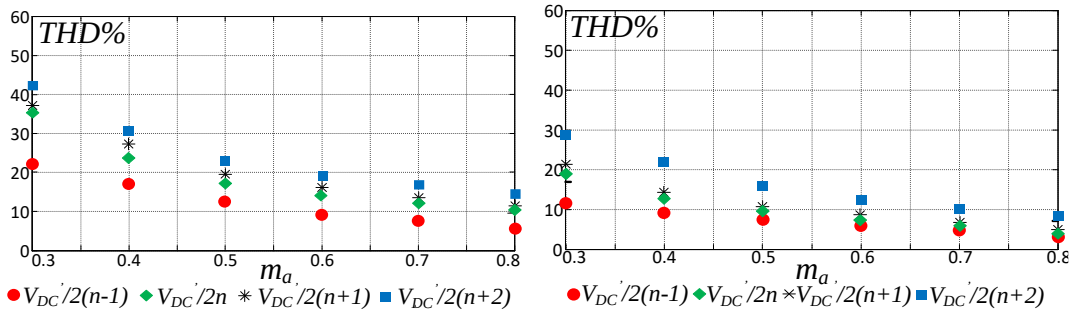


Fig. 4. 17 THD vs. m for 3LI+TLI (left) and 5LI+TLI (right), when reducing V_{DC}''.

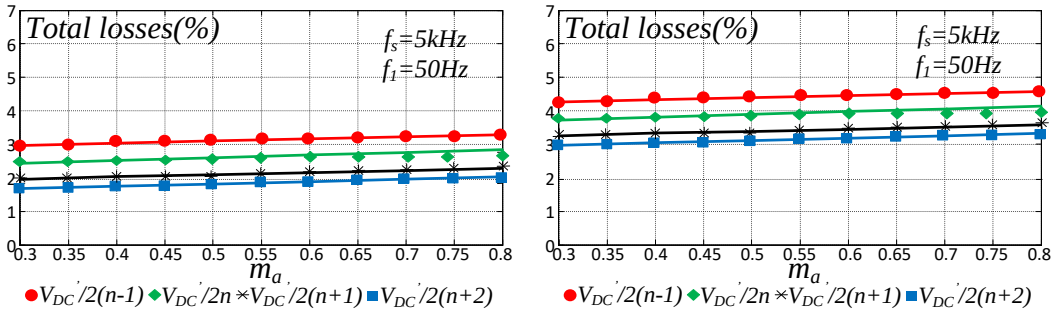


Fig. 4. 18 Average power losses at 70% of the rated power vs. m for 3LI+TLI (up) and 5LI+TLI (down), when reducing V_{DC}''.

According to the proposed configuration, the auxiliary TLI theoretically requires a $V_{DC}''=V_{DC}'/[2(n-1)]$ DC input voltage to generate the V_{TLI}* waveform. However, V_{DC}'' can be further reduced in an effort to achieve an optimal trade-off between the TLI switches voltage ratings and switching power losses on one hand and the motor phase voltage THD on the other hand. As shown in Fig. 4. 17 and Fig. 4. 18, a progressive worsening of the THD and power losses is observed when V_{DC}'' is reduced. Obtained results can be improved by equipping the TLI with fast switching IGBTs, or by exploiting optimized PWM techniques. Fig. 4. 19 depicts the effectiveness of the proposed method on the current harmonic content, when V_{DC}'' is set to optimal value $V_{DC}'/[2(n-1)]$, for a 3LI+MLI feeding an induction motor with open loop *V/f* control algorithm.

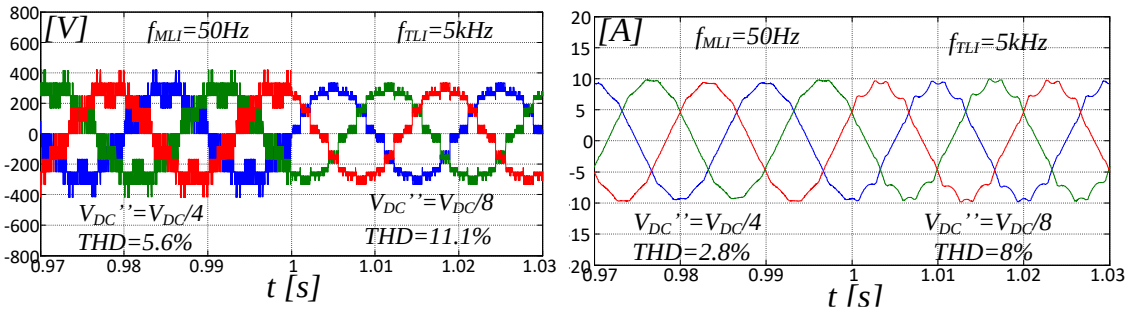


Fig. 4. 19 AHMLI phase voltage V_{abcm} for 3LI+TLI (left) and phase currents i_{abcm} (right), when reducing V_{DC}'' from $V_{DC}'/4$ to $V_{DC}'/8$

Fig. 4. 20 shows the same results using a 5LI+MLI. To highlight the effectiveness of the proposed method in term of improving of current harmonic content, when V_{DC}'' is set to optimal value $V_{DC}'/[2(n-1)]$. The improvement is obtained thank to the higher number of voltage levels, as discussed in section 4.1.1. The 3LI+TLI, in fact, works as a six-level inverter when $V_{DC}'' = V_{DC}'/[2(n-1)]$ featuring 17 output phase voltage levels. The 5LI+TLI, instead, works as a ten-level inverter featuring 25 output phase voltage levels.

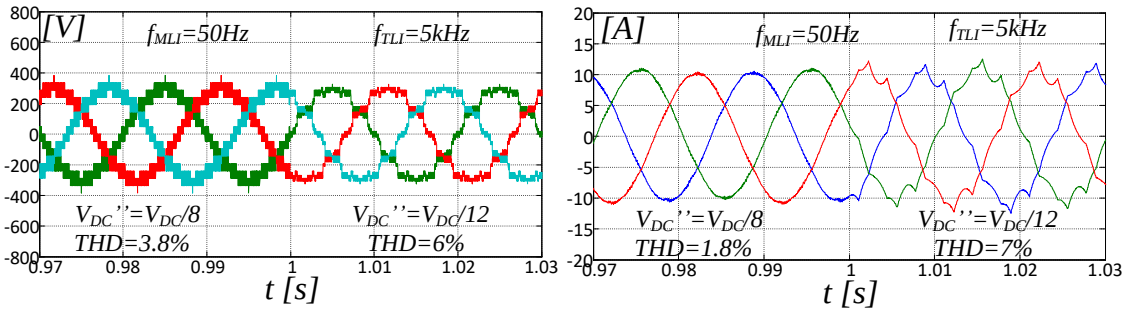


Fig. 4. 20 AHMLI phase voltage V_{abcm} for 5LI+TLI (left) and phase currents i_{abcm} (right), when reducing V_{DC}'' from $V_{DC}'/8$ to $V_{DC}'/12$

4.1.4.1 TLI DC-Bus voltage control algorithm

As mentioned earlier, since the TLI works as active power filter, it provides zero average active power to the machine. Thus, it can be supplied by a floating capacitor. However, while V_{DC}'' is ideally constant, in practice inverter power losses P_L cause a progressive discharge of the TLI DC-bus capacitor, as depicted in Fig. 4. 21.

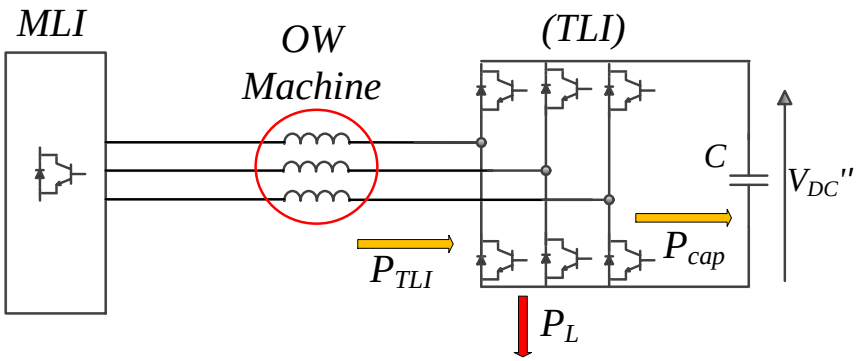


Fig. 4. 21 Contribution of the Inverter power losses P_L *in discharging the TLI DC-bus capacitor*

Since the capacitor is floating, it can be charged only by establishing a controlled active power stream between the two inverters. Two main capacitor voltage control techniques are available in the literature. The first uses a PI DC-Bus capacitor voltage control, as shown in Fig. 4. 22. The output signal *K* of the PI controller represents the amount of active power required by the capacitor *C* in in order to keep the DC-Bus voltage constant at $V_{DC}''^{*}$. The

term K is multiplied for the MLI reference three-phase voltages V_{MLIa}, $V_{MLIb,}$ V_{MLIc} in order to obtain the synchronized additional corrective terms $V_{a\text{-}cap}$, $V_{b\text{-}cap}$ and $V_{c\text{-}cap}$. Fig. 4. 23 shows the DC-Bus voltage $V_{DC}{}''$ when exploiting the algorithm of Fig. 4. 22.

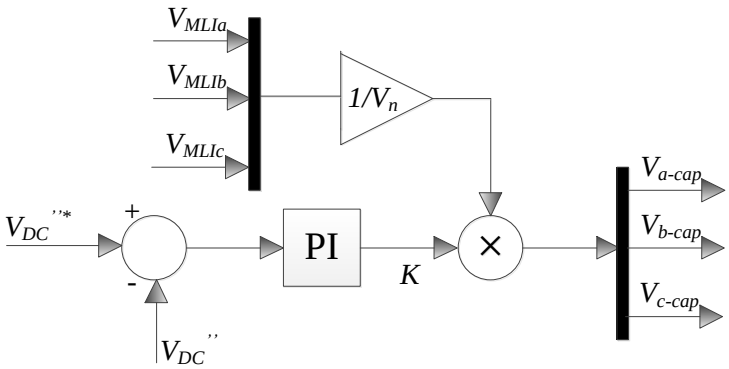


Fig. 4. 22 TLI DC-Bus voltage control algorithm

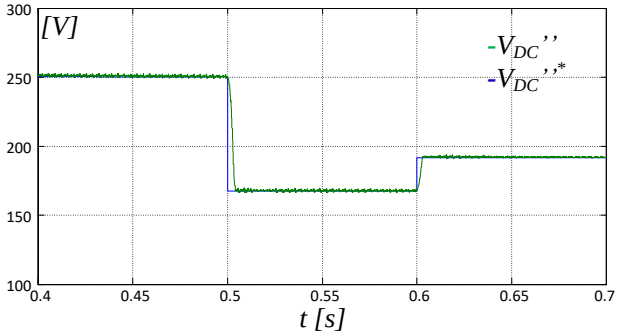


Fig. 4. 23 DC-Bus voltage $V_{DC}{}''$

The second approach exploits a qd0 transformation. Fig. 4. 24 shows the $V_{DC}{}''$ qd0 control scheme, where θ_e is the transformation angle and i_q and i_d are the qd components of the phase current of the machine. Hence, also in this case, additional corrective terms $V_{a\text{-}cap}$, $V_{b\text{-}cap}$ and $V_{c\text{-}cap}$, are introduced into the generic TLI reference voltage to hold the TLI DC-Bus voltage at a specified level. The reactive power is forced to zero by setting:

$$Q = \frac{3}{2}\left(i_q V_{dc} - i_d V_{qc}\right) \tag{4.23}$$

From eq. (4.22), the d-axis voltage component V_{dc} is obtained:

$$V_{dc} = \frac{i_d}{i_q} V_{qc} \tag{4.24}$$

The active power component P is determined as the output of a DC-Bus capacitor voltage controller, resulting in a q-axis voltage component $V_{qc.}$ Fig. 4. 25 shows the DC-Bus voltage $V_{DC}{}''$ variation. Note, that the qd0 control approach is dynamically faster than first technique.

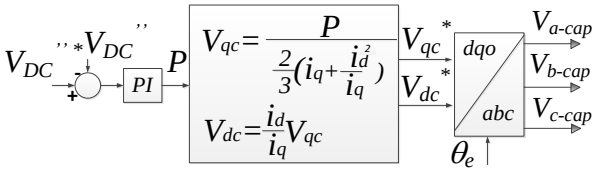


Fig. 4. 24 qd0 DC-Bus voltage V_{DC}'' control loop

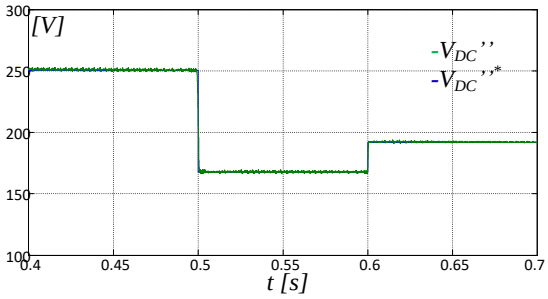


Fig. 4. 25 DC-Bus voltage V_{DC}'' controlled with qd0 approach

The reference voltage V_{TLI}^* of the TLI, then becomes:

$$V_{TLI}^{*} = V_{MLI} - V^{*} + V_{CAP} \quad j(odd,\ non\text{-}triple) > K \tag{4.25}$$

4.1.4.2 MLI DC-Bus Capacitor Voltage Balance techniques

A key issue of any NPC MLI topology relies in DC-link capacitors voltage balance. In order to overcome such a drawback, different solutions can be adopted. PWM switching patterns can be superimposed to the staircase modulation in order to exploit redundant power converter states [23]. This solution however causes additional power losses. A further solution exploits a transformer with multiple outputs. Each output is cascade connected to a three-phase a rectifier in order to obtain *n* isolated DC-power sources [24]. A voltage balance among MLI input capacitors can be required also for other reasons. On photovoltaic generators, in fact, MLIs are supplied by *n* isolated DC-Buses obtained by suitably partitioning PV strings split, a similar situation occurs also on hybrid/electric vehicles, where MLIs are supplied by series connected storage units [24]. The proposed AHMLI topology allows to balance the DC-link capacitors by acting on the active power transferred to the floating capacitor of the TLI, as depicted in Fig. 4. 26. In particular, on a three-level inverter, the two averaged DC-link capacitor voltages V_{c1} and V_{c2} are kept constant by increasing the output active power of an additional term ΔP whenever $V_{c1} > V_{c2}$, while setting $\Delta P = 0$ if $V_{c1} < V_{c2}$.

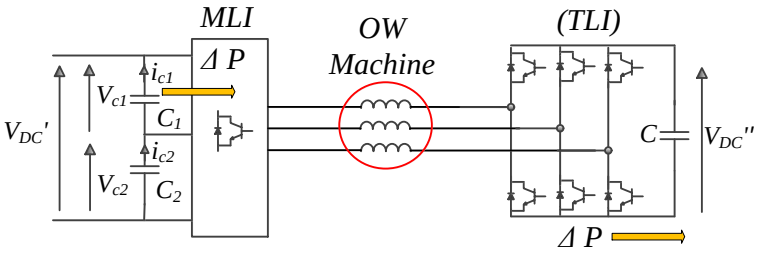


Fig. 4. 26 AHMLI with 3LI+TLI: MLI capacitor voltage balancing approach

In this way, additional corrective terms $V_{a\text{-}c1}$, $V_{b\text{-}c1}$ and $V_{c\text{-}c1}$, are introduced into the TLI reference voltage:

$$V_{TLI}^{*} = V_{MLI}^{*} - V_{cap} + V_{c1}\ \mathrm{j(odd,\ \ non\ -\ triple) > k} \tag{4.26}$$

Hence, the AHMLI voltage control scheme of Fig. 4. 10 becomes that of Fig. 4. 27. Fig. 4. 28 MLI DC Bus voltage balance: a) DC-Bus voltage VDC''. *b*) capacitor voltages Vc1 *and* Vc2. *c*) phase voltages Vabcm. d) phase currents iabcm. The balancing algorithm is active for t<1s, where the voltage V_{c1} and V_{c2} are kept constant, and is unactive for t>1s, where C_1 is charging and C_2 is discharging. As depicted in Fig. 4. 29, the modulation of V_{DC}'' causes the circulation of a zero-average current on each capacitor.

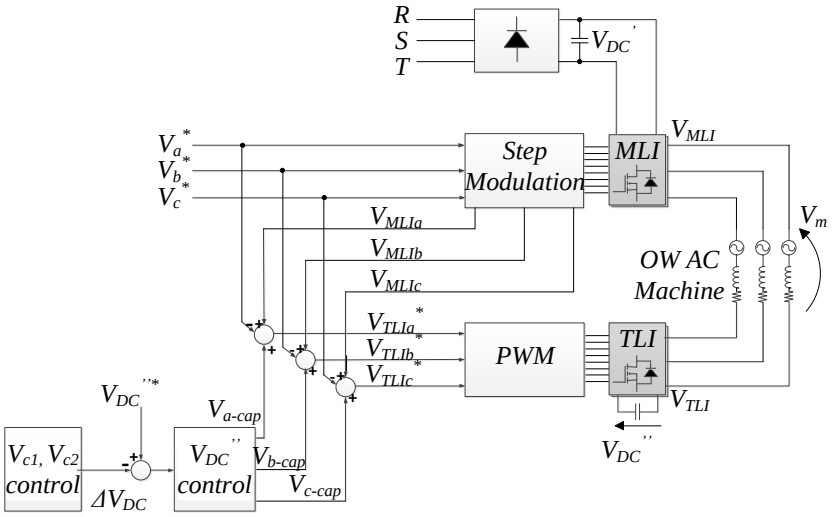


Fig. 4. 27 AHMLI voltage control scheme with DC-Bus voltage balancing method of the MLI

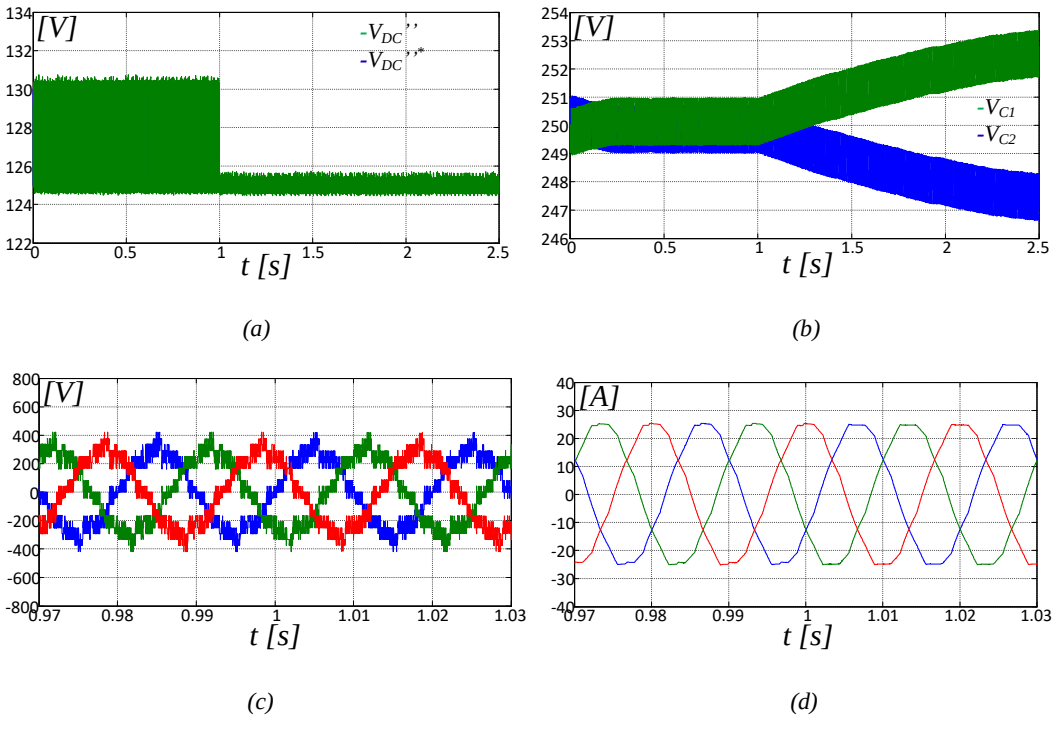


Fig. 4. 28 MLI DC Bus voltage balance: a) DC-Bus voltage V_{DC}''. b) capacitor voltages V_{c1} and V_{c2}. c) phase voltages V_{abcm}. d) phase currents i_{abcm}

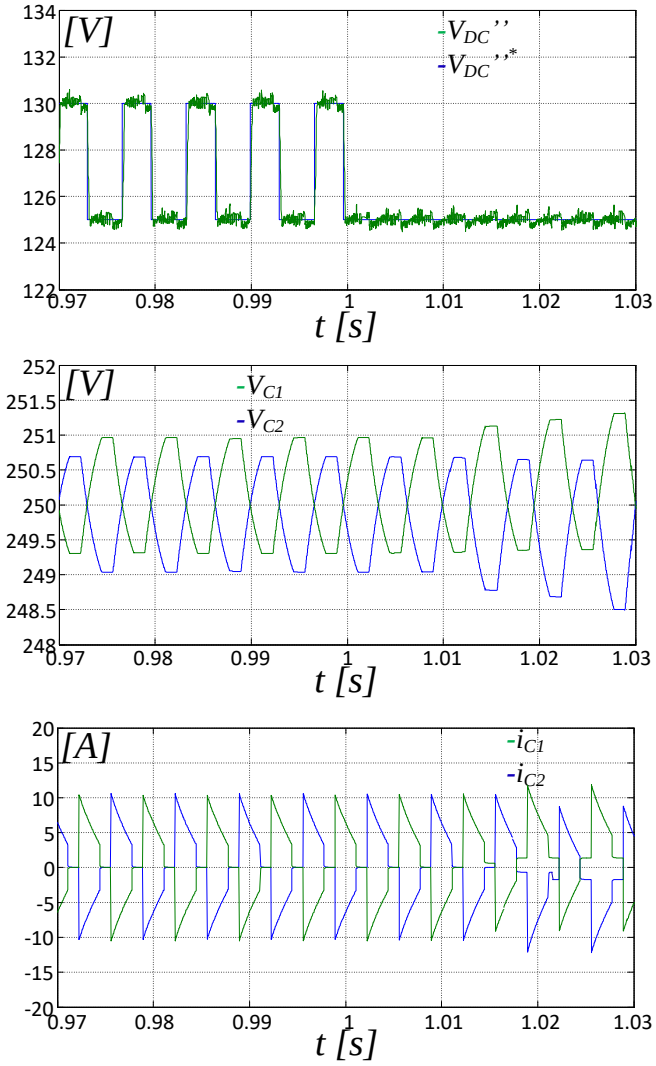


Fig. 4. 29 MLI DC Bus voltage balance: up) DC-Bus voltage V_{DC}''. middle) capacitor voltages V_{c1} and V_{c2}. down) capacitor currents i_{c1} and i_{c2}

4.1.5 Experimental results on AHMLI AC Motor Drives: V/f control

An experimental validation of the application of the AHMLI concept in constant *V/f* induction motor drive applications has been accomplished. The aim is that to verify the effectiveness of the proposed harmonic compensation method in terms of THD reduction and efficiency improvement. Fig. 4. 30 depicts the experimental setup. The prototype has been tailored around a standard 3.7 kW, three-phase, 4 poles IM featuring: V_n=400V, f_n=50Hz and i_n=8.6A. Another 4 poles, 5.5 kW three-phase IM, rated at: V_n=400V, f_n=50Hz and i_n =12.5A provided the load torque, ranging from 30% to 100% of the rated value. The MLI DC-Bus voltage is set to 500V. Technical specifications of motor and power switches are shown in Table. 4.3, Table 4.4 and Table 4.5. The AHMLI AC Motor

Drive prototype has been tested using either a three-level inverter (3LI), either a five-level inverter (5LI) NPC as main unit. The switching frequency of the active power filter is set to 10kHz with a dead time of 1μs. Both the main and auxiliary inverters are controlled through a dSpace 1103 development control board, while the voltage across each MLI DC-Bus capacitor is kept constant by a suitable actively controlled power supply system. Furthermore, a FPGA control board has been exploited to implement the PWM at 10kHz.

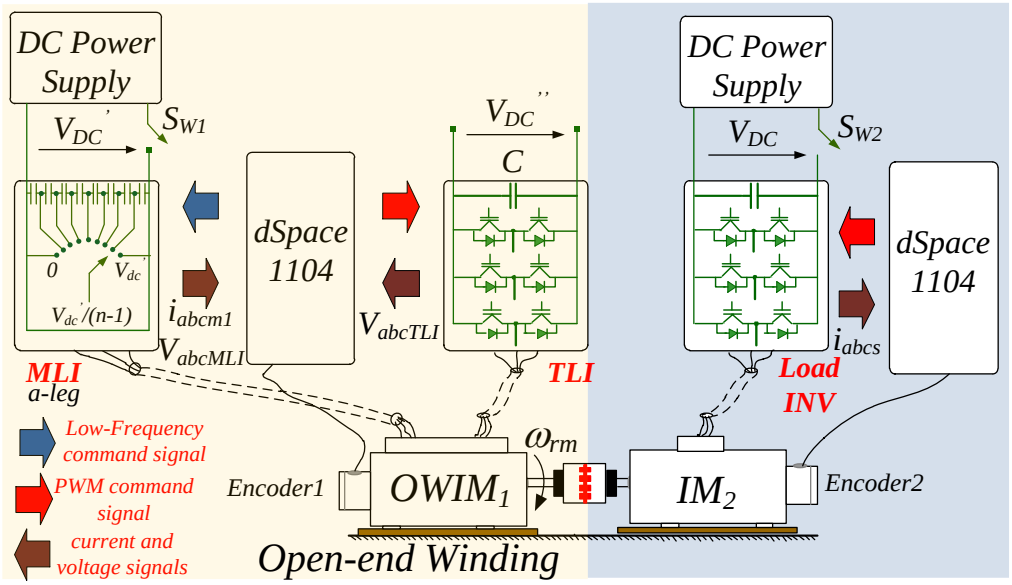
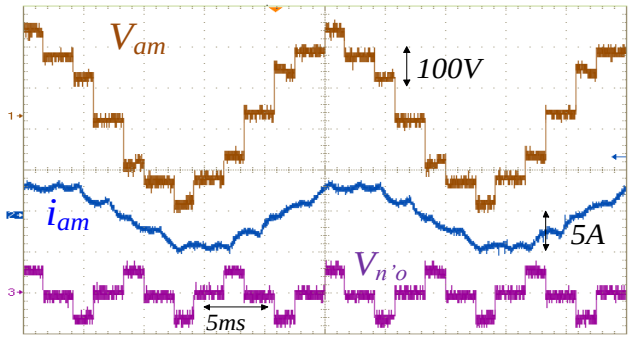


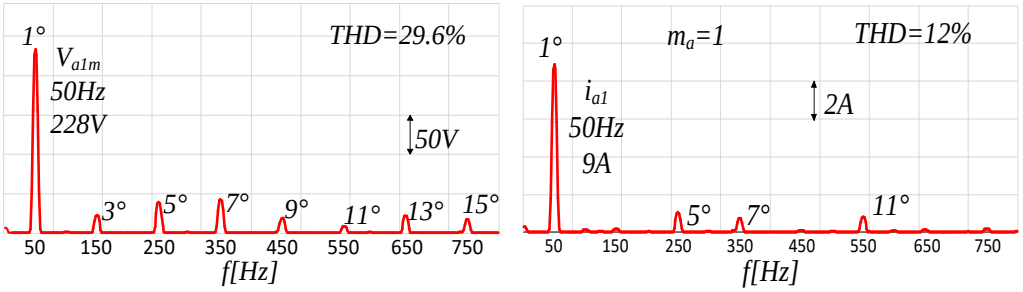
Fig. 4. 30 Experimental setup for AHMLI AC Motor Drive

The behavior of the motor with a classical wye connection and supplied by conventional 3LI and 5LI using a step voltage modulation technique was initially evaluated. In particular, Fig. 4. 31a shows the phase current i_a, the phase voltage V_m and the voltage $V_{n'o}$ (see Fig. 4. 4) between the motor neutral point and the mid-point of the DC-Bus, at 50% of the rated load torque when a 3LI is adopted. Voltage and current frequency spectra are displayed in Fig. 4. 31b and Fig. 4. 31c. At half load, with modulation index m_a=1, the obtained voltage THD is 29% using a 3LI, while the current THD is 12%. At the same way, Fig. 4. 32a shows the phase current i_a, the phase voltage V_m and the voltage $V_{n'o}$, when a 5LI is adopted. Voltage and current frequency spectra are displayed in Fig. 4. 32b and Fig. 4. 32c. In the two cases the voltage THD is 29% and 11%, while the current THD is 12% and 9.2%. The two MLIs have been also PWM operated at fs=10 kHz, under the same conditions, giving the results shown in Fig. 4. 33 and Fig. 4. 34. The voltage and current THD are better when compared with those obtained with voltage step modulation, because in the last case, only few low-order harmonics are cancelled. The proposed AHMLI configuration has been finally adopted, exploiting the 3LI+TLI and the 5LI+TLI configurations, giving the results shown in Fig. 4. 35 and Fig. 4. 36, respectively. According to the AHMLI approach, the value of V_{DC}'' is set to

$V_{DC}'/[2(n-1)]$, $V_{DC}'/4$ and $V_{DC}'/8$ for a 3LI+TLI and 5LI+TLI configurations, respectively. As it is possible to observe, the voltage THD decreases up to 4.4% with the first configuration and up

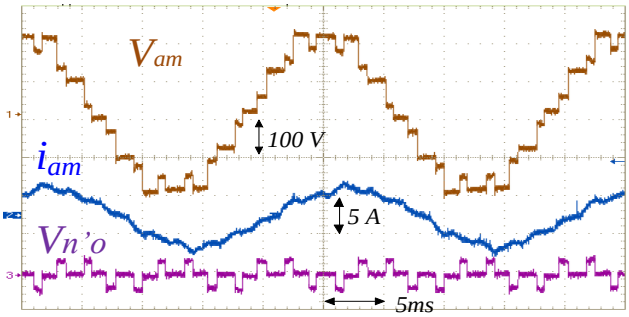


(a)

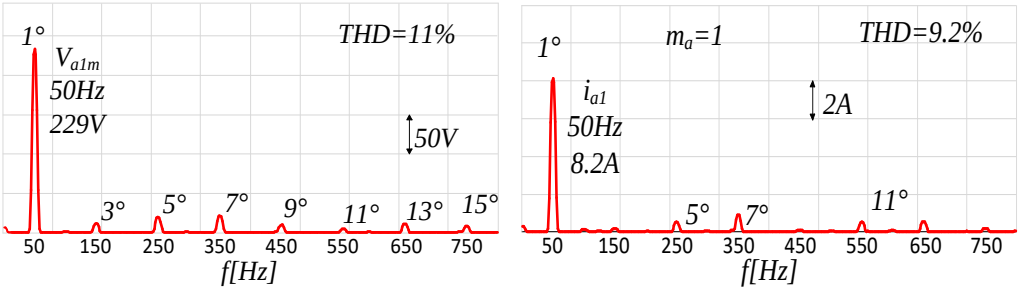


(b) (c)

Fig. 4. 31 3LI with Step modulation at 50% of rated load: (a) i_a, V_m and $V_{n'o}$;(b) V_m. harmonic spectrum; (c) i_a harmonic spectrum

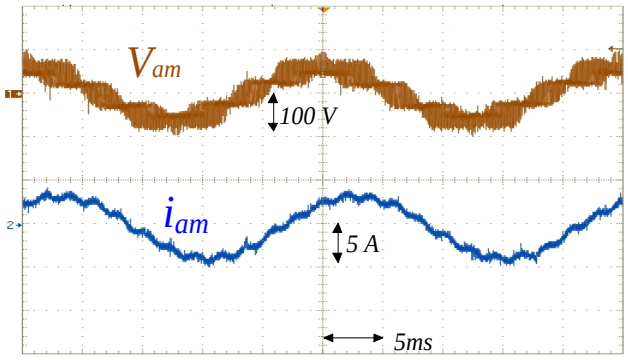


(a)



(b) (c)

Fig. 4. 32 5LI with Step modulation at 50% of rated load: (a) i_a, V_m and $V_{n'o}$;(b) V_m. harmonic spectrum; (c) i_a harmonic spectrum



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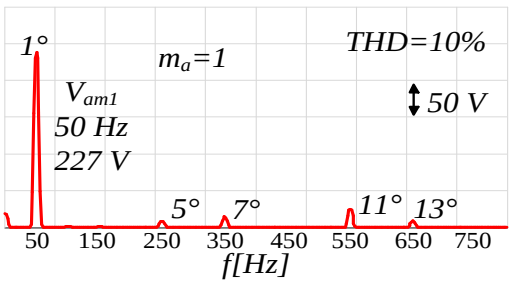

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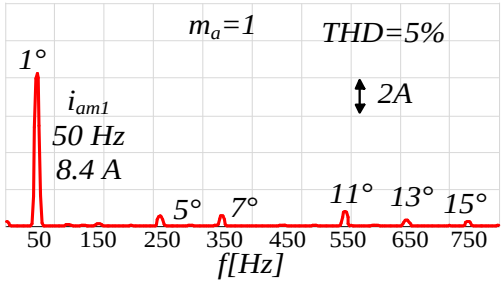
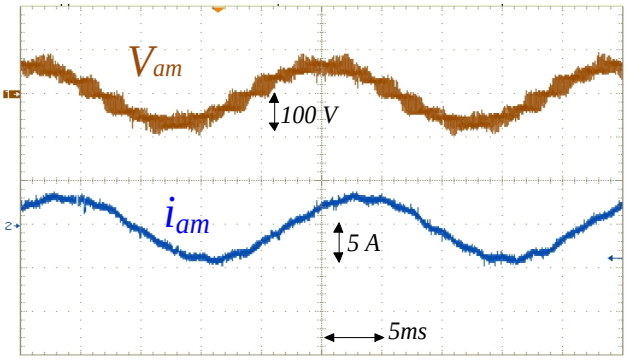
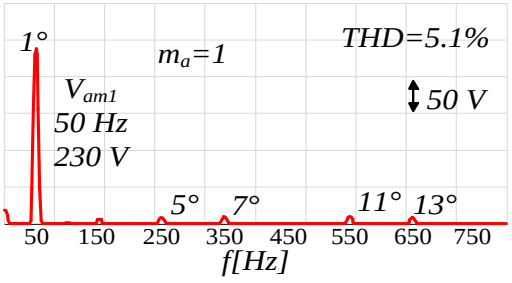


(c)

Fig. 4. 33 3LI with PWM (fs=10kHz) at 50% of rated load: (a) i_a, V_m;(b) V_m harmonic spectrum; (c) i_a harmonic spectrum



(a)



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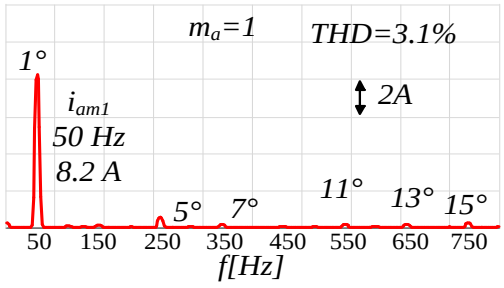


(c)

Fig. 4. 34 5LI with PWM (fs=10kHz) at 50% of rated load: (a) i_a, V_m;(b) V_m harmonic spectrum; (c) i_a harmonic spectrum

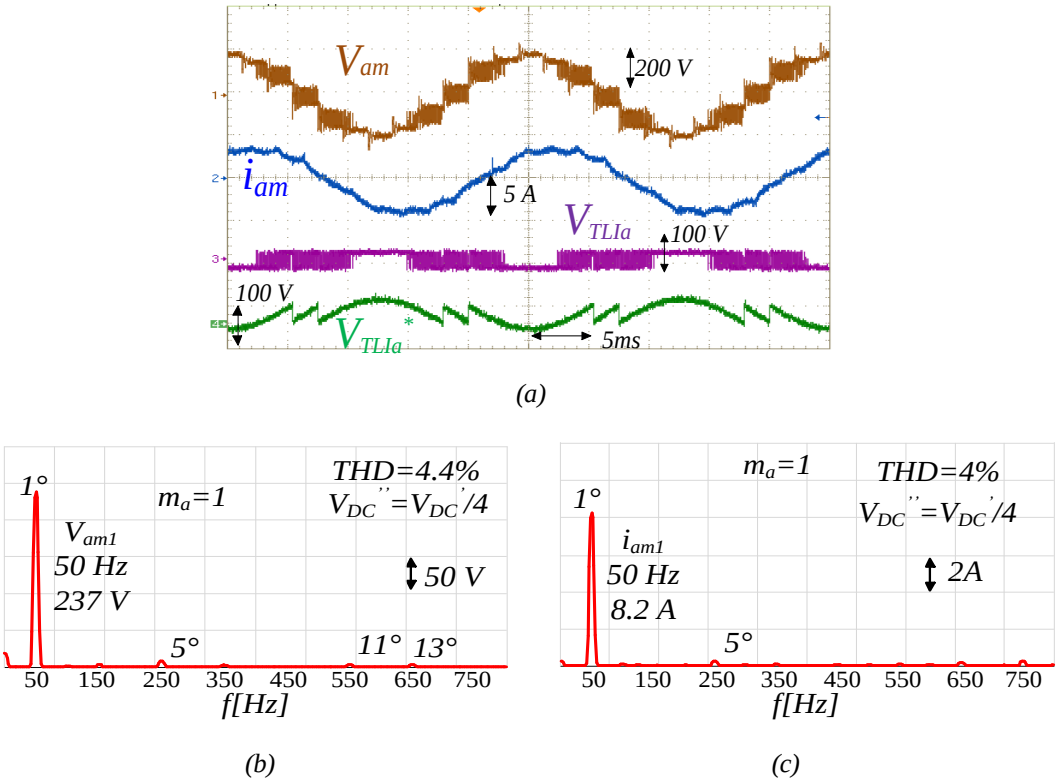


Fig. 4. 35 3LI+TLI with TLI PWM modulated (fs=10kHz) at 50% of rated load: (a) i_a, V_m and V_{TLI};(b) V_m harmonic spectrum; (c) i_a harmonic spectrum.*

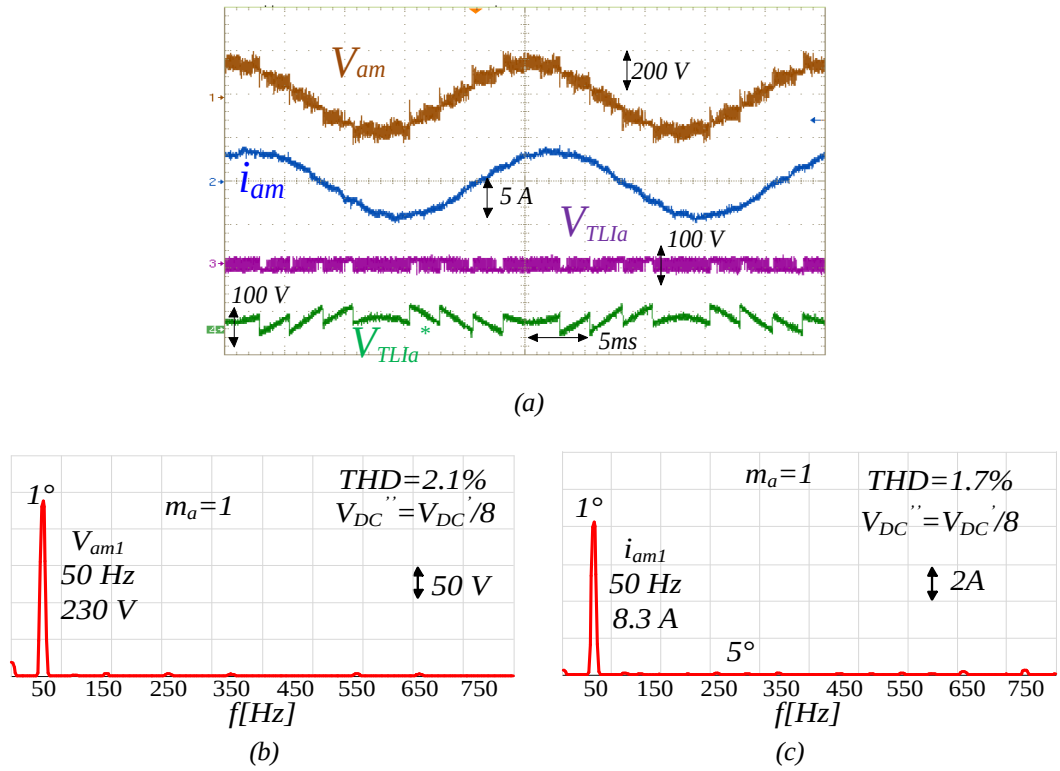


Fig. 4. 36 5LI+TLI with TLI PWM modulated (fs=10kHz) at 50% of rated load: (a) i_a, V_m and V_{TLI};(b) V_m harmonic spectrum; (c) i_a harmonic spectrum.*

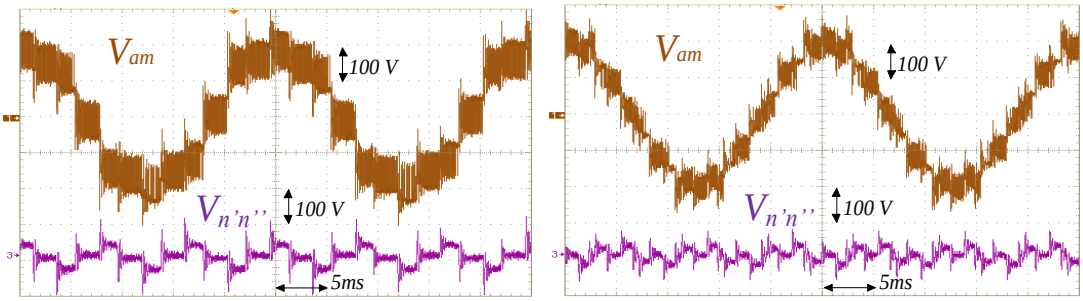


Fig. 4. 37 V_m and $V_{n'n''}$ at 50% of rated load: (left) 3LI+TLI; (right) 5LI+TLI.

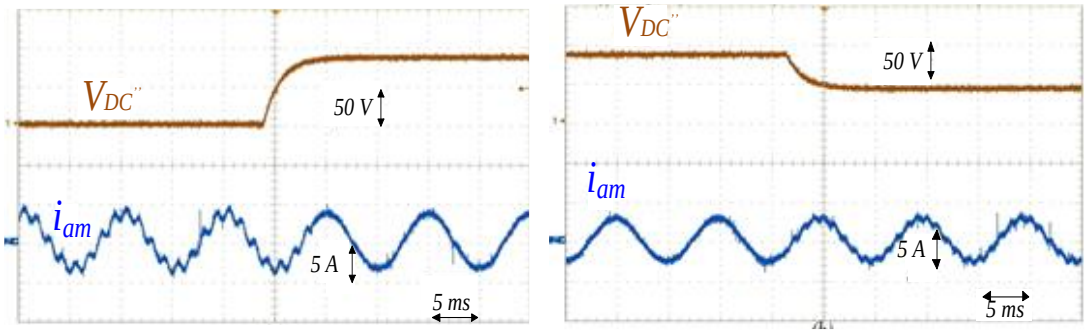


Fig. 4. 38 3LI+2LI, Capacity Voltage Control V_{DC}''. V_{DC}'' from 0V to 80V and phase current i_m (a). V_{DC}'' from 80V to 50V and phase current i_m (b)...

to 2.1% with the second, while the current THD is 4% in the first case and 1.7% in the second one. The voltage between the mid-points of the two DC Buses (see Fig. 4. 3) on 3LI+TLI and 5LI+TLI systems are also displayed in Fig. 4. 37. Fig. 4. 38 shows the effect of a DC-Bus voltage V_{DC}'' variation on the motor phase currents exploiting the capacitor voltage control discussed in the section 4.1.4.1. It is worth noting that, when the drive is operated with a V_{DC}'' lower than $V_{DC}'/[2(n-1)]$ a distortion is present in the motor current waveform. The voltage and current THD have been measured by exploiting a power analyzer in order to compare the experimental results with simulation results shown in Fig. 4. 15, Fig. 4. 16, Fig. 4. 17 and Fig. 4. 18. Fig. 4. 39 and Fig. 4. 40 refer to the phase voltage THD up to the 90th harmonic as measured on 3LI and 5LI as function of the modulation index, in case of wye-connected stator windings.

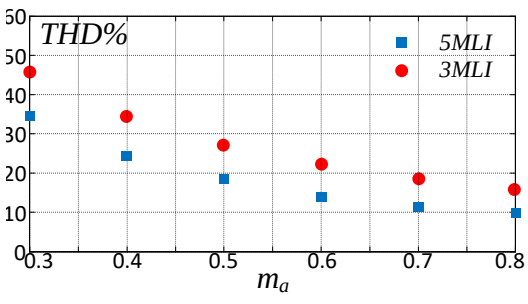


Fig. 4. 39 Phase voltage THD for 3LI and 5LI with Step Modulation.

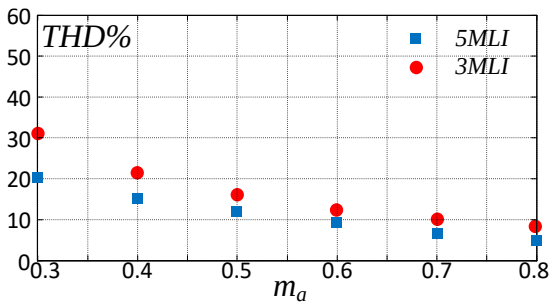
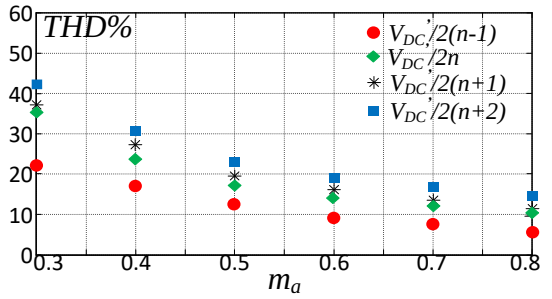
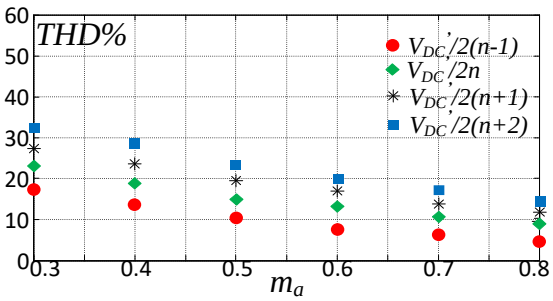


Fig. 4. 40 Phase voltage THD for 3LI and 5LI with sine PWM (fs=10kHz).

Both Staircase Vector Modulation and sine PWM techniques are considered for comparison. Results obtained with the 3LI+TLI and 5LI+TLI configurations with different values of V_{DC}'' are shown in Fig. 4. 41 and Fig. 4. 42. As predicted by simulations, a remarkable THD improvement is obtained in any operating condition.

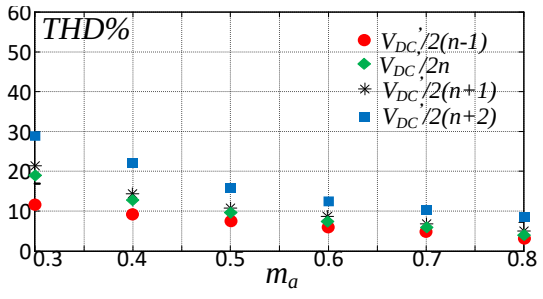


(a)

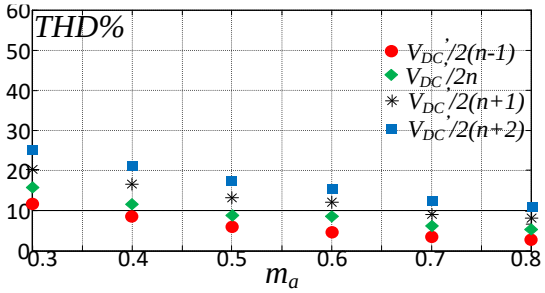


(b)

Fig. 4. 41 3LI+TLI (fs=10kHz): (a) phase voltage THD, (b) phase current THD.



(a)



(b)

Fig. 4. 42 5LI+TLI (fs=10kHz): (a) phase voltage THD, (b) phase current THD.

4.1.6 AHMLI Motor Drive Efficiency

The total system efficiency η_{tot}, the motor efficiency η_{mot} and the power conversion efficiency η_{conv} have been experimentally measured for various load torque levels T_L, taking into account the six of the above-considered configurations, namely:

- 3LI Step Modulated
- 5LI Step Modulated
- 3LI PWM Modulated
- 5LI PWM Modulated
- 3LI+TLI Hybrid
- 5LI+TLI Hybrid

Fig. 4. 43 shows the conceptual block scheme for measuring η_{tot}, η_{mot} and η_{conv}.

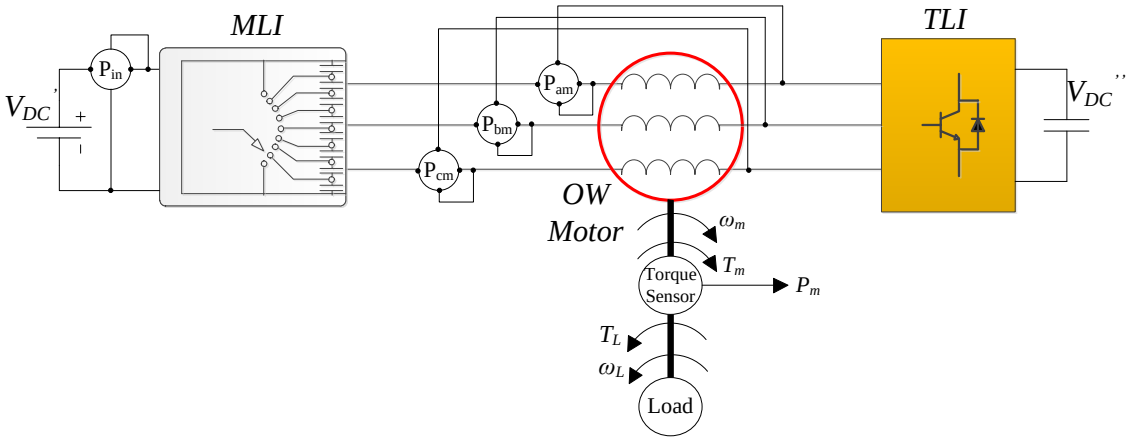


Fig. 4. 43 Experimental setup for measuring system efficiency

The total drive efficiency η_{tot}, is evaluated as the ratio between the motor output mechanical power P_m, measured with a torque sensor situated between the mechanical load and the OW motor, and the system input electrical power P_{in}, measured with a power analyzer. The motor efficiency η_{mot}, is given by the ratio between the output mechanical power P_m and the motor input electrical power P_{inm}, obtained by the sum of motor input powers measured on each phase winding P_{am}, P_{bm} and P_{cm}. TLI switching losses are included with switching losses measured at the system input. Hence, the converter efficiency η_{conv} is given by the ratio between the motor input electric power P_{inm} and the system input electric power P_{in}. **Errore. L'origine riferimento non è stata trovata.** and Fig. 4. 45 shows the power converter efficiency, motor efficiency and total efficiency for the six considered configurations.

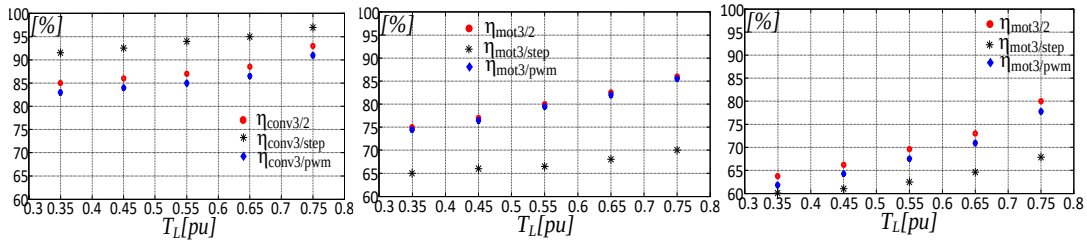


Fig. 4. 44 3LI: Power converter efficiency $\eta_{conv.}$(left); motor efficiency η_{mot} (mid); total system efficiency η_{tot} (right)..

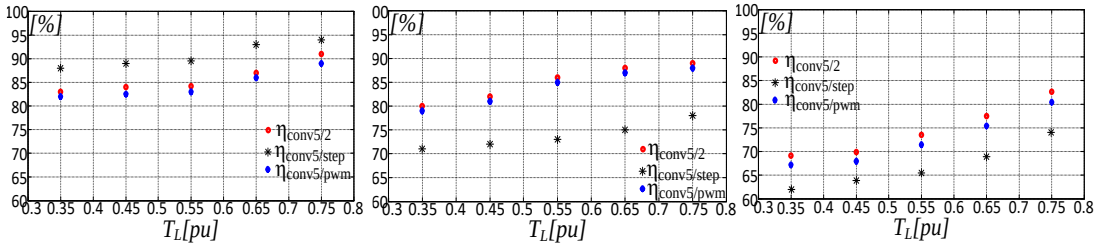


Fig. 4. 45 5LI: Power converter efficiency $\eta_{conv.}$(left); motor efficiency η_{mot} (mid); total system efficiency η_{tot} (right)

Note that the best power converter efficiency is given by step modulated MLI configurations. On the other hands, they also feature the worst motor efficiency, due to low-order current harmonic components. It is clear that, the

effect of the motor efficiency on the total efficiency is greaten that the effect of the converter efficiency. The AHMLI features a converter efficiency slightly lower than that of a step modulated MLI, but higher than of a PWM MLI. It however shows the higher motor efficiency, thanks to the absence of low-order current harmonic components. As a result, the AHMLI scores the higher total efficiency.

4.2 Field Oriented Control on AHMLI AC Motor Drives

A current controlled AHMLI has been developed suitable for vector control applications in fields as, motor drives, STATCOM, photovoltaic and wind generators Fig. 4. 46. Multilevel inverters are today common equipment for variable speed AC drives used in laminators, pumps, conveyors, compressors, fans, blowers and mills, as well as, in railway and naval propulsion plants. In these systems phase current distortion is the cause of torque oscillation and additional power losses.

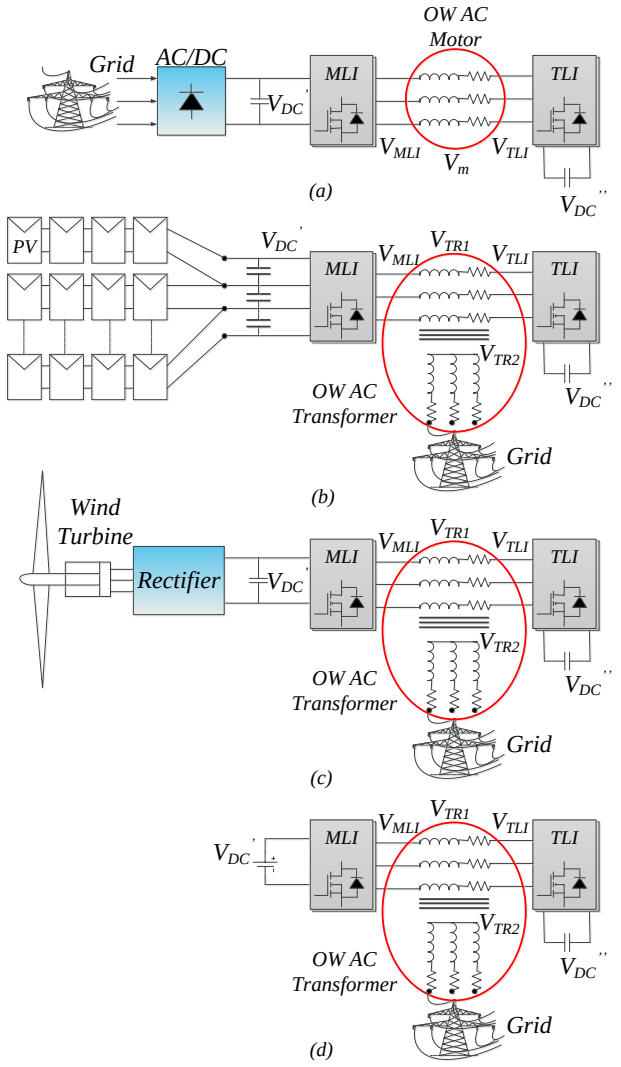


Fig. 4. 46 AHMLI applications: AC motor drives (a); Photovoltaic (b); Wind generators (c), STATCOM (d).

The developed AHMLI current control system for field oriented induction motor drives is shown in Fig. 4. 47. It encompasses two different subsystems, respectively driving the MLI and the TLI and belongs to the class of synchronous current regulators acting on rotating d,q axes components of the current. According to the proposed AHMLI configuration, the MLI manages the main active power stream, thus its current control subsystem is mainly tasked to regulate the fundamental component of the phase current, while also decoupling the q,d axes regulation. It is of the predictive type, in fact, motor back-EMF components E_d* and E_q*, are estimated and then used to determine q,d axes MLI voltage references.

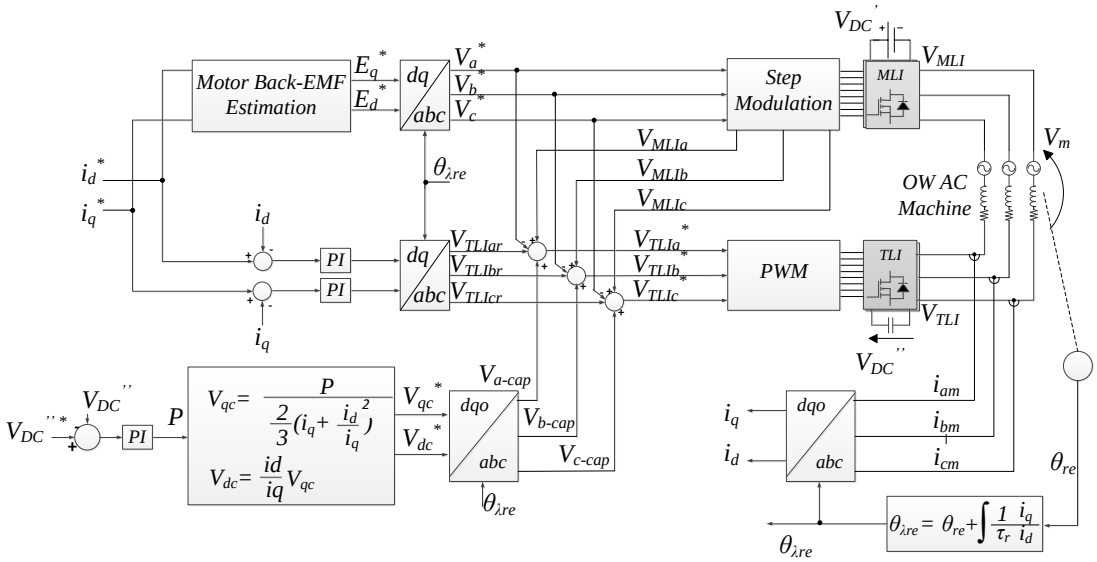


Fig. 4. 47 AHMLI current control system for field oriented induction motor drives.

The qd0 voltage equations in a rotor flux reference frame of an induction motor are expressed as:

$$\begin{aligned} V_{qs} &= R_s i_{qs} + p\lambda_{qs} + \omega_{\lambda r}\lambda_{ds} = R_s i_{qs} + p\lambda_{qs} + E_{qs} \\ V_{ds} &= R_s i_{ds} + p\lambda_{ds} - \omega_{\lambda r}\lambda_{qs} = R_s i_{ds} + p\lambda_{ds} + E_{ds} \\ V_{qr} &= R_r i_{qr} + p\lambda r + (\omega_{\lambda r} - \omega_r)\lambda_{dr} = 0 \\ V_{dr} &= Rri_{dr} + p\lambda_{dr} - (\omega_{\lambda r} - \omega_r)\lambda_{qr} = 0 \end{aligned} \tag{4.27}$$

where E_{ds} and E_{qs} are the back-EMF components, R_s and R_r are the stator and rotor resistances and $\omega_{\lambda re}$ is the rotor flux angular speed. The stator and rotor fluxes are given by:

$$\begin{aligned} \lambda_{qs} &= (L_{ls} + L_m)i_{qs} + L_m i_{qr} = L_s i_{qs} + L_m i_{qr} \\ \lambda_{ds} &= (L_{ls} + L_m)i_{ds} + L_m i_{dr} = L_s i_{ds} + L_m i_{dr} \\ \lambda_{qr} &= (L_{lr} + L_m)i_{qr} + L_m i_{qs} = L_r i_{qr} + L_m i_{qs} \\ \lambda_{dr} &= (L_{lr} + L_m)i_{dr} + L_m i_{ds} = L_r i_{dr} + L_m i_{ds} \end{aligned} \tag{4.28}$$

being L_s, L_r and L_m the stator, rotor and magnetizing inductances, respectively. Since that λ_{qr}=0 in Field Oriented Control condition, the q-axes stator current i_{qs} can be written as a function of q-axes rotor current i_{qr}:

$$\begin{aligned} L_r i_{qr} + L_m i_{qs} &= 0 \\ i_{qr} &= -\frac{L_m}{L_r} i_{qs} \end{aligned} \tag{4.29}$$

Furthermore, since V_{dr}=0 the d-axes stator current i_{ds} can be written as a function of d-axes rotor current i_{dr}:

$$\begin{aligned} V_{dr} &= R_r i_{dr} + p\lambda_{dr} = 0 \\ 0 &= R_r i_{dr} + pL_r i_{dr} + pL_m i_{ds} \\ pi_{ds} &= -i_{dr} \frac{(R_r + pL_r)}{L_m} \end{aligned} \tag{4.30}$$

Since the flux is kept constant at the rating value by holding i_{ds}= i_{rated}, comes from eq. (4.29) that i_{dr}=0.

Thus, the d-axes stator and rotor flux can be written as:

$$\begin{aligned} \lambda_{ds} &= L_s i_{ds} \\ \lambda_{dr} &= L_m i_{ds} \end{aligned} \tag{4.31}$$

The q-axis back-EMF E_{qs} is given by:

$$E_{qs} = \omega_{\lambda r} \lambda_{ds} = \omega_{\lambda r} L_s i_{ds} \tag{4.32}$$

while the d-axis back-EMF E_{ds} is given by:

$$E_{ds} = \omega_{\lambda r} \lambda_{qs} = \omega_{\lambda r} (L_s i_{qs} + L_m i_{qr}) \tag{4.33}$$

replacing eq. (4.28) into eq. (4.32):

$$E_{ds} = \omega_{\lambda r} \lambda_{qs} = \omega_{\lambda r} i_{qs} (L_s - \frac{L_m{}^2}{L_r}) \tag{4.34}$$

imposing:

$$L_K = (\frac{L_r L_s - L_m^2}{L_r}) \tag{4.35}$$

the qd-axis back-EMF will be:

$$\begin{aligned} E_{qs} &= \omega_{\lambda r} L_s i_{ds} \\ E_{ds} &= -L_K \omega_{\lambda r} i_{qs} \end{aligned} \tag{4.36}$$

These quantities are the estimated q,d axes MLI reference voltages and are synthetized through a high efficiency step-modulation. The composition of the voltage across the stator resistance $R_s i_s$ and the inductive voltage term $p\lambda_s$, which represents the difference between the reference voltage and the back-EMF, are instead obtained by the PWM TLI. The TLI current control subsystem acts as the main closed loop regulator, taking advantage from the dynamic and precision of PWM techniques. It exploits two PI regulators to generate the TLI *q,d* axes voltage references V_{TLIqd}, as depicted in Fig. 4. 47. According to the AHMLI approach, the TLI is also tasked to act as an active power filter. Thus some additional components are added to *a,b,c* voltage references, namely:

$$\begin{aligned} V_{MLIa} &- V_a^* \\ V_{MLIb} &- V_b^* \\ V_{MLIc} &- V_c^* \end{aligned} \tag{4.37}$$

These terms predictively compensate low order phase voltage harmonics generated by MLI, as shown in Fig. 4. 11.

As discussed in section 4.1.4.1, the TLI is floating, thus, it can be charged only by establishing a controlled active power stream between the two inverters, through the DC-Bus voltage V_{DC}'' control of Fig. 4. 24. Thus, a further corrective term $V_{abc\text{-}c}$, is introduced into the TLI reference voltage. Finally, additional terms $V_{abc\text{-}DC}$ are also added to balance the voltages across the DC-Bus capacitors of the MLI. The TLI voltage references V_{TLIabc}^*, thus, consists of four terms:

$$V_{TLIabc}^* = V_{TLIabcr} + (V_{MLIabc} - V_{abc}^*) + V_{abc-cap} + V_{abc-DC} \tag{4.38}$$

where $V_{TLIabcr}$ is the generic output of the TLI current control system, (V_{MLIabc} -V_{abc}^*) is the harmonic compensation term, $V_{abc\text{-}c}$ is the DC-Bus voltage V_{DC}'' control term and $V_{abc\text{-}DC}$ is the MLI DC-Buses capacitors term.

4.2.1 Simulation and Experimental results on AHMLI AC Motor Drives

Simulation tests and experimental validations have been carried out in order to evaluate the effectiveness of the AHMLI current control system. The considered test bench is that of Fig. 4. 30 with V_{DC}'=575V and V_{DC}''=50V. The d-axes motor current is set to 2.5 A in order to obtain the rated flux. A -40rad/s to 40rad/s speed transient response is shown in Fig. 4. 48, giving a quite satisfactory performance. A comparison between the simulation and experimental results is also depicted. Fig. 4. 49 shows the motor phase currents i_a, i_b and i_c when a reversal speed transient is applied. According to the AHMLI current control algorithm, the *qd* components of motor Back-EMF

are estimated, transformed to the abc reference frame and generated by the MLI, Fig. 4. 50. Fig. 4. 51 shows the TLI reference voltage, which consists of the harmonic compensation term, the TLI DC-Bus voltage control term and the output current control term. The TLI DC-Bus voltage V_{DC}'', MLI staircase output voltage V_{MLIa} and the motor phase voltage V_{ma} are also depicted. The 5LI qdo Back-EMF voltage angular θ_{re} and the a-phase current i_a are shown in Fig. 4. 52. Experimental results of Fig. 4. 53 confirm the validity of the simulation tests in terms of voltage and current THD improvement and current control response.

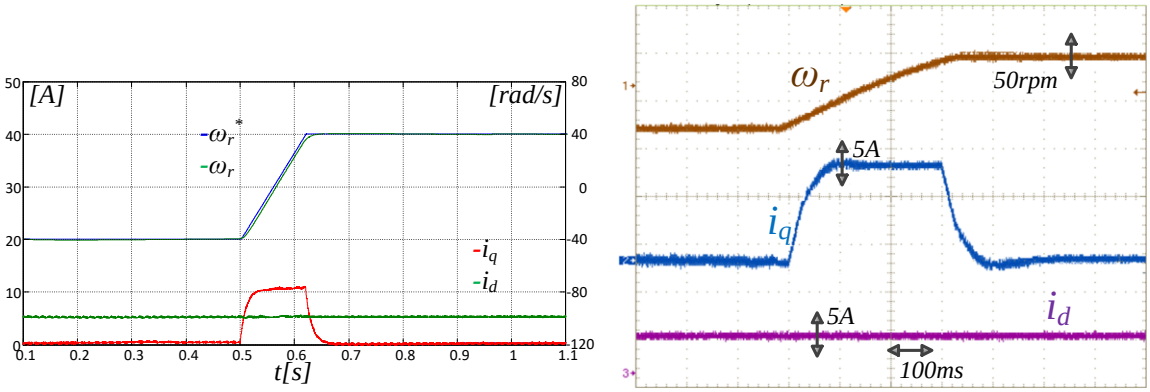


Fig. 4. 48 5MLI+TLI AHMLI: Speed step response from -40rad/s to 40 rad/s: ωr,, iq and id. Simulation results(up), Experimental results(down)

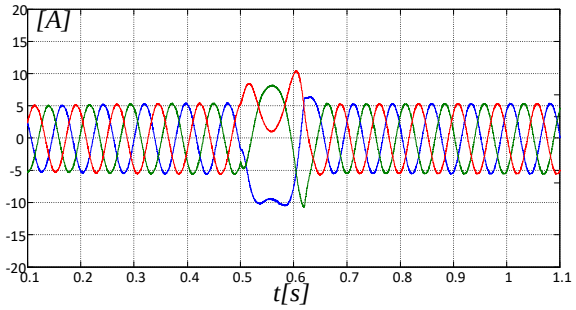


Fig. 4. 49 5MLI+TLI AHMLI: Speed step response from -40rad/s to 40 rad/s: ωr, phase currents ia, ib and ic

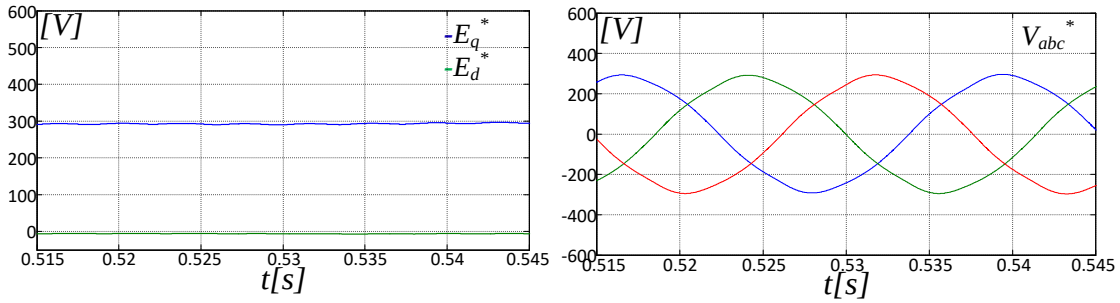


Fig. 4. 50 5LI+TLI AHMLI steadt state simulations: 5LI qdo Back-EMF voltage references E_q^* and E_d^*(left). 5LI phase voltage references V_{abc}(right)*

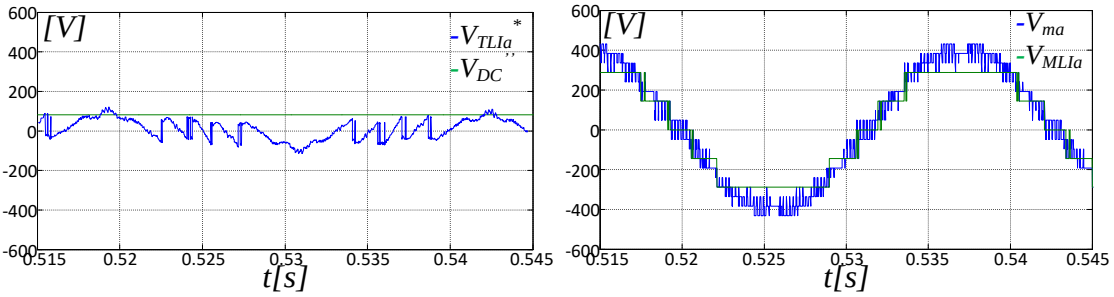


Fig. 4. 51 5LI+TLI AHMLI steadt state simulations: TLI a-phase voltage references V_{TLIa}^{*}, TLI DC-Bus voltage V_{DC}'' (left). 5LI starcase a-phase voltage V_{MLIa} and motor a-phase voltage V_{ma} (right)

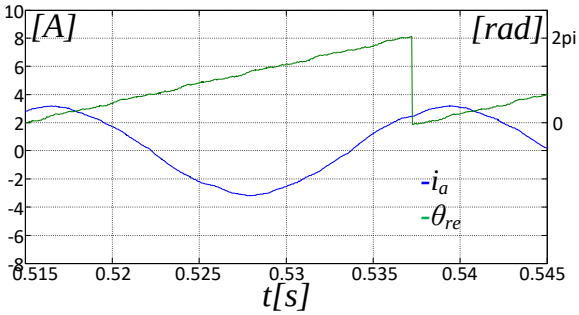


Fig. 4. 52 5LI+TLI AHMLI steadt state simulations: 5LI qdo Back-EMF voltage angular θ_e and a-phase current i_a

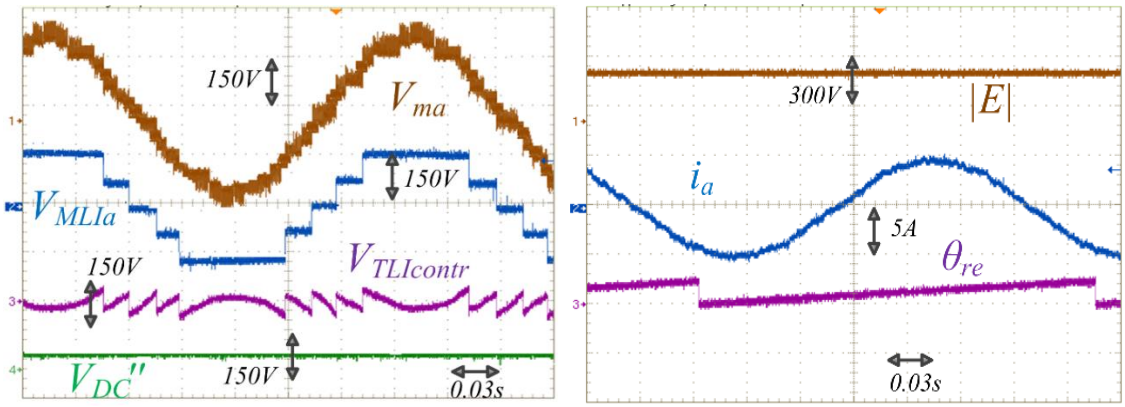


Fig. 4. 53 5MLI+TLI AHMLI steadt state Experimental tests: a-Motor phase voltage V_{ma},, 5LI starcase output voltage V_{MLIa}, TLI phase voltage reference $V_{TLIacontr}$, TLI DC Bus voltage V_{DC}'',(left). Back-EMF |E|, stator current i_a and 5LI voltage angle θre.

4.3 AHMLI approach for STATCOM and Generators

The AHMLI approach has been also applied for STATCOM and renewable energy applications [25]. In this case, as shown in Fig. 4. 54, an Open-end Winding Transformer (OWTR) interfaces the main MLI, acting as a grid-side inverter, and the utility grid. The primary windings of the transformer are connected to a MLI from one side, and on the other side to a TLI inverter. The secondary windings of the transformer are instead connected to the grid. According to the AHMLI approach, the MLI is step modulated while the TLI works as active power filter, in order

to compensate undesired low-order voltage harmonics generated by MLI. Since the phase voltages V_{ap}, V_{bp} and V_{cp} of the primary windings are filtered by TLI, the phase voltages V_{as}, V_{bs} and V_{cs} of the secondary windings are sinusoidal. Thus, it is possible to realize a grid-side inverter without large additional passive filters.

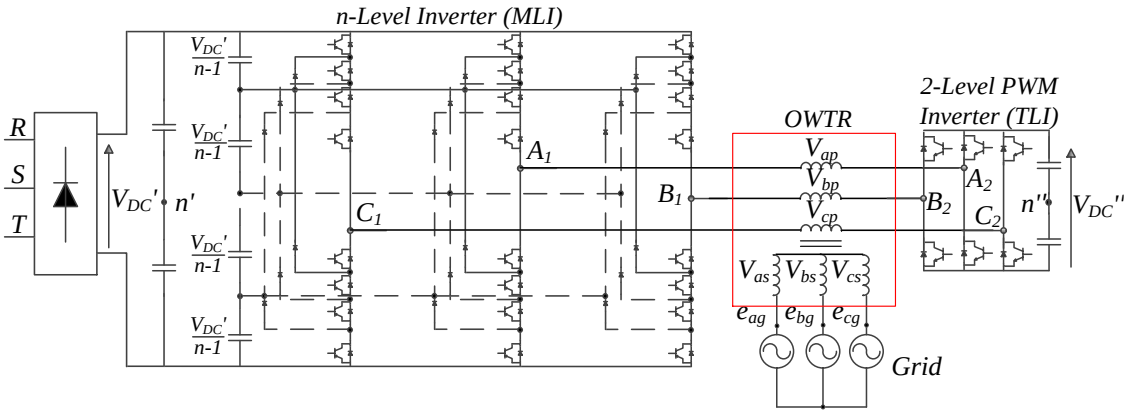


Fig. 4. 54 Asymmetrical Hybrid Multilevel Inverter applied to STATCOM and generators

The transformer voltage equations are given by:

$$\begin{aligned} V_{abcp} &= R_p i_{abcp} + p\lambda_{abcp} \\ V_{abcs} &= R_s i_{abcs} + p\lambda_{abcs} \\ \frac{V_{abcp}}{V_{abcs}} &= \frac{i_{abcs}}{i_{abcp}} = t \end{aligned} \tag{4.39}$$

being t the transformation ratio of the transformer, i_{abcp} and i_{abcs} the phase currents of the primary and secondary windings respectively, λ_{abcp} and λ_{abcs} the total fluxes of the primary and secondary windings, respectively. Fig. 4. 55 shows the equivalent circuit of a AHMLI exploiting an open-end winding transformer. The phase currents of the primary windings depend on: the MLI phase output voltages V_{MLIabc}, the TLI phase output voltages V_{TLIabc}, the differential-mode voltage $V_{n'n''}$, the primary resistance R_p and inductance and L_p. The grid currents instead can be written as a function of the secondary phase voltages V_{abcs}, the phase grid voltage e_{abcg}, the resistance R_p and inductance of the grid L_p. These current equations are given by:

$$\begin{aligned} i_{ap} &= \frac{V_{MLIa} - V_{TLIa} + V_{Tn'n''}}{R_p + j\omega L_p} & i_{ag} &= \frac{e_{ag} - V_{as}}{Z_{ag}} \\ i_{bp} &= \frac{V_{MLIb} - V_{TLIb} + V_{Tn'n''}}{R_p + j\omega L_p} & i_{bg} &= \frac{e_{bg} - V_{bs}}{Z_{bg}} \\ i_{cp} &= \frac{V_{MLIc} - V_{TLIc} + V_{Tn'n''}}{R_p + j\omega L_p} & i_{cg} &= \frac{e_{cg} - V_{cs}}{Z_{cg}} \end{aligned} \tag{4.40}$$

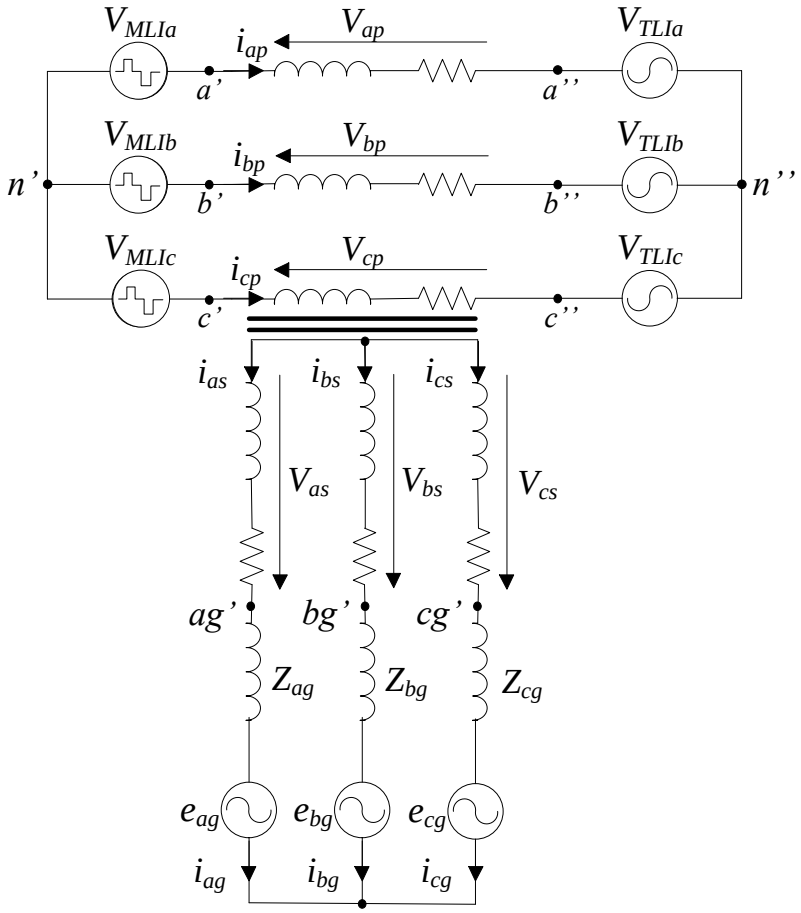


Fig. 4. 55 Equivalent circuit of a AHMLI configuration for STATCOM and generators

The grid current can be controlled by acting on the MLI reference voltages or on the TLI reference voltages. As will be demonstrated in the following, the grid voltages will be synthetized by MLI (considering the transformation ratio *t*) while the control current acts on the TLI reference voltages V_{TLI}. Thus, the MLI provides the entire active power required by the system while the TLI works as active power filter and, at the same time, regulates the grid current.

According to the voltage control scheme of Fig. 4. 56, MLI output voltage is synchronized with the grid voltage through a Phase Looked Loop (PLL) system, which detects the phase and the amplitude of the grid voltages e_{abcg}. [26] Fig. 4. 57. A 50Hz, 400/230 V, 10kVA three-phase open-end winding transformer is tested. Fig. 4. 58 shows the transformer phase voltages with the grid disconnected from the secondary windings. The grid voltage frequency is f=50Hz, the TLI switching frequency is f_{sw}=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$. In particular, Fig. 4. 58(left) depicts the primary phase voltages V_{abcp} while Fig. 4. 58(right) shows the secondary phase voltages V_{abcs}. The phase grid voltages e_{abcg} are shown in Fig. 4. 59(left), while Fig. 4. 59(right) shows the electric angular frequency of e_{ag}, as detected by the PLL. When the OWT is disconnected from the grid, the phase magnetization currents circulate through the primary windings, as in Fig. 4. 60(left). Once the secondary phase voltages V_{abcs} are synchronized with the phase grid voltage e_{abcg} (the same in amplitude, frequency and phase), the secondary windings of the transformer

can be physically connected to the network. Active and reactive power control can be performed by acting on the amplitude and phase of the MLI phase voltages V_{MLIabc} and on the TLI phase voltages $V_{TLIabc,}$ as shown in Fig. 4. 60 (right).

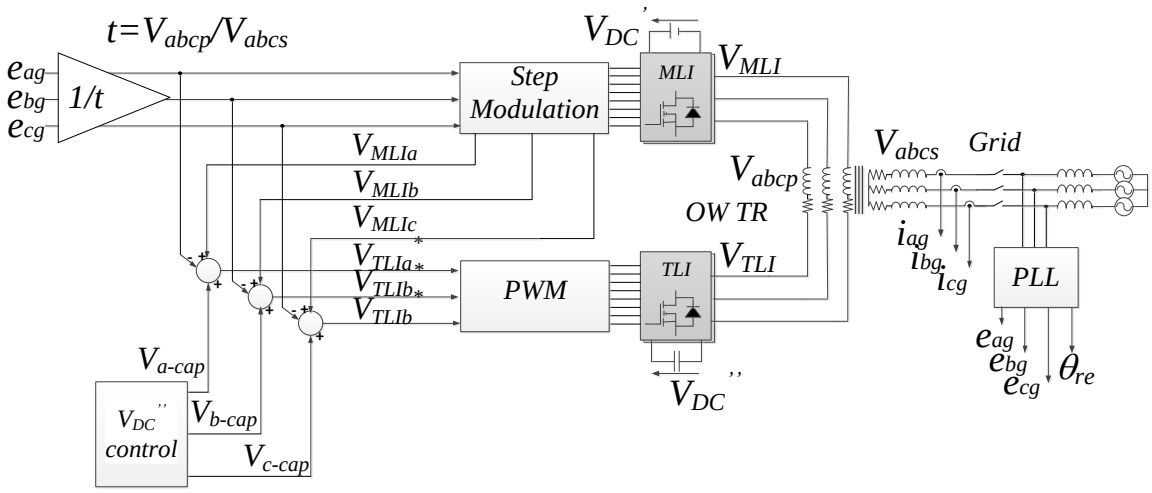


Fig. 4. 56 Voltage control scheme of an AHMLI system for STATCOM and generators

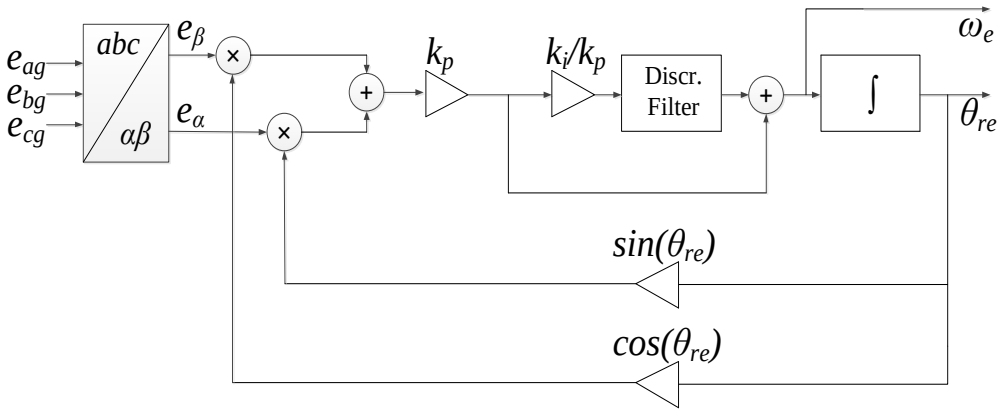


Fig. 4. 57 Phase Looked Loop (PLL)

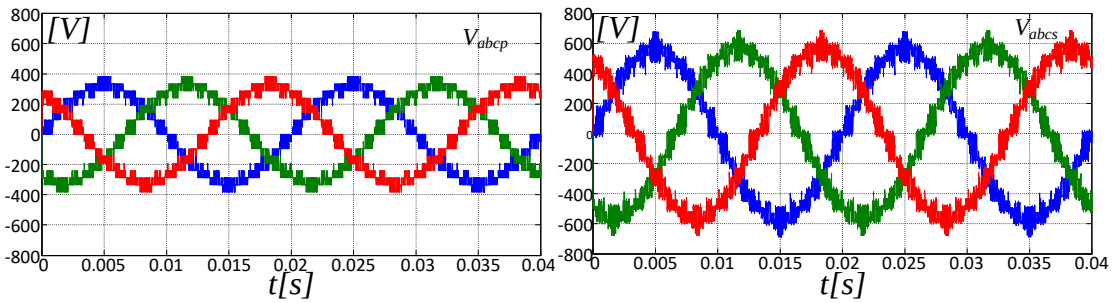


Fig. 4. 58 Phase voltage of the transformer with voltage control and no-grid connected, f=50Hz, fsw=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: Primary voltages V_{abcp} (left), secondary voltages V_{abcs} (right)

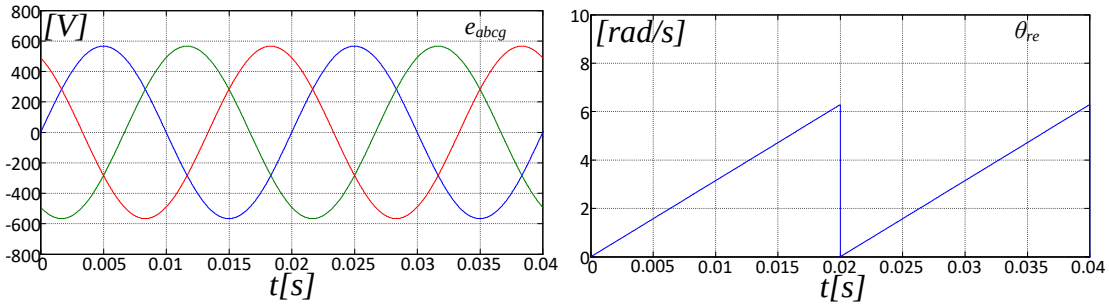


Fig. 4. 59 Phase grid voltages with voltage control and no-grid connected, f=50Hz, fsw=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: Grid voltages e_{abcg} (left), electrical angular of the phase voltage θ_{re} (right)

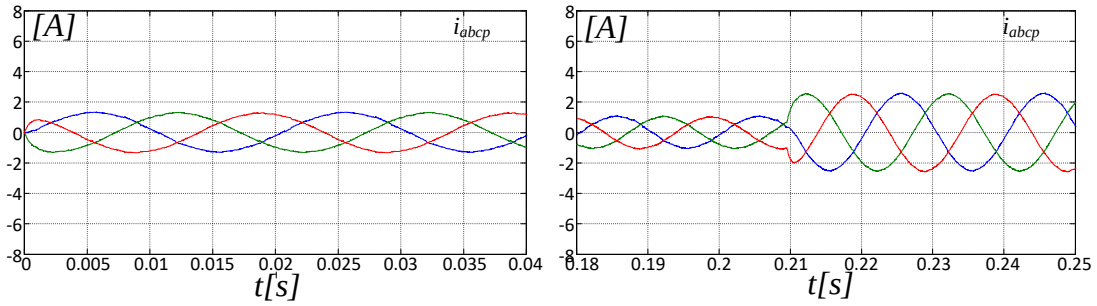


Fig. 4. 60 Phase magnetization currents of the transformer with voltage control, f=50Hz, fsw=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: no grid connected(left), grid connected(right)

4.3.1 AHMLI current control system for STATCOM and Generators

In order to control the active and reactive power flow in STATCOM and Generator applications, a suitable current controlled AHMLI has been developed, exploiting an OWT. Fig. 4. 61 shows the block scheme of the proposed system. It consists of a step modulated MLI, managing the main active power stream, and a current controlled TLI, which acts as the main closed loop regulator, controlling the grid current. A suitable TLI DC-Bus voltage control is also included to regulate V_{DC}''. Hence, as in the previous case, the TLI compensates low order harmonics generated by MLI step modulation, while also controlling the grid phase currents. Thus, the reference voltages of the MLI are e_{ag}^*, e_{bg}^* and e_{cg}^*:

$$e_{abcg}^{*} = \frac{e_{abcg}}{t} \tag{4.41}$$

while the reference voltages of the TLI are given by:

$$V_{TLIabc}^{*} = V_{TLIabcr} + (V_{MLIabc} - e_{abcg}^{*}) + V_{abc-cap} \tag{4.42}$$

being $V_{abc\text{-}c}$ the output voltage control of the TLI DC-Bus V_{DC}''.

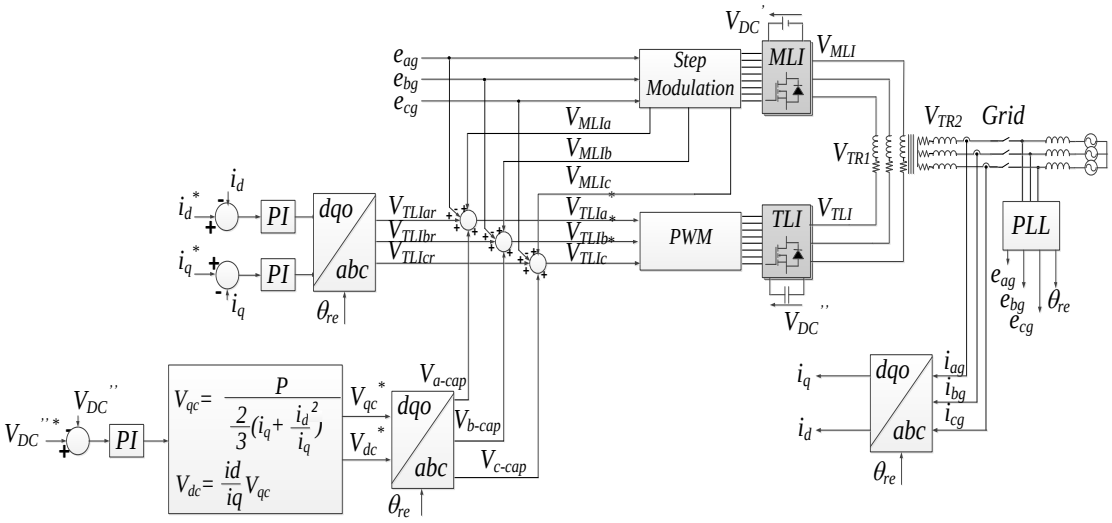


Fig. 4. 61 AHMLI current control system for STATCOM and generators.

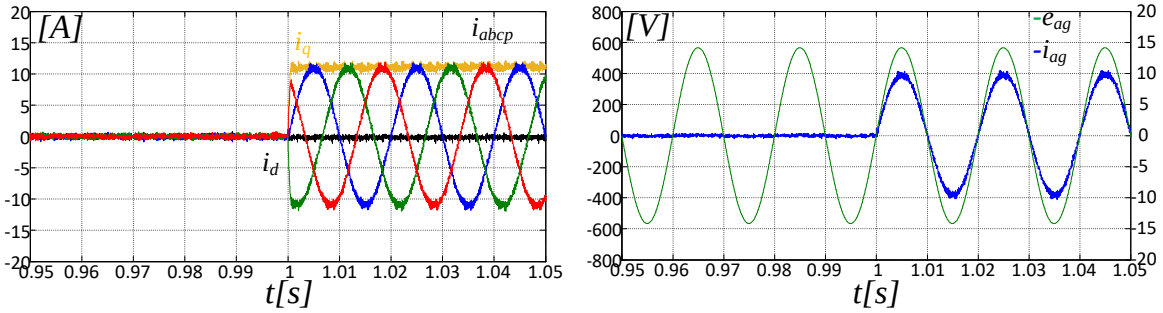


Fig. 4. 62 AHMLI simulation results for generators with f=50Hz, fsw=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: q-axis grid current transient iq from 0 to 12 A and null reactive power id=0, grid currents i_{abcg} (left), a-phase grid current i_{ag} and a-phase grid voltage e_{ag}(right)

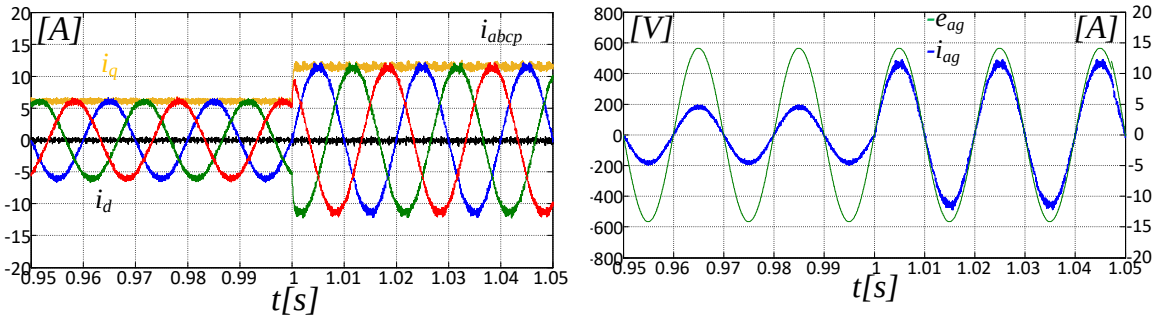


Fig. 4. 63 AHMLI simulation results for generators with f=50Hz, fsw=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: q-axis grid current transient iq from 6 to 12 A and null reactive power id=0, grid currents i_{abcg} (left), a-phase grid current i_{ag} and a-phase grid voltage e_{ag}(right)

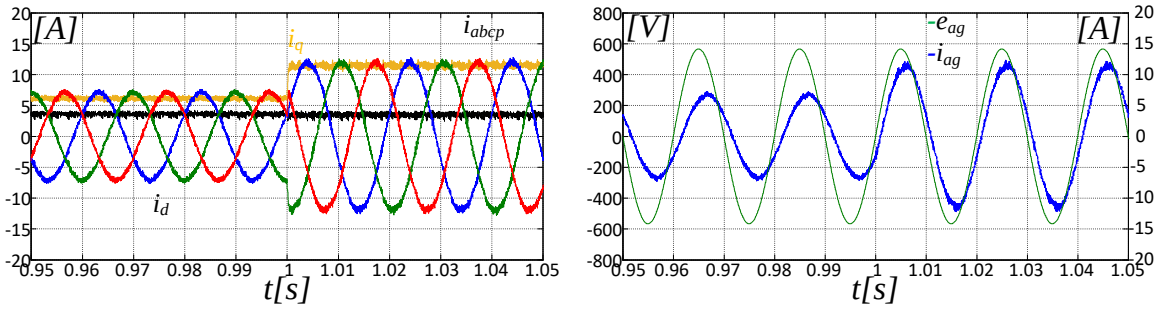


Fig. 4. 64 AHMLI simulation results for STATCOM with f=50Hz, f_{sw}=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: q-axis grid current transient iq from 6 to 12 A and reactive power id=4 A, grid currents i_{abcg} (left), a-phase grid current i_{ag} and a-phase grid voltage e_{ag}(right)

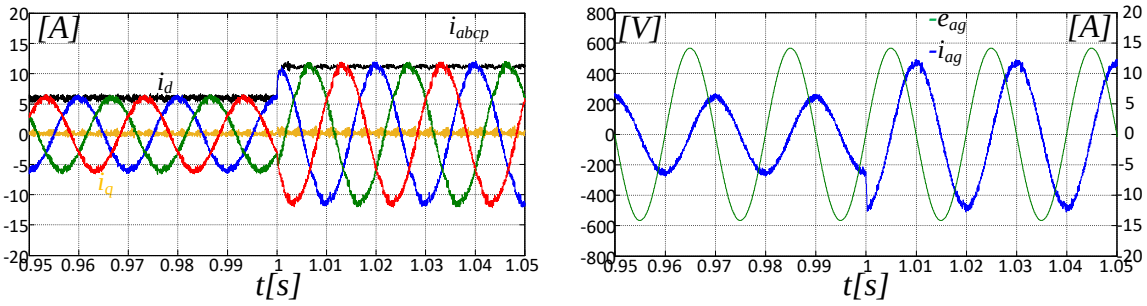


Fig. 4. 65 AHMLI simulation results for STATCOM with f=50Hz, f_{sw}=5kHz and $V_{DC}''=V_{DC}'/2(n-1)$: d-axis grid current transient iq from 6 to 12 A and null active power iq=0 A(left), a-phase grid current i_{ag} and a-phase grid voltage e_{ag}(right)

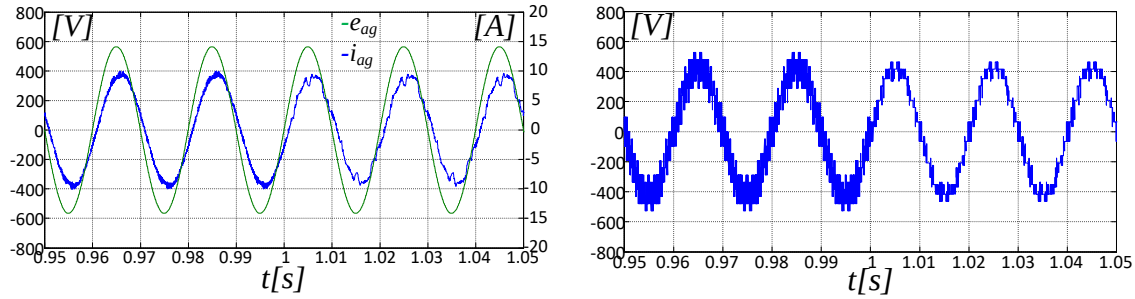


Fig. 4. 66 AHMLI simulation results, impact of the variation of TLI DC Bus voltage V_{DC}'' from $V_{DC}'/2(n-1)$ to $V_{DC}'/2n$(left) on the waveforms with f=50Hz, fsw=5kHz. a-phase grid voltage and a-phase grid current (left), a-phase primary voltage V_{ap} (right)

The performance of the AHMLI approach depends on the value of V_{DC}''. In Fig. 4. 62, after grid connection, the AHMLI is tasked to provide active power to the grid by acting on the q-axis current components, while holding null the reactive power delivered to the main AC grid. In Fig. 4. 62(right), the *a*-phase grid voltage e_{ag} is in phase with the *a*-phase grid current i_{ag}. Fig. 4. 63 depicts a q-axis current transition from 6 A to 12 A, with a null reactive power. In Fig. 4. 64, a reactive power is also generated with i_d=4A. Simulation tests about STATCOM applications are depicted in Fig. 4. 65 where a null active power is transferred to the grid, i_q=0. In a second test the performance of the system is evaluated for two different V_{DC}'' values. As shown in Fig. 4. 66, if $V_{DC}''=V_{DC}'/8$ the TLI is able to perfectly compensate the low-order current harmonic components giving a grid current i_{ag} THD lower than 2%. A distortion of the grid currents is observed when reducing V_{DC}'' to $V_{DC}'/12$.

Experimental tests have been carried out in order to verify the effectiveness of the AHMLI output current control algorithm in STATCOM and generator applications. The test bench is composed by an open-end winding 5kVA - 230V/400V three phase transformer, a five-level NPC inverter with a 600 V DC-Bus voltage and a two-level inverter operating at 10kHz, Fig. 4. 67. Power switches technical specifications are shown in Table 4.4 and Table 4.5 of the previous section.

The secondary winding of the transformer is initially disconnected from the grid, in such a way to synchronize the output voltages V_{abcs} with the grid voltage e_{abcg} with the help of a PLL. At the same time, the TLI compensates undesired low order harmonic components generated by MLI step modulation, as depicted in Fig. 4. 68. In this condition, magnetization currents i_{abcp} flow in the primary winding of the transformer. Once that the secondary winding can be connected to the grid the power flow can be controlled by acting on the current control algorithm.

An active power step response is depicted in Fig. 4. 69. The picture shows the q-axis grid current transient from 0 to 13 A, the *a*-phase grid current waveform and the TLI DC-Bus voltage V_{DC}'', set to $V_{DC}'/2(n-1)=75$ *V*. Fig. 4. 70 demonstrates what seen in simulation tests. The best current harmonic content is achieved by setting V_{DC}'' to *75V*, as depicted in Fig. 4. 71.

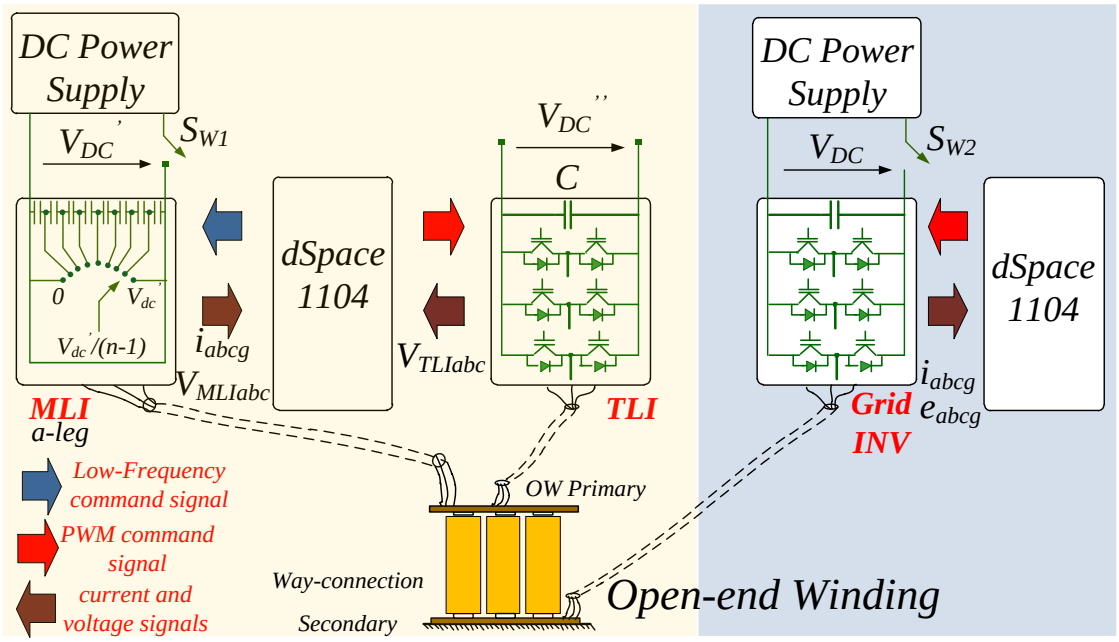


Fig. 4. 67 AHMLI test bench exploiting an open-end winding transformer for STATCOM and Generators

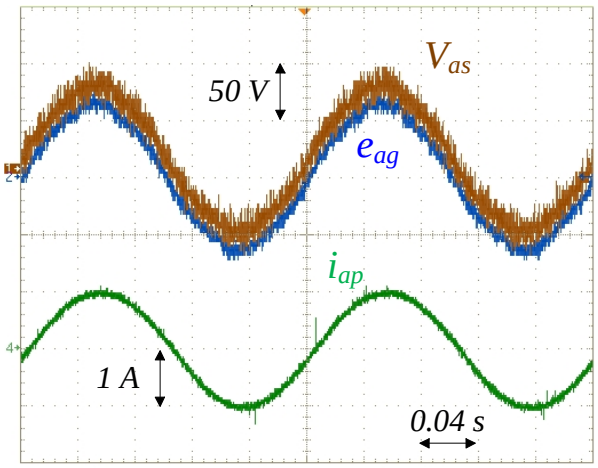


Fig. 4. 68 AHMLI Grid voltage synchronization: Secondary a-phase voltage of the transformer V_{as}, a-phase grid voltage e_{ag}, a-phase magnetization current i_{ap}

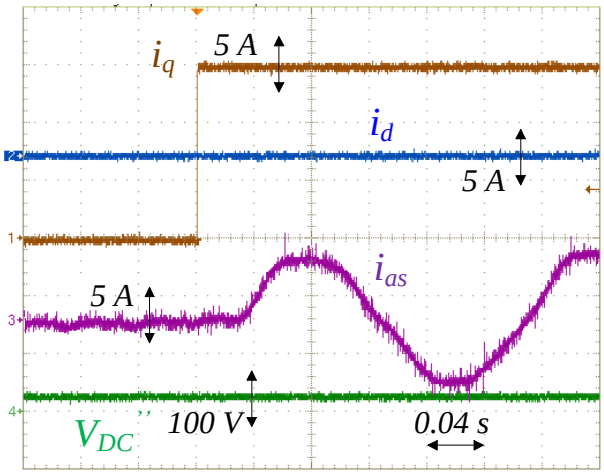


Fig. 4. 69 5MLI+TLI AHMLI active power step response.

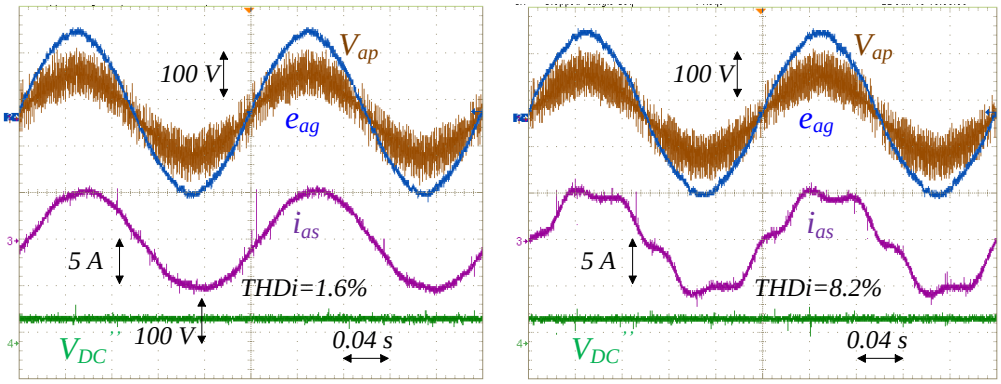


Fig. 4. 70 Grid connected 5MLI+TLI AHMLI: Transformer primary voltage V_{ap}, grid voltage e_{ag}, transformer secondary current i_{ag} and TLI DC Bus voltage V_{DC}''(V_{DC}''= V_{DC}'/8 (left), V_{DC}''= V_{DC}'/12 (right)).

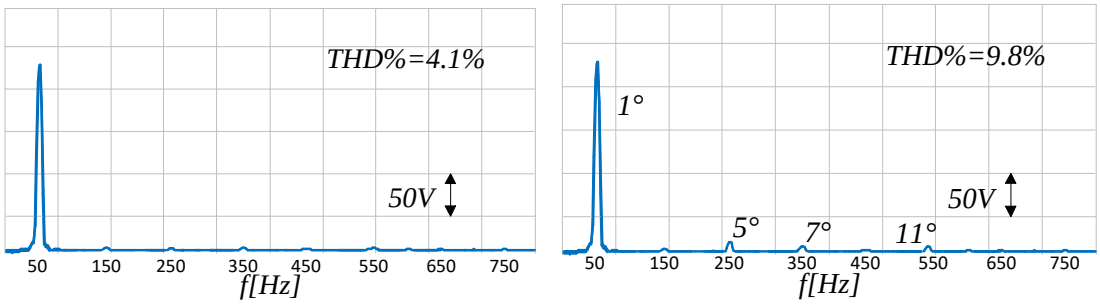


Fig. 4. 71 Grid connected 5MLI+TLI AHMLI: harmonic spectra of Transformer primary voltage V_{ap} (V_{DC}''= V_{DC}'/8 (left), V_{DC}''= V_{DC}'/12 (right)).

4.3.2 AHMLI current control system with grid current harmonic compensation

The TLI of an AHMLI can be exploited to improve the grid phase current harmonic content. The grid voltage, in fact, generally encompasses a 5th and a 7th harmonic, generating correspondent harmonic components of the grid current. A suitable detector has been developed to measure the phase and the amplitude of each undesired

current harmonic. The last are then eliminated through specific additional current control loops driving the TLI. The control system is depicted in Fig. 4. 72. Grid currents are given by:

$$\begin{aligned} i_{ag} &= \frac{e_{ag}1 + e_{ag}5 + e_{ag}7 - V_{as}}{Z_{ag}} \\ i_{bg} &= \frac{e_{bg}1 + e_{bg}5 + e_{bg}7 - V_{bs}}{Z_{bg}} \\ i_{cg} &= \frac{e_{cg}1 + e_{cg}5 + e_{cg}7 - V_{cs}}{Z_{cg}} \end{aligned} \tag{4.43}$$

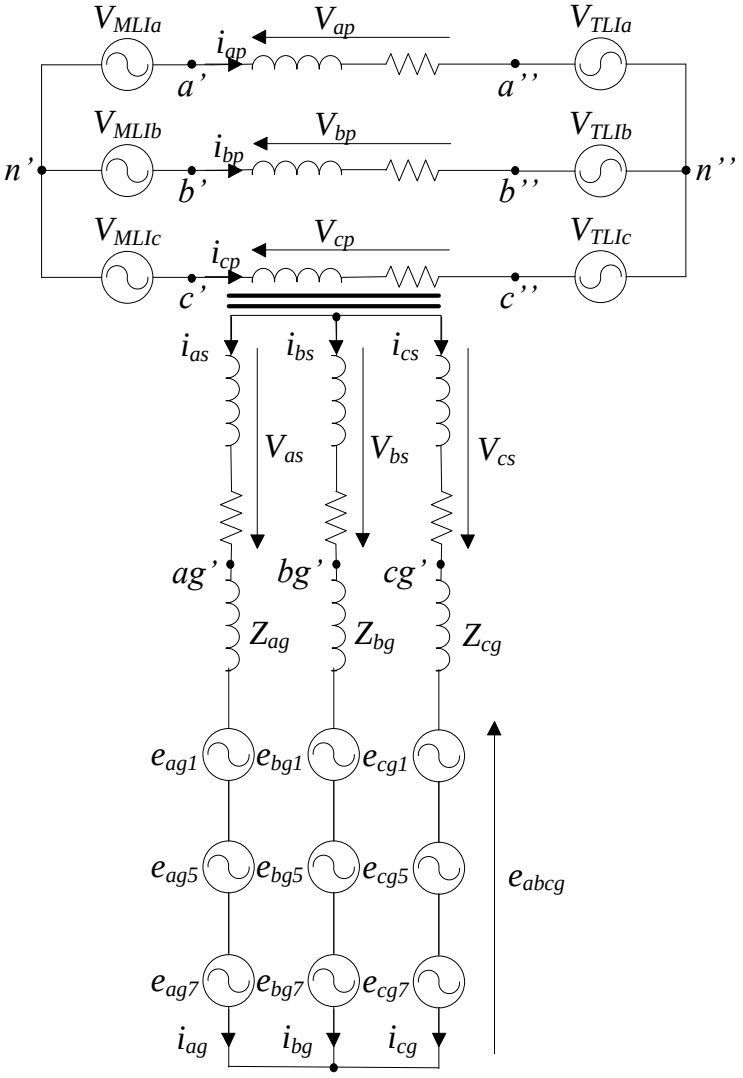


Fig. 4. 72 Equivalent circuit of a AHMLI configuration for STATCOM and generators with distorted grid voltage, 5th and 7th harmonic component

The transformer secondary phase voltage V_{abcs} consists of the fundamental harmonic and of 5th and 7th harmonic components in phase opposition with the 5th and 7th harmonics present on the grid voltage.

According to the eq. (4.42) the TLI reference voltage is given by:

$$V_{TLIabc}^{*} = (V_{MLIabc} - e_{abcg1}^{*}) + e_{abcg5} + e_{abcg7} \tag{4.44}$$

Simulation tests have been performed only considering the 5th harmonic component of the grid voltage. The amplitude of the fundamental phase grid voltage e_{g1} is set to 565 V and frequency f=50Hz, while the 5th harmonic component e_{g5} is set to 50 V and in phase with e_{g1}. The MLI DC-Bus voltage is 575V. Fig. 4. 73(left) shows the grid voltage, which consists of the fundamental and undesired 5th harmonic. Fig. 4. 73(right) shows the transformer primary voltage, with $V_{DC}''=V_{DC}'/2(n-1)=70V$ and f_{sw}=5kHz. At t=0.2 s the 5th harmonic compensation is activated, improving the grid current harmonic content, as depicted in Fig. 4. 74. Harmonic spectra of the grid current and the transformer primary voltage are shown in Fig. 4. 75 and Fig. 4. 76 respectively.

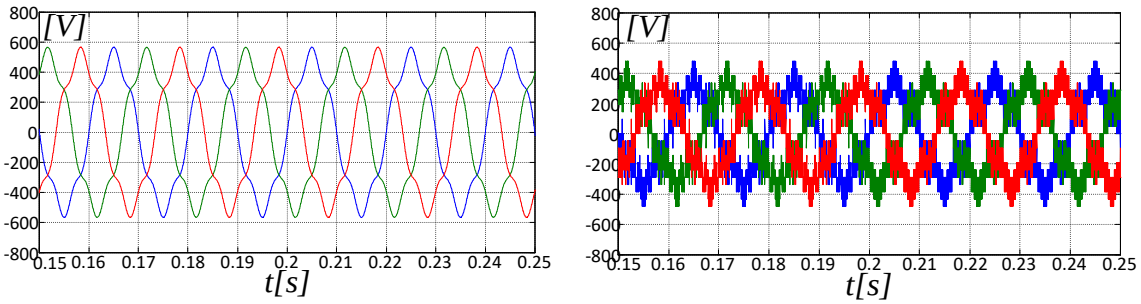


Fig. 4. 73 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th harmonic component. At t=0.2s the 5th harmonic compensation is active: grid voltages e_{abcg} (left), primary voltages V_{abcp}(right)

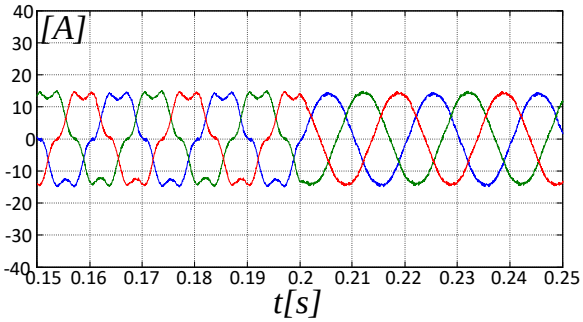


Fig. 4. 74 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th harmonic component. At t=0.2s the 5th harmonic compensation is active: grid currents i_{abcg}

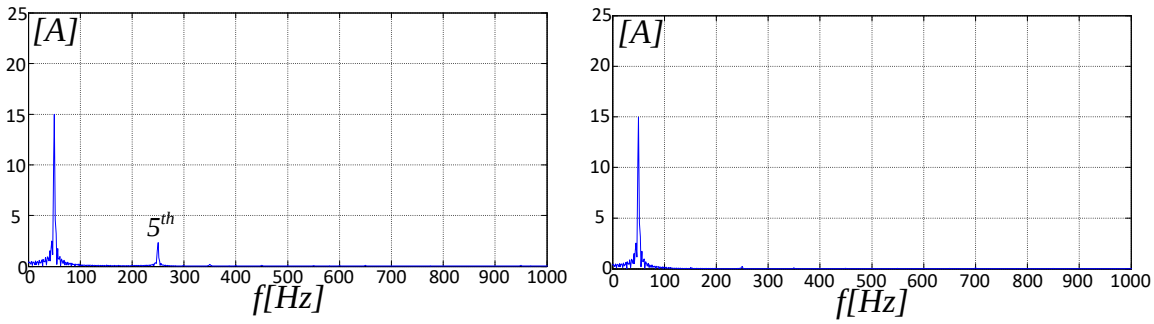


Fig. 4. 75 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th harmonic component. Current i_{ag} harmonic spectrum without 5th harmonic compensation(left), Current i_{ag} harmonic spectrum with 5th harmonic compensation.

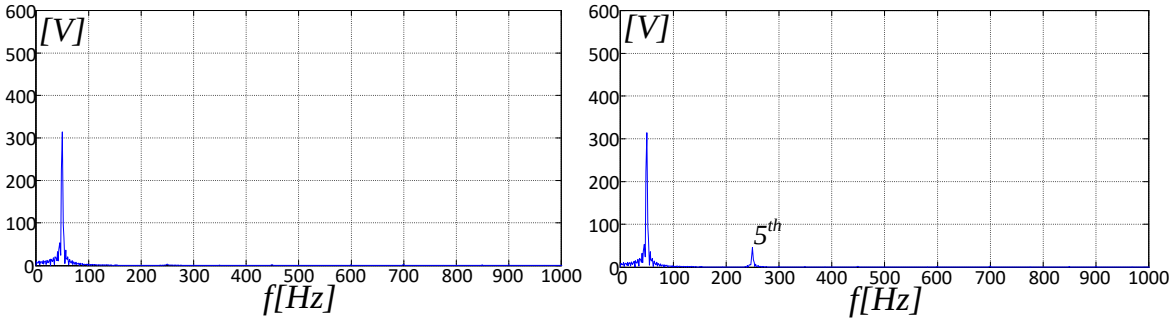


Fig. 4. 76 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th harmonic component. Primary voltage V_{ap} harmonic spectrum without 5^{th} harmonic compensation(left), Primary voltage V_{ap} harmonic spectrum with 5^{th} harmonic compensation.

The same tests are also performed considering the presence of undesired 5^{th} and 7^{th} harmonic components of the grid voltage as depicted in Fig. 4. 77Fig. 4. 78Fig. 4. 79Fig. 4. 80. The 5^{th} harmonic component is set to 50 V and in phase with e_{ag1} while the 7^{th} harmonic component is set to 20 V and in phase with e_{ag1}.

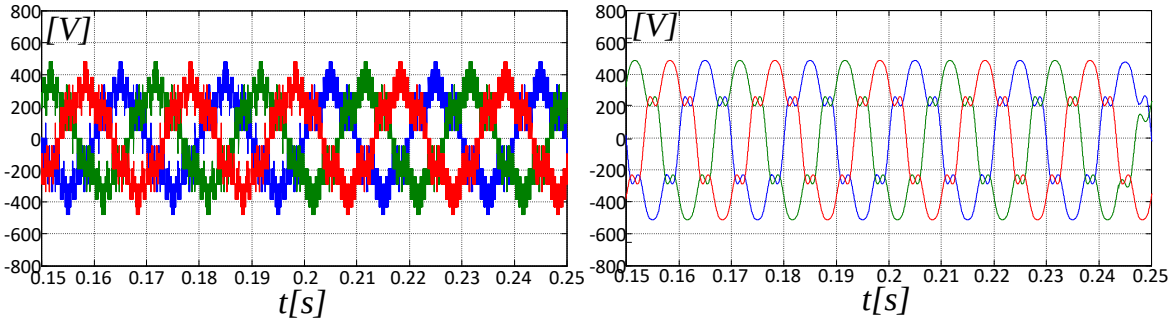


Fig. 4. 77 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5^{th} and 7^{th} harmonic components. At t=0.2s the 5^{th} and 7^{th} harmonic compensation is active: primary voltages V_{abcp}(left), grid voltages e_{abcg}

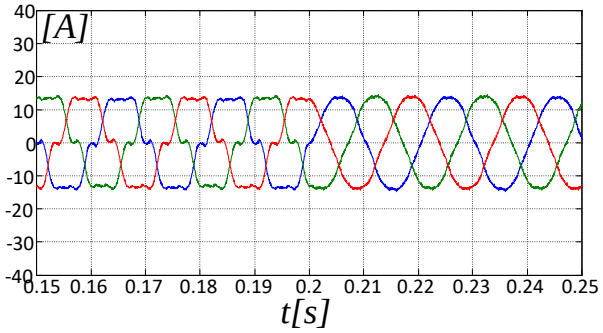


Fig. 4. 78 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5^{th} and 7^{th} harmonic component. At t=0.2s the 5^{th} and 7^{th} harmonic compensation is active: grid currents i_{abcg}

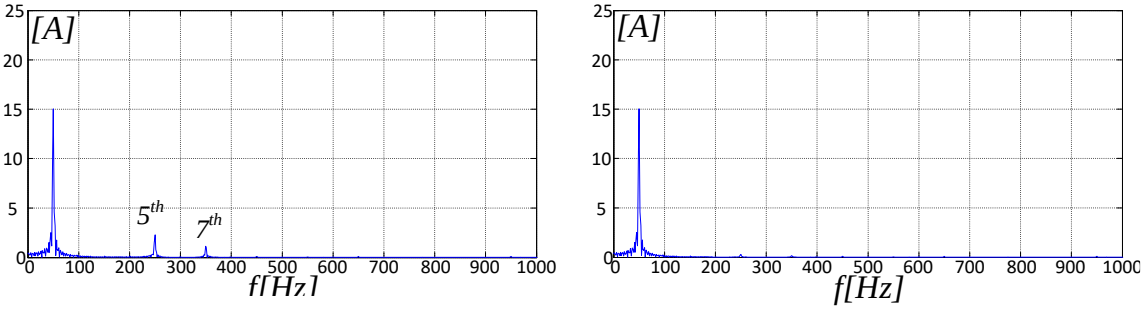


Fig. 4. 79 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th and 7^{th} harmonic component. Current i_{ag} harmonic spectrum without 5^{th} and 7^{th} harmonic compensation(left), Current i_{ag} harmonic spectrum with 5^{th} and 7^{th} harmonic compensation.

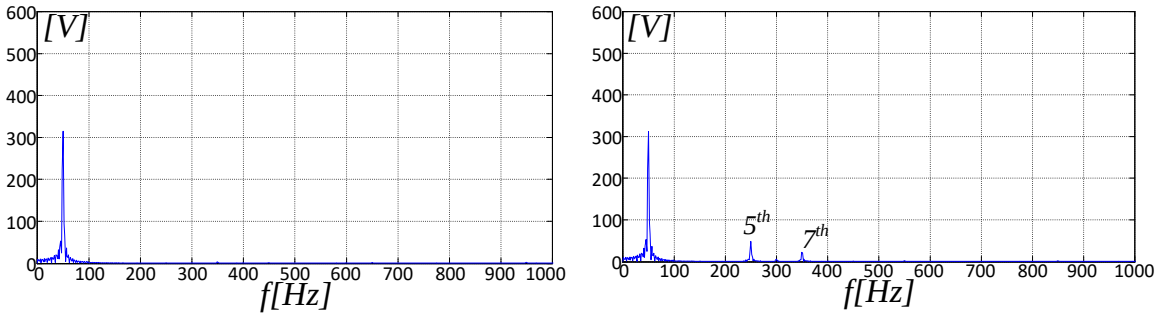


Fig. 4. 80 AHMLI simulation results for STATCOM and generators with distorted grid voltage, 5th and 7th harmonic component. Primary voltage V_{ap} harmonic spectrum without 5th and 7th harmonic compensation(left), Primary voltage V_{ap} harmonic spectrum with 5th and 7th harmonic compensation.

The output current control block diagram is shown in Fig. 4. 81.

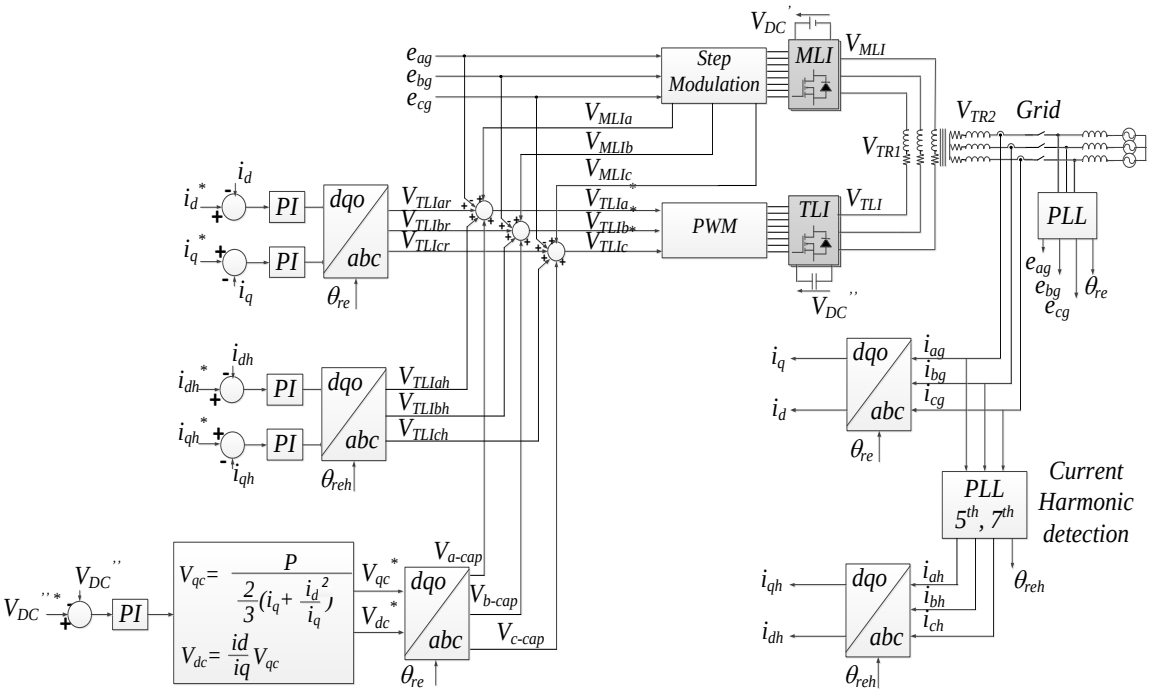


Fig. 4. 81 AHMLI current control system for STATCOM and generators with grid current harmonic elimination.

The PLL system detecting 5th and 7th harmonic components of the grid voltage has been modified as shown in Fig. 4. 83 , by including the two discrete low pass filters sketched in Fig. 4. 83. .

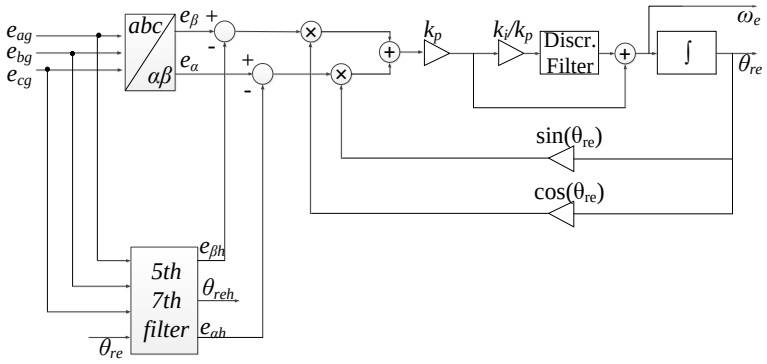


Fig. 4. 82 Phase Looked Loop (PLL) with harmonics detection.

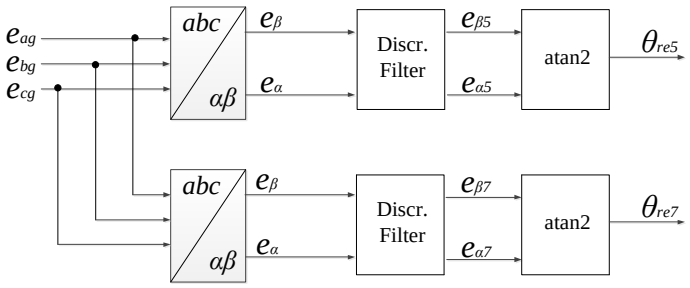


Fig. 4. 83 5th and 7th filter of the Phase Looked Loop (PLL) harmonics detection.

The amplitude of 5th and 7th harmonic components are given by:

$$\begin{aligned} |e_5| &= \sqrt{e_{\alpha 5}^2 + e_{\beta 5}^2} \\ |e_7| &= \sqrt{e_{\alpha 7}^2 + e_{\beta 7}^2} \end{aligned} \tag{4.45}$$

while the phase angles are:

$$\begin{aligned} \theta_{re5} &= {}^5\theta_{re} = tg^{-1}\left(\frac{e_{\alpha 5}}{e_{\beta 5}}\right) \\ \theta_{re7} &= {}^7\theta_{re} = tg^{-1}\left(\frac{e_{\alpha 7}}{e_{\beta 7}}\right) \end{aligned} \tag{4.46}$$

Hence, the generic TLI voltage reference $V_{TLIcontr}$ becomes:

$$V_{TLIabc}^{*} = V_{TLIabcr} + V_{TLIabch} + (V_{MLIabc} - e_{abcg}^{*}) + V_{abc-cap} \tag{4.47}$$

being $V_{TLIabch}$ an additional component of the TLI voltage reference to compensate the grid harmonic components. Simulation tests have been carried out in order to verify the effectiveness of the output current control. The dynamic response of the qd-axes and grid currents are shown in Fig. 4. 84, highlighting that undesired grid currents harmonics are wiped out, Fig. 4. 85.

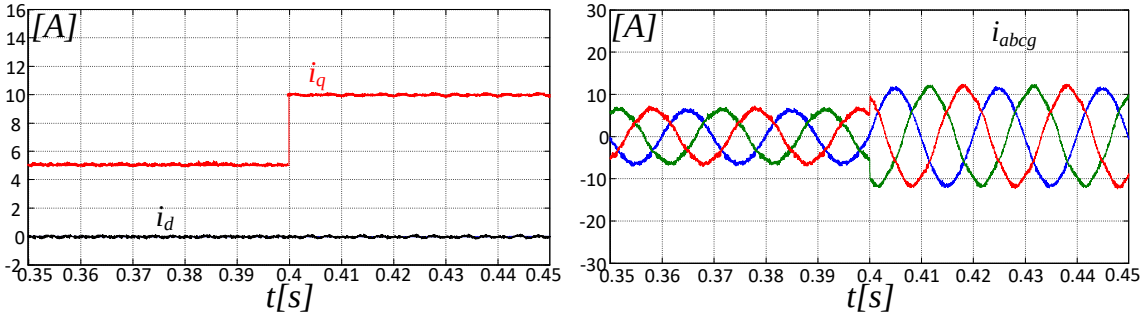


Fig. 4. 84 AHMLI Output current control with 5th and 7th harmonic compensation. qd-axes grid currents(left), abc grid currents (right).

Effects of current harmonic compensation are observable in Fig. 4. 87,. Fig. 4. 87 and Fig. 4. 88. The harmonic spectrum of the transformer primary voltage encompasses 5th and the 7th harmonic components, in phase opposition with the correspondent components of the grid voltage.

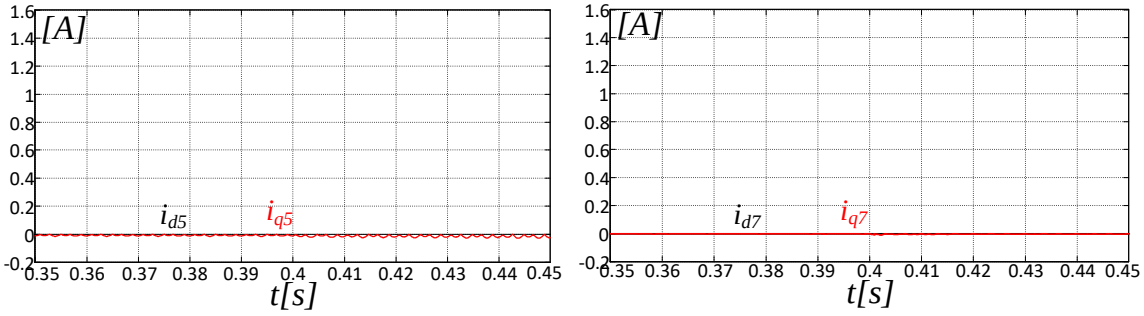


Fig. 4. 85 AHMLI Output current control with 5th and 7th harmonic compensation. 5th harmonic qd-axes grid currents(left), 7th harmonic qd-axes grid currents (right).

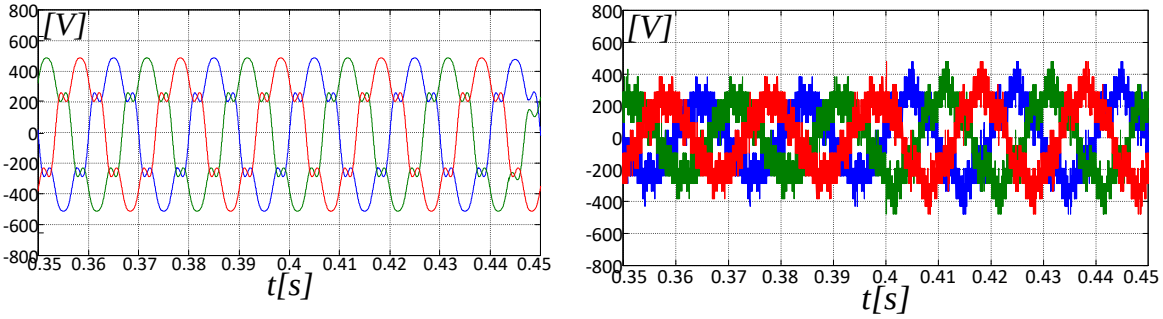


Fig. 4. 86 AHMLI Output current control with 5th and 7th harmonic compensation. grid voltages with 5th and 7th harmonic(left), primary voltage of the transformer with 5th and 7th harmonic compensation (right).

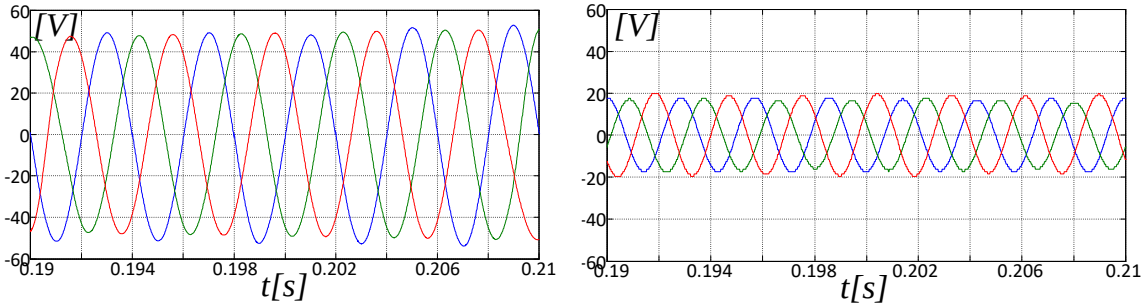


Fig. 4. 87 AHMLI Output current control with 5th and 7th harmonic compensation. TLI reference output voltage $V_{TLIabc5}$(left), TLI reference output voltage $V_{TLIabc7}$ (right).

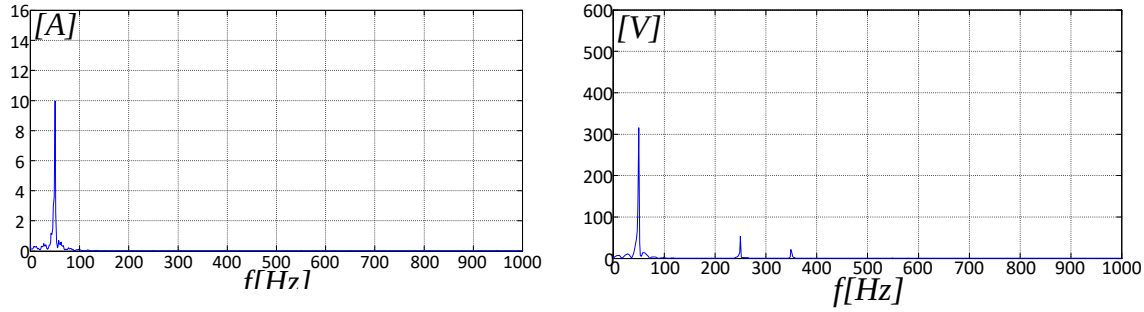


Fig. 4. 88 AHMLI Output current control with 5th and 7th harmonic compensation. Harmonic spectrum of i_{abcg}(left), Harmonic spectrum of V_{TR1} (right).

Experimental tests confirmed the accuracy of the simulation results. The test bench is that of Fig. 4. 67. As mentioned earlier, once that the output voltage V_{abcs} is synchronized with the grid voltage e_{abcg}, the new output current control algorithm is activated. In Fig. 4. 89, the 5th harmonic component e_{abcg5} is equal to 50V while the 7th harmonic component e_{abcg7} is equal to 20V. The TLI DC-Bus voltage is 50 V. Fig. 4. 90 deals with an evaluation of the effectiveness of the AHMLI in compensating 5th and 7th harmonic components of the grid current. After activating the power filter, the grid current i_{ag} becomes almost perfectly sinusoidal. Starting from time t^*, two additional TLI current control loops generate 5th and 7th output current components in phase opposition with grid harmonics. According to Fig. 4. 91, the THD of the grid current and transformer primary voltage without harmonics compensation are respectively 10.9% and 5.2%. Having activated the power filter their values become 2.9% and 11.9% respectively. The last result is caused by the intentional introduction of additional harmonic components on the transformer secondary voltage to compensate the grid current distortion.

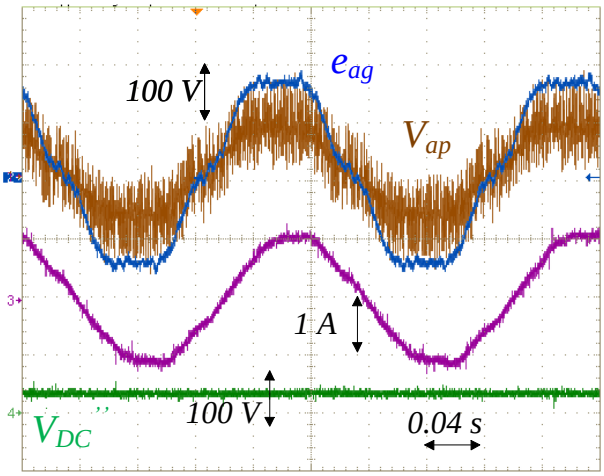


Fig. 4. 89 AHMLI Grid voltage synchronization with distorted grid voltage: Primary a-phase voltage of the transformer V_{ap}, a-phase grid voltage e_{ag}, a-phase magnetization current i_{ap} and TLI DC-Bus voltage V_{DC}''

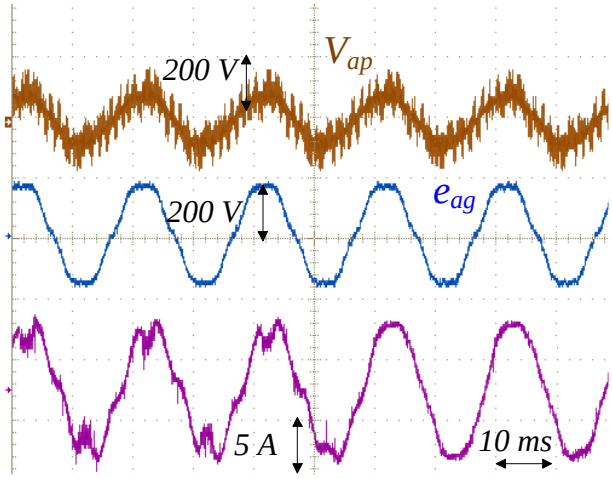


Fig. 4. 90 AHMLI System connected to the distorted grid: Primary a-phase voltage of the transformer V_{ap}, a-phase grid voltage e_{ag} with 5th and 7th harmonic components, a-phase grid current i_{ag}

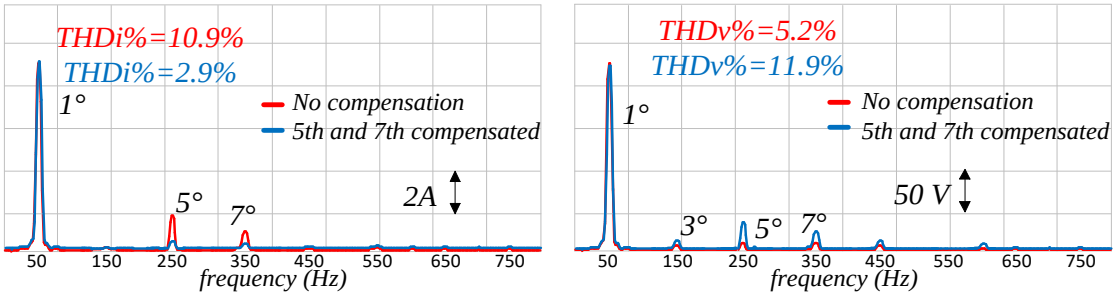


Fig. 4. 91 AHMLI Spectrum of grid current (left) and primary voltage V_{ap} (right) with and without additional control loop on 5th and 7th grid harmonic components.

4.3.3 AHMLI Conversion Efficiency for STATCOM and Generators

The total system efficiency η_{tot}, exploiting an open-end winding transformer has been experimentally measured for various output power levels, taking into account the 5MLI+TLI system configuration. It has been evaluated as the ratio between the output power P_{abcg} delivered to the grid and the MLI input power P_{in}.

$$\eta_{tot} = \frac{Pag+Pbg+Pcg}{Pin} \tag{4.48}$$

The block scheme of the system is shown in Fig. 4. 92.

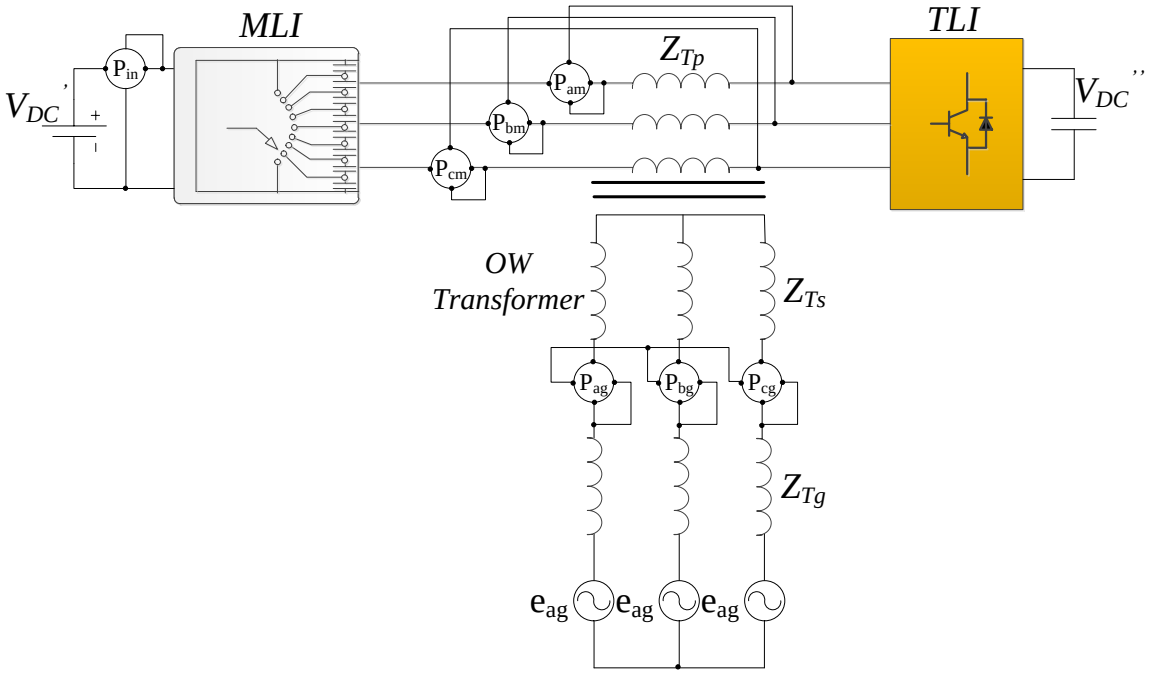


Fig. 4. 92 Experimental setup for measuring system efficiency on AHMLI for STATCOM and Generators

The total system efficiency η_{tot}, including the transformer efficiency, is plotted vs. the load ratio i_g/i_n in Fig. 4. 93 for two different values of V_{DC}''. The trend of the total efficiency is the same of the efficiency of a common transformer. Furthermore, lower is the TLI DC-Bus voltage V_{DC}'' lower is the efficiency, because the TLI doesn't fully compensate the undesired low order harmonic components.

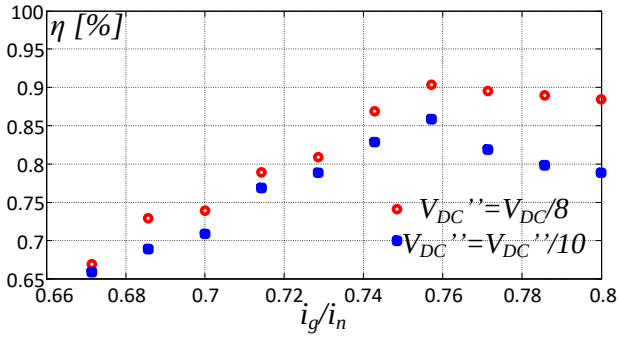


Fig. 4. 93 Conversion efficiency of the AHMLI system for STATCOM and Generators.

4.4 AHMLI for High-Speed Gen-Set Applications

Multilevel topologies have been recently proposed for use in power generating units, especially when power filter size, current and voltage THD are critical. This is the case of micro-turbine powered gen-set units, exploiting high speed permanent-magnet synchronous generators (HSPMSG) for more electric aircraft (MEA), distributed electric generation (DEG) and automotive applications [27], [28], [29], [30]. An application of the AHMLI concept is considered to realize a three-phase six-level Asymmetrical Hybrid Unidirectional T-Type Boost Rectifier (AHUTTBR) to be connected to a HSPMSG. Main design goals are efficiency, size, reliability, and cost. Several advanced rectifier topologies have been presented in literature, among them, the Vienna, Swiss, and T-type [31], [32]. An Asymmetrical Hybrid Unidirectional T-Type Boost Rectifier (AHUTTBR) is considered exploiting an Open-end Winding configuration, Fig. 4. 94, including a DC bus capacitors voltage equalization system. The PMSG generator is connected on one side to a three-level Unidirectional T-Type rectifier (3L-T RECT) working at a low switching frequency and on the other side, to a three phase two-level inverter (TLI) operating at high switching frequency. For cost reasons, the conventional Three-Level-T-Type inverter is modified by replacing the upper and lower switches with diodes, thus obtaining a unidirectional converter. The 3L-T RECT accomplishes a high efficiency step or staircase voltage modulation. The TLI is PWM modulated and shapes the AC generator current in order to obtain sinusoidal waveforms, to prevent additional power losses and torque ripple. The TLI is supplied through a floating capacitor C_f making a second independent power source redundant. In the scheme of Fig. 4.96,

E_{ag}, E_{bg} and E_{cg} are the back-EMFs of the PMSM generator, L_s is the inductance, V_{DC}' is the DC voltage rectified and V_{DC}'' is the floating capacitor voltage of the TLI.

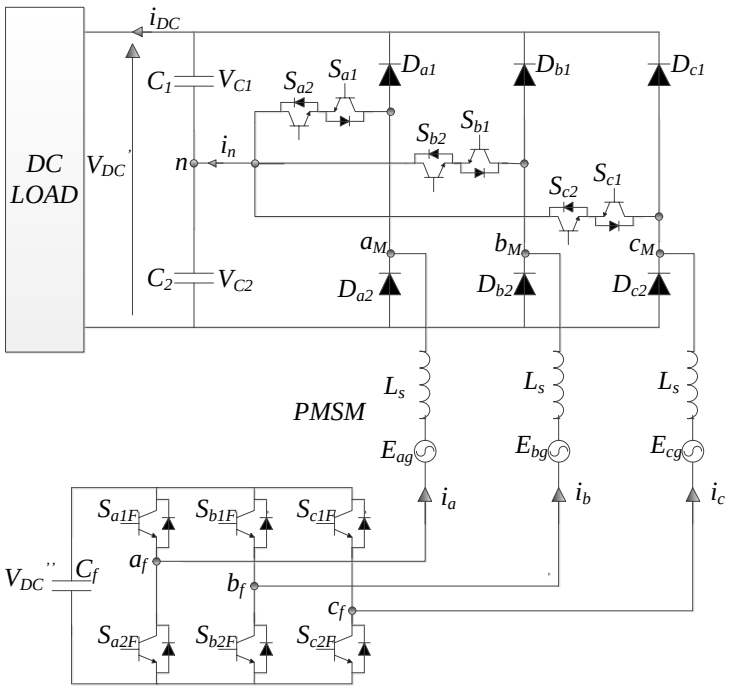


Fig. 4. 94 Asymmetrical Hybrid Unidirectional T-Type Boost Rectifier.

Bidirectional switches S_{a1}, S_{a2}, S_{b1}, S_{b2} and S_{c1}, S_{c2} are exploited to connect the midpoint *n* with the middle point of each phase leg to obtain a zero level voltage. They are operated at low frequency depending on the rectified DC-Bus voltage V_{DC}' and to the sign of the AC generator current. The mean value of the rectified voltage V_{DC}' can be controlled by acting on the switching angle α. Moreover, a three level modulation is accomplished, thus improving the harmonic content of the generator phase current namely; $+ V_{DC}'/2$, *0* and $- V_{DC}'/2$. The time in which the 0-level is produced is determined by acting on the switching angle α. The last is the output of a V_{DC}' control loop, as depicted in Fig. 4. 95. Table 4.6 shows the staircase voltage generation algorithm. Note that the power switches for each leg are turned on one at time, based on the sign of the phase current, minimizing the power losses.

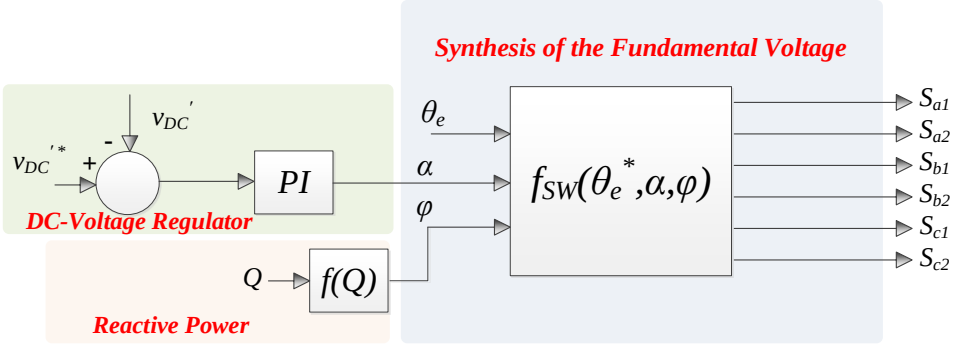


Fig. 4. 95 Block diagram of the voltage control algorithm.

Tab. 4.6 Table indicating the staircase voltage generation.

V_{aMn}	V_{bMn}	V_{cMn}
if $0<\theta_e<\alpha$ && $i_a>0$ $S_{a1}=1 \quad S_{a2}=0$ *if* $0<\theta_e<\alpha$ && $i_a<0$ $S_{a1}=0 \quad S_{a2}=1$	*if* $0<\theta_{(e-2/3*\pi)}<\alpha$ && $i_b>0$ $S_{b1}=1 \quad S_{b2}=0$ *if* $0<\theta_{(e-2/3*\pi)}<\alpha$ && $i_b<0$ $S_{b1}=0 \quad S_{b2}=1$	*if* $0<\theta_{(e+2/3*\pi)}<\alpha$ && $i_c>0$ $S_{c1}=1 \quad S_{c2}=0$ *if* $0<\theta_{(e+2/3*\pi)}<\alpha$ && $i_c<0$ $S_{c1}=0 \quad S_{c2}=1$

Fig. 4. 96 deals with simulation results obtained with a conventional three phase six pulse rectifier with L_s=350µH, C_1=C_2=80 µF, V_g=350 V peak and f=750Hz. The DC load consists of a resistance R=37Ω. The value of the rectified voltage V_{DC}' is 550 V. The generator current waveform is distorted, while, the DC voltage V_{DC}' shows a 1% ripple.

Two modulation regions can be identified namely: Mode 1 (α <27°) and Mode 2 (27°<α <45°). Fig. 4. 97 shows the output voltage in Mode 1. According to Fig. 4. 98 twelve converter states are possible, they are summarized in Table 4.7. The switching angle α affects the charge and discharge of the capacitors C_1 and C_2 and the DC voltage. In Mode 2, as shown in Fig. 4. 99, the state (111) causes a high generator current because the three stator inductances are short circuited, as described in Fig. 4. 100. Possible converter states are summarized in Table 4.8. In these conditions, the efficiency of the system rapidly decreases.

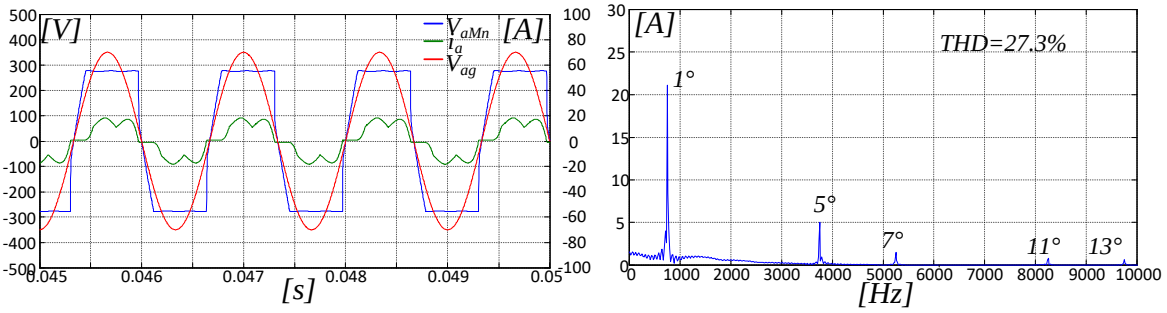


Fig. 4. 96 Conventional trhee phase rectifier: generator current i_a, 3L RECT output voltage V_{aMn} and generator voltage Vag (left). Harmonic spectrum of i_a

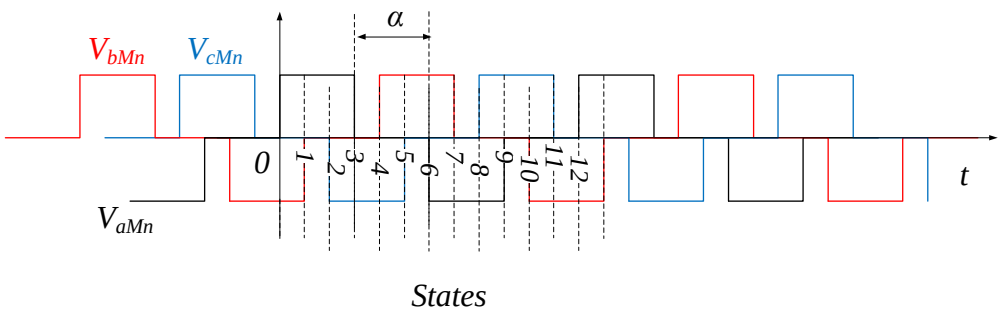


Fig. 4. 97 3L RECT: Mode 1.

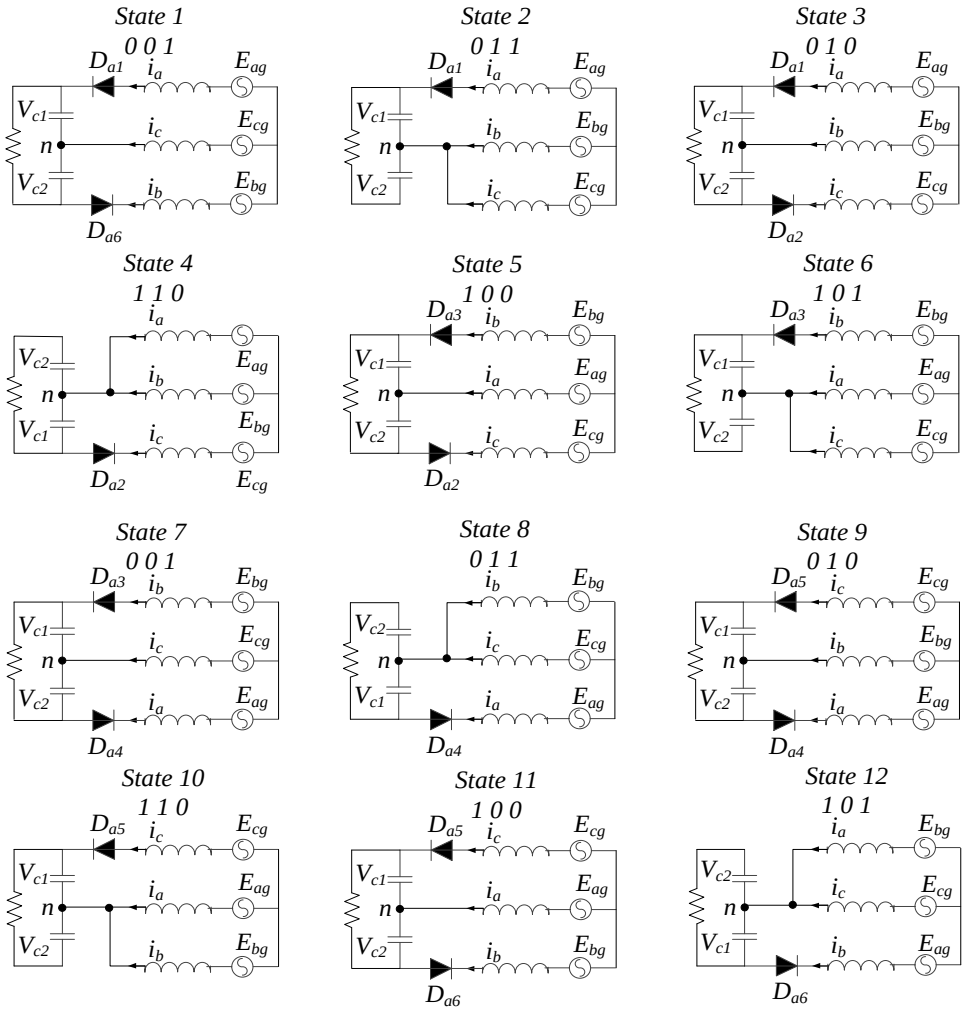


Fig. 4. 98 3L RECT: Voltage combinations in Mode 1

Tab. 4.7 Vector combination Mode 1: Charging and discharging of the DC-link capacitors.

S_1	S_2	S_3	i_{c1}	i_{c2}	C_1	C_2	V_{aMn}	V_{bMn}	V_{cMn}
0	0	1	$i_a >>$	$i_b <<$	Charge	discharge	$V_{DC}/2$	$-V_{DC}/2$	0
0	1	1	$i_a >>$	$-V_{DC}/R$	Charge	discharge	$V_{DC}/2$	0	0
0	1	0	$i_a <<$	$i_c >>$	Discharge	discharge	$V_{DC}/2$	0	$-V_{DC}/2$
1	1	0	$-V_{DC}/R$	$i_c >>$	Discharge	Charge	0	0	$-V_{DC}/2$
1	0	0	$i_b >>$	$i_c <<$	Charge	discharge	0	$V_{DC}/2$	$-V_{DC}/2$
1	0	1	$i_b >>$	$-V_{DC}/R$	Charge	discharge	0	$V_{DC}/2$	0
0	0	1	$i_b <<$	$i_a >>$	Charge	discharge	$-V_{DC}/2$	$V_{DC}/2$	0
0	1	1	$-V_{DC}/R$	$i_a >>$	Discharge	Charge	$-V_{DC}/2$	0	0
0	1	0	$i_c >>$	$i_a <<$	Charge	Discharge	$-V_{DC}/2$	0	$V_{DC}/2$
1	1	0	$i_c >>$	$-V_{DC}/R$	Charge	Discharge	0	0	$V_{DC}/2$
1	0	0	$i_c <<$	$i_b >>$	Discharge	Charge	0	$-V_{DC}/2$	$V_{DC}/2$
1	0	1	$-V_{DC}/R$	$i_b >>$	Discharge	Charge	0	$-V_{DC}/2$	0

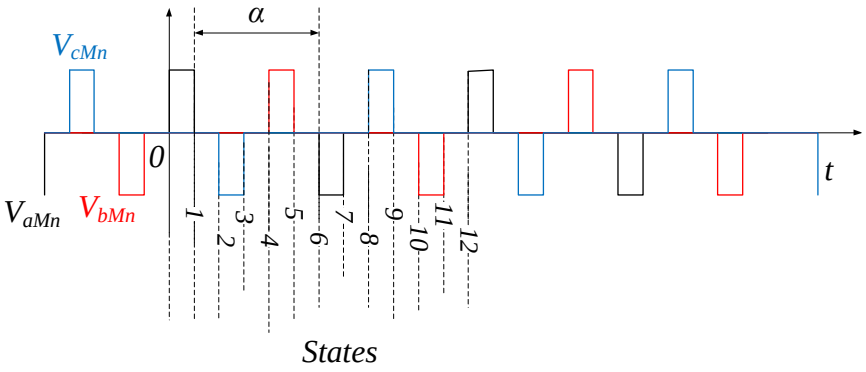


Fig. 4. 99 3L RECT: Mode 2.

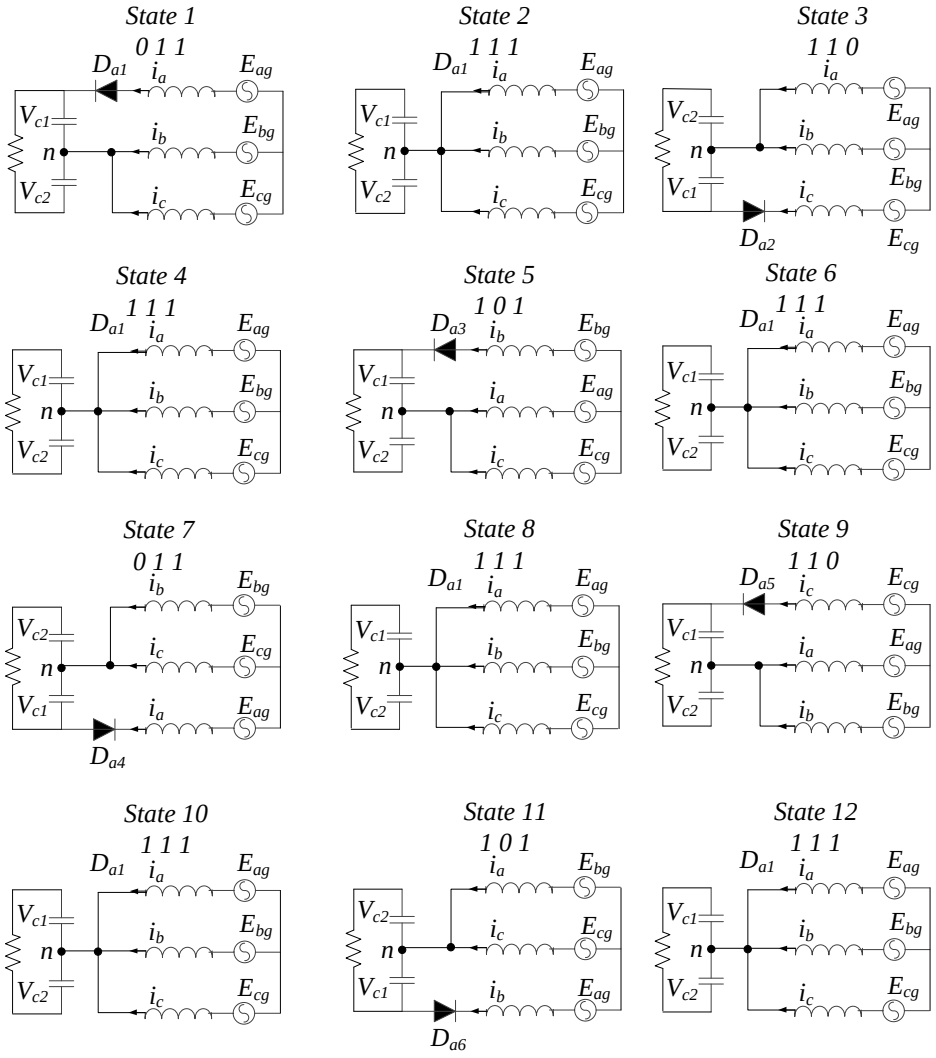


Fig. 4. 100 3L RECT: Voltage combinations in Mode 2

Simulation test have been carried out to investigate the system. In Mode 1 (0°<α<27°), it is possible to regulate the DC from 550V to 750V. As shown in Fig. 4. 101, by operating the converter in Mode 2 as a boost rectifier (27°<α<32.3°) V_{DC}' varies from 750V to 550V, while operating in Mode 2 as a buck rectifier (32.3°<α< 45°)

the voltage V_{DC}' varies from 550V to 0V. As, for α>27°, the the rms value of the generator current rapidly increases, reducing the efficiency, the optimal operation range is 0°<α< 27°.

Tab. 4.8 Vector combination Mode 2: Charging and discharging of the DC-link capacitors.

S_1	S_2	S_3	i_{c1}	i_{c2}	C_1	C_2	V_{aMn}	V_{bMn}	V_{cMn}
0	1	1	i_a >>	$-V_{DC}/R$	*Charge*	*discharge*	$V_{DC}/2$	*0*	0
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	*0*	0	0
1	1	0	$-V_{DC}/R$	i_c >>	*Discharge*	*charge*	*0*	0	$-V_{DC}/2$
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	0	0	*0*
1	0	1	i_b >>	$-V_{DC}/R$	*Charge*	*discharge*	0	$V_{DC}/2$	*0*
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	0	*0*	*0*
0	1	1	$-V_{DC}/R$	i_a >>	*Discharge*	*charge*	$-V_{DC}/2$	*0*	*0*
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	*0*	*0*	*0*
1	1	0	i_c >>	$-V_{DC}/R$	*Charge*	*discharge*	*0*	*0*	$V_{DC}/2$
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	*0*	*0*	*0*
1	0	1	$-V_{DC}/R$	i_b >>	*Discharge*	*charge*	*0*	$-V_{DC}/2$	*0*
1	1	1	$-V_{DC}/R$	$-V_{DC}/R$	*Discharge*	*discharge*	*0*	*0*	*0*

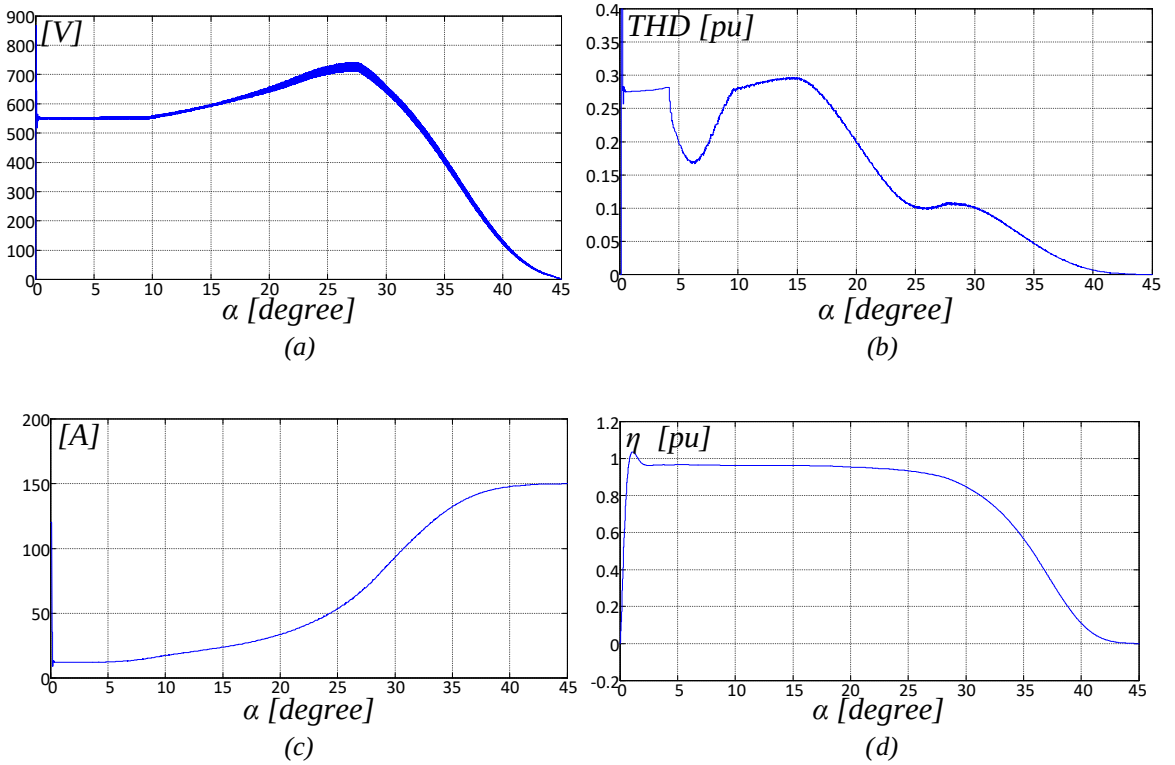


Fig. 4. 101 3L RECT without TLI filter: V_{DC}' vs α (a). THD of the generator current i_a vs α (b). Generator current i_a vs α (c). Efficiency vs α (d).

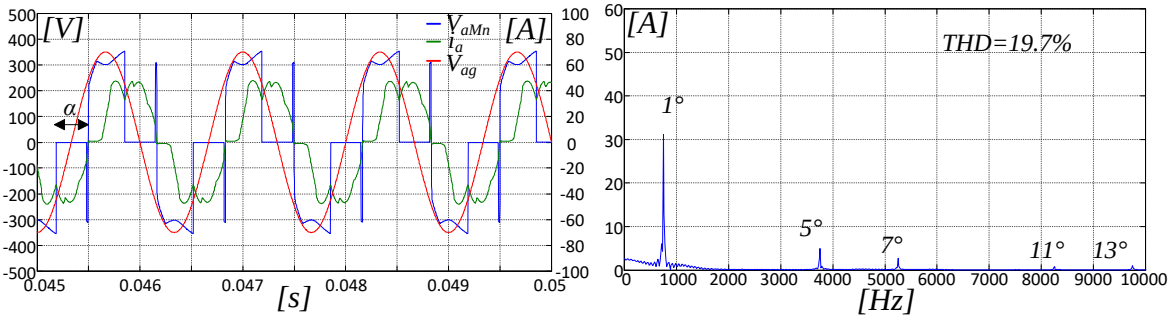


Fig. 4. 102 3L RECT without TLI filter: Generator current i_a, 3L RECT output voltage V_{aMn} and generator voltage V_{ag} (left). Harmonic spectrum of i_a

Some spikes are present in the 3L-T RECT output voltages $V_{abcMn,}$ due to the reactive power Fig. 4. 102(left). This issue can be overcome by acting on the additional angle φ in order to reduce the reactive power Q, although also the DC-Bus voltage V_{DC}' is modified, Fig. 4. 103.

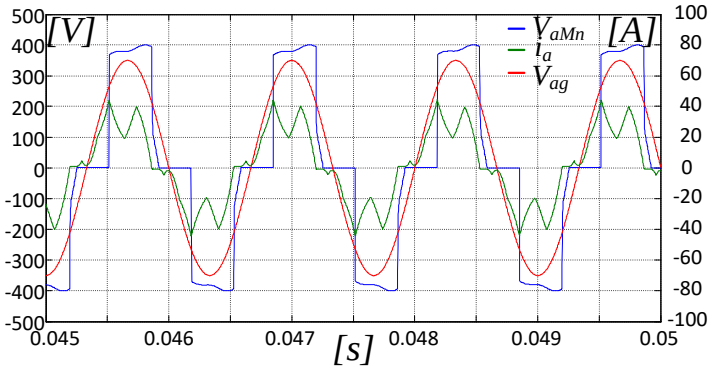


Fig. 4. 103 3L RECT without TLI filter and reduced reactive power: Generator current i_a, 3L RECT output voltage V_{aMn} and generator voltage V_{ag}

The TLI reference voltage consists of the difference between the 3L-T RECT output voltage V_{abcMn} and the fundamental component V_{abc1Mn} as shown in Fig. 4. 104. Fig. 4. 105 shows the TLI harmonic voltage reference V_{ah}^* when α=20° and V_{DC}' is 760 V.

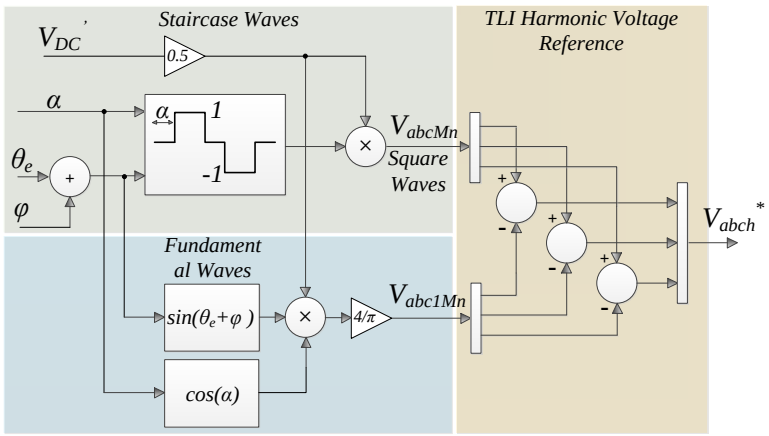


Fig. 4. 104 Block diagram of the V_{TLI} generation

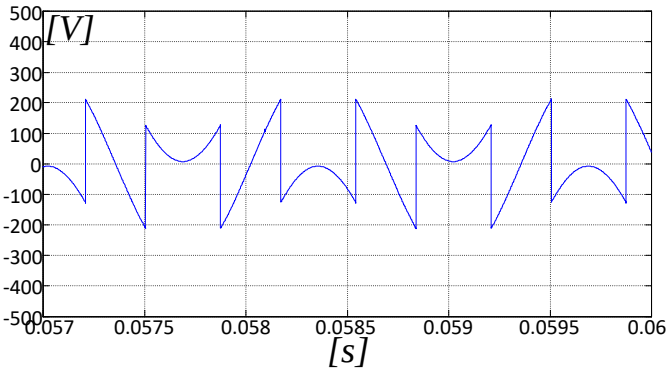


Fig. 4. 105 A-phaseTLI harmonic voltage reference V_{ah}^{*}

A suitable voltage control loop is implemented in order to control the TLI DC-Bus voltage, Fig. 4. 106. A further control loop acts on the DC-Bus voltage of the 3L-T RECT in order to balance the voltages across the capacitors C_1 and C_2. Hence the TLI voltage reference is given by:

$$\begin{aligned} V_{TLIabc}^{*} &= V_{TLIcap\_abc}^{*} + V_{MLIcap\_abc}^{*} + V_{abch}^{*} \\ V_{abch}^{*} &= V_{abcMn}^{*} - V_{abc1Mn}^{*} \end{aligned} \tag{4.49}$$

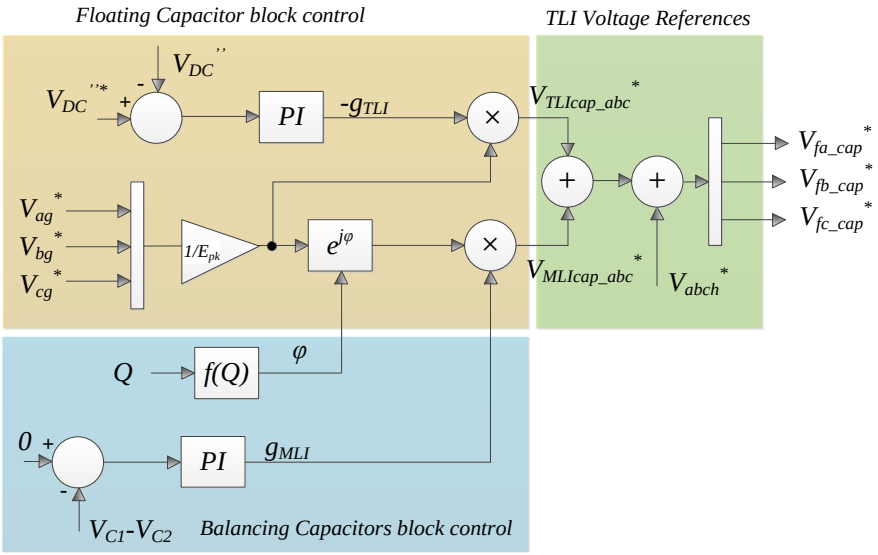


Fig. 4. 106 TLI voltage references

According with Fig. 4.109, the power equations are given by:

$$\begin{aligned} &P_{DC}'(t) + P_{MLI2}(t) + P_{MLI1}(t) + P_{TLI}(t) + P_{DC}''(t) = 0 \\ &P_{TLI}(t) = \eta_{TLI}(t) P_{DC}''(t) \\ &P_{MLI2}(t) = \eta_{MLI}(t) P_{MLI1}(t) \\ &P_{DC}''(t) = C_{TLI} \frac{d}{dt} V_{DC}''^{2}(t) \\ &P_{MLI2}(t) - C_1 \frac{d}{dt} V_{C1}^{2}(t) - C_2 \frac{d}{dt} V_{C2}^{2}(t) = P_{DC}'(t) = R i_{DC}^{2}(t) \end{aligned} \tag{4.50}$$

$$P_{MLI1}(t) = e_{ag}(t)i_a(t) + e_{bg}(t)i_b(t) + e_{cg}(t)i_c(t) - L\frac{d}{dt}i_a^2(t) - L\frac{d}{dt}i_b^2(t) - L\frac{d}{dt}i_c^2(t) = P_{TLI}(t) + P_{DC}''(t)$$
$$P_{TLI}(t) = \eta_{TLI}(t)P_{DC}''(t) = -\eta_{TLI}(t)C_{TLI}\frac{d}{dt}V_{DC}''^2(t) \quad (4.51)$$

The output of the TLI DC-Bus voltage controller is the fundamental input conductance g_{TLI} on the AC-side of the inverter. The generator phase currents can be expressed as:

$$i_a(t) = -g_{TLI}e_{ag}(t)$$
$$i_b(t) = -g_{TLI}e_{bg}(t) \quad (4.52)$$
$$i_c(t) = -g_{TLI}e_{cg}(t)$$

Combining eq. 4.52 and eq. 4.51:

$$P_{MLI1}(t) = -g_{TLI}(t)(e_{ag}^2(t) + e_{bg}^2(t) + e_{cg}^2(t)) - Lg_{TLI}^2(t)\frac{d}{dt}(e_{ag}^2(t) + e_{bg}^2(t) + e_{cg}^2(t))$$
$$= C_{TLI}\frac{d}{dt}V_{DC}''^2(t) - \eta_{TLI}(t)C_{TLI}\frac{d}{dt}V_{DC}''^2(t) \quad (4.53)$$

At steady state V_{DC}'' is constant and $P_{MLI1}=0$. Hence, the power P_{MLI1} is a function of the conductance g_{TLI}.

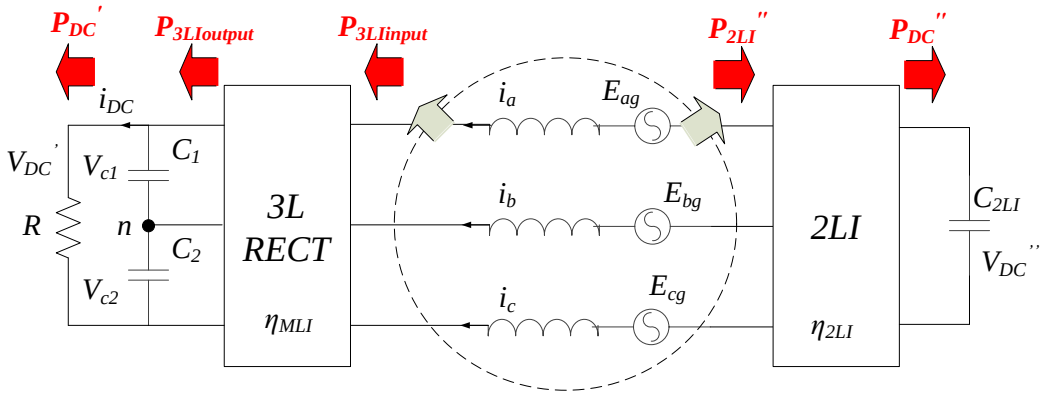


Fig. 4. 107 Power flows

The same approach can be used to balance the output capacitors voltage. The generator phase currents can be expressed as a function of g_{MLI}, considering that the reference voltages V_{ag}^*, V_{bg}^* and V_{cg}^* are shifted by angle φ.

$$i_a = g_{MLI}(t - t_\varphi)e_{ag}(t - t_\varphi)$$
$$i_b = g_{MLI}(t - t_\varphi)e_{bg}(t - t_\varphi) \quad (4.54)$$
$$i_c = g_{MLI}(t - t_\varphi)e_{cg}(t - t_\varphi)$$

According to Fig. 4.109, the power equations are given by:

$$P_{MLI2}(t-t_\varphi) = \eta_{MLI}(t-t_\varphi)P_{MLI1}(t-t_\varphi) = g_{MLI}\eta_{MLI}(e_{ag}^2(t-t_\varphi) + e_{bg}^2(t-t_\varphi) + e_{cg}^2(t-t_\varphi)) +$$
$$+ Lg_{MLI}^2(t-t_\varphi)\eta_{MLI}^2(t-t_\varphi)\frac{d}{dt}(e_{ag}^2(t-t_\varphi) + e_{bg}^2(t-t_\varphi) + e_{cg}^2(t-t_\varphi)) = \quad (4.55)$$
$$C_1\frac{d}{dt}V_{C1}^2(t) + C_2\frac{d}{dt}V_{C2}^2(t) + Ri_{DC}^2(t)$$

If V_{C1}= V_{C2} =constant, then P_{MLI2}=Ri_{DC}^2. Thus, the power P_{MLI2} is a function of the conductance g_{MLI}.

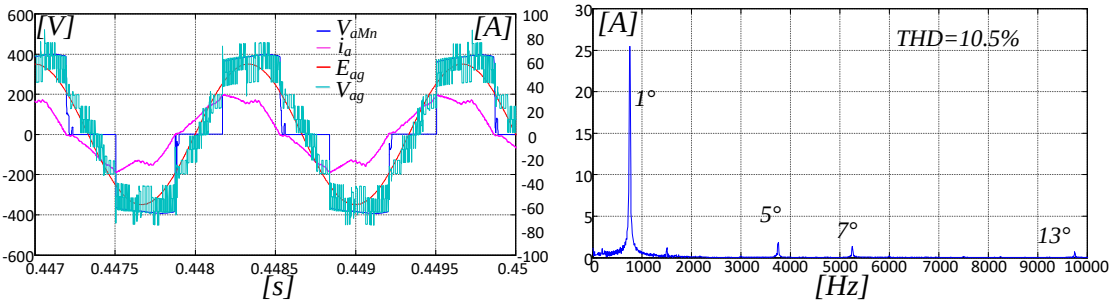


Fig. 4. 108 AHUTTBR rectifier with 12kH TLI: Generator current ia, 3L RECT output voltage VaMn, generator back-EMF Eag and phase generator voltage Vag(left). Harmonic spectrum of ia

The effectiveness of the active power filter is shown in Fig. 4. 108, where a reduction of the THD from 19.7% to 10.5% is observable.

Fig. 4. 109 shows the rectified voltage V_{DC}', the TLI DC-Bus Voltage V_{DC}'' and the capacitor voltages V_{C1} and V_{C2}, when α=20°, and V_{DC}''= 200 V. An unbalanced capacitor voltage condition is achieved by introducing an additional 500 Ω resistance in parallel to C_1. The capacitors voltage balance is active in 0<t<0.8s. In t=0.8s, the balance is deactivated. The ripple of V_{DC}' is measured in 5% V_{DC}'.

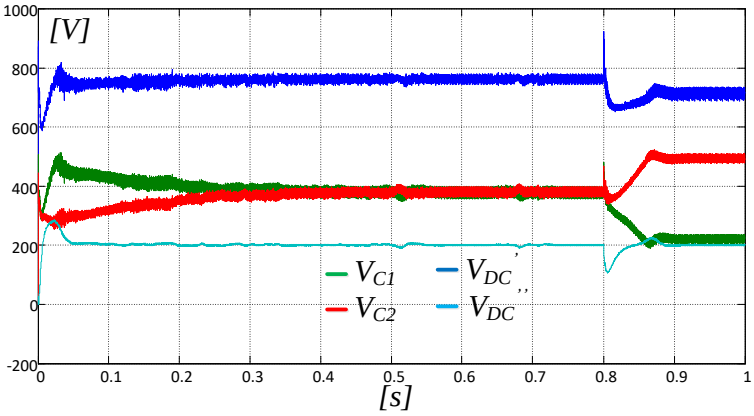


Fig. 4. 109 AHUTTBR rectifier: 3L RECT DC-Bus voltage V_{DC}', 3L RECT DC-Bus capacitor voltages V_{C1}, V_{C2} and TLI DC-Bus voltage V_{DC}''

The proposed AHUTTBR is compared with a conventional PWM 3L RECT with the same DC-Bus voltage V_{DC}'=750 V and amplitude of generator current. Fig. 4. 110 shows the generator current i_a and the THD which

is increased from 10.5%, with TLI, to 23.7%. Furthermore, unbalanced capacitor voltages are present in Fig. 4. 111.

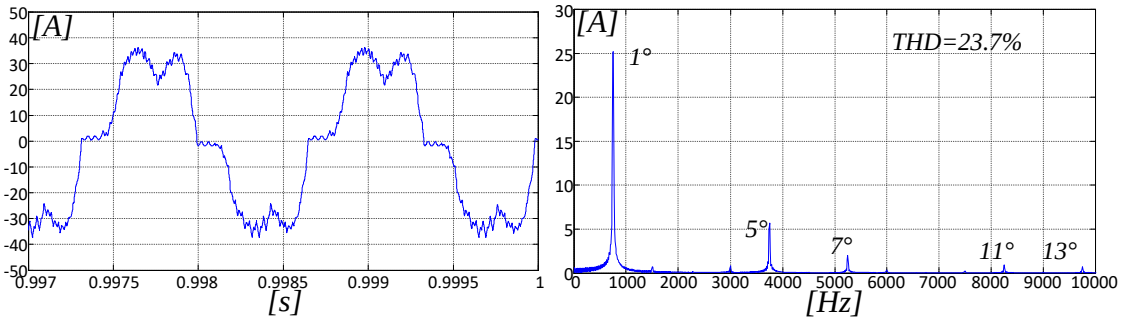


Fig. 4. 110 12kHz PWM 3L RECT rectifier: Generator current i_a(left). Harmonic spectrum of i_a

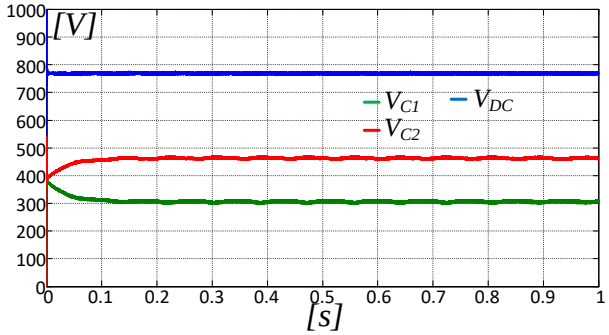


Fig. 4. 111 12kHz PWM 3L RECT rectifier: 3L RECT DC-Bus voltage V_{DC}, 3L RECT DC-Bus capacitor voltages V_{C1}, V_{C2}

4.5 References of Chapter 4

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5 Multi-Motor Drive Exploiting the AHMLI approach

Multi-Motor Drives are used in construction, container handling and in a number of industrial plants such as ironworks, paper mills and textile. A standard MMD is composed by at least two electrical motors, coupled on the load side through mechanical transmission devices, Fig. 5. 1.

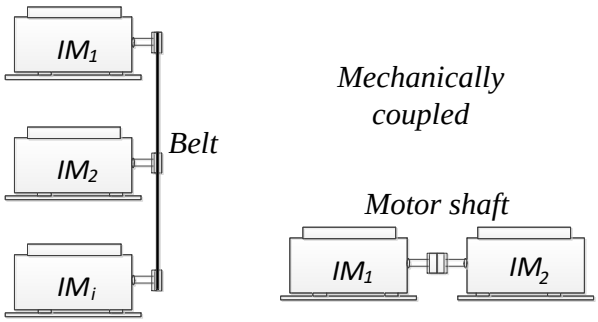

Fig. 5. 1 Multi-Motor Drives

The general equation of the coupling torque existing between two generic drives (*i* and *i+1*) of a MMD is:

$$m_{s,i,i+1} = K_p\left(\omega_i - \omega_{i+1}\right) + K_e\left(\theta_i - \theta_{i+1}\right) \tag{5.1}$$

where: K_p is the viscous damping coefficient, K_e is the saliency coefficient of the coupling material, and ω and θ are the motor shaft angular speed and angular position. Different coupling configurations may exist, namely:

- Rigid coupling $Kp \approx 0$ $Ke \rightarrow \infty$;
- Resilient coupling, $Kp \approx 0$ $Ke \neq 0$;
- Viscous damping coupling, $Kp \neq 0$ $Ke \approx 0$;
- Uncoupling, $Kp \approx 0$ *i* $Ke \approx 0$.

Based on the structure of the power converter, MMDs are classified into two main groups:

1. Multiple Motors fed by Single Converter (MMSC)
2. Multiple Motors fed by Multiple separated Converters (MMMC)

In a MMSC, only one converter is adopted to control all motors and the torque load is proportionally divided among the motors, as depicted in (left). An individual motor torque-control is impossible and the load sharing is determined by motor torque-speed characteristic. To overcame this problem, a MMMC can be used where each motor is fed by

one converter, Fig. 5. 2(right). The torque contribution of each motor can be separately set by acting on the specific converter [5]. MMD systems with rigid coupling require only one speed controller, therefore, only one power converter can feed all the motors. However, on medium and high power drives, the use of a separate converter for each motor is generally required. In this case the load distribution is accomplished at the control level, tasking each motor to provide a fraction of the total load proportional to its size.

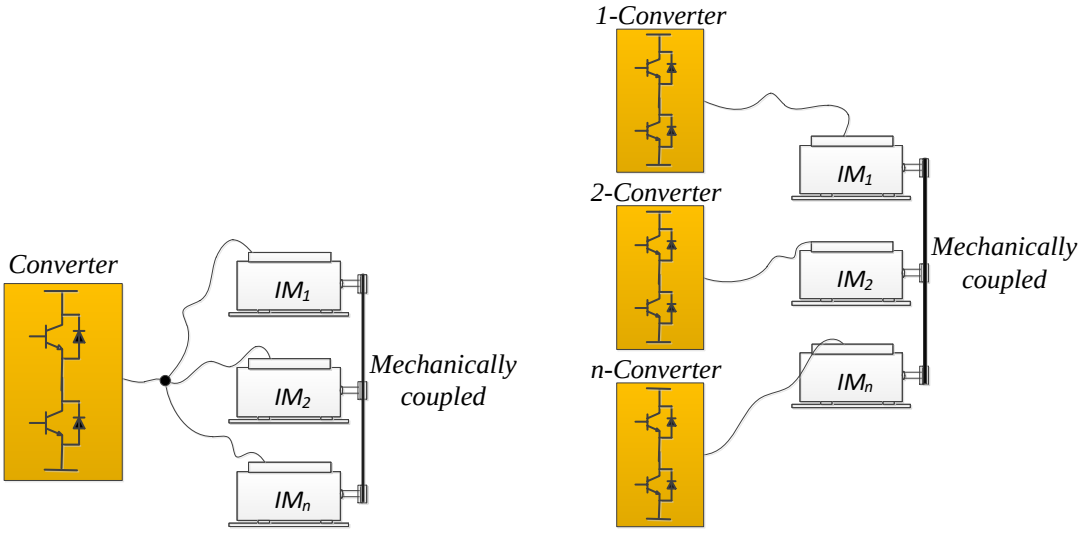

Fig. 5. 2 Multiple Motors fed by Single Converter (MMSC) (left). Multiple Motors fed by Multiple separated Converters (MMMC) (left).

The common speed controller determines the total torque reference, as shown in Fig. 5. 3, where: T_{e1} and T_{e2} are the electromagnetic torques of the two motors and K_1 and K_2 two factors depending on the power rating of the motors.

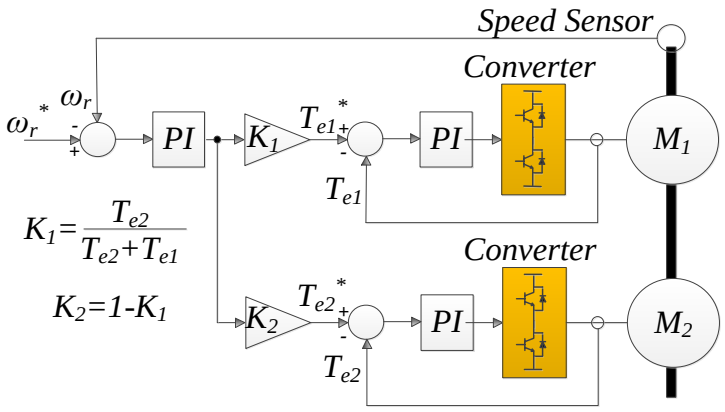

Fig. 5. 3 Two rigidly coupled drives, with separate power converters

On MMDs with resilient and viscous damping couplings, each drive must be speed controlled, thus, it must have its own controller, speed sensor, and the separate converter, Fig. 5. 4. The same considerations apply for uncoupled MMDs.

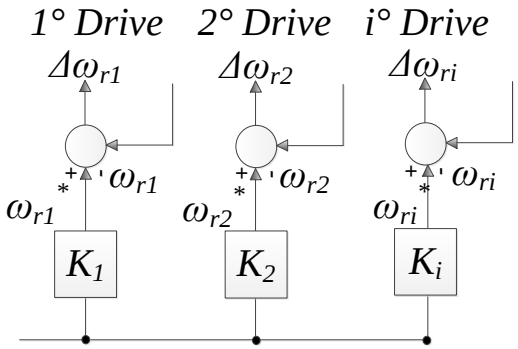

Fig. 5. 4 Resilient coupled drives, with separate power converters

A typical MMD applications is on cranes. Cranes featuring different size and structures are largely used for handling heavy loads in the metallurgy, paper and cement industry, as well as in transport for loading and unloading of containers and in the construction for the movement of materials, Fig. 5. 5.

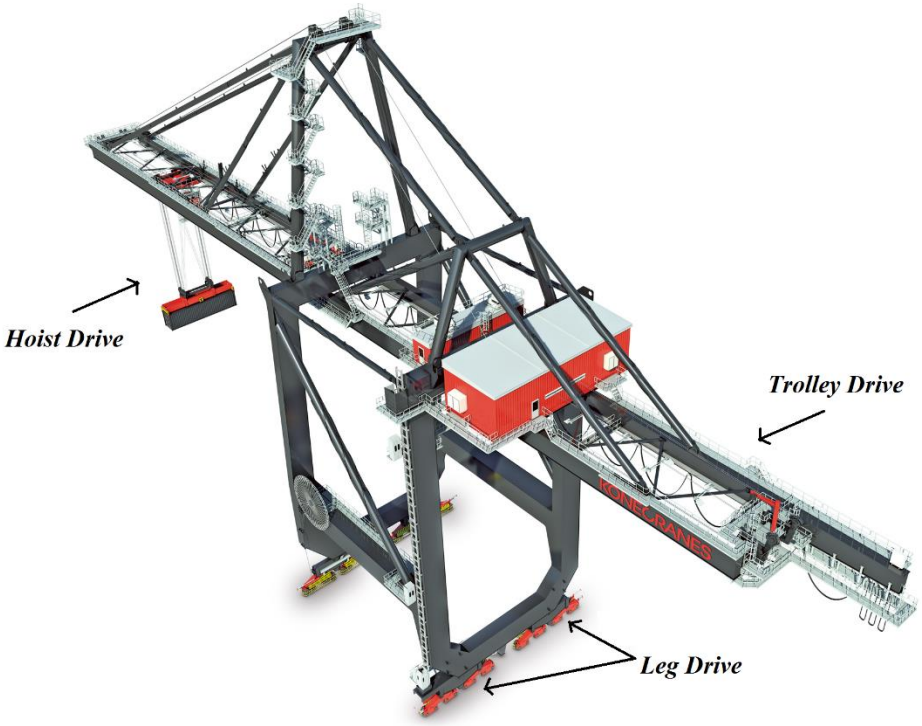

Fig. 5. 5 Rail mounted gantry crane.

Early electrically operated cranes were equipped with grid connected wound rotor Induction Motors (IM). Speed control was achieved through rotor resistors and electro-mechanical contactors and braking by plugging. Variable speed four quadrant thyristor based DC motor drives were subsequently introduced in an effort to improve the efficiency [1]. Last generation cranes finally switched to more efficient, compact and robust digitally controlled AC motor drives [2], [3]. Main advantages of this solution are precise positioning of the load by torque control at very low and zero speed, reduction of load swing by acceleration control and improved efficiency by regenerative braking.

Moreover, an increased motor lifetime is achieved because a lower voltage is applied at the starting, thus leading to lower in-rush currents. As a result, AC motor drives not only are today the standard equipment of modern cranes, but they are also progressively replacing wound rotor IM and DC drives on revamped old cranes [4]. Large size cranes very often exploit MMDs which are less expensive than a set of single motor drives, while, if compared to a single large drive, their inner redundancy can be exploited to mitigate the effects of motor faults [5]-[7].

5.1 Proposed Open-end Winding Multi-Motor Drives (OW MMDs)

Two novel multi-level inverters multi-motor drive topologies for crane applications have been developed exploiting the AHMLI configuration [11]. A key feature of the proposed multi-motor systems is that each motor is connected to a single multilevel inverter from one side and, on the other side, to a two-level inverter acting as an active power filter, [7]. The two proposed MMDs configuration are:

1. Open-end Winding Multi-Motor-Single-Converter (OW MMSC)
2. Open-end Winding Multi-Motor-Multi-Converters (OW MMMC)

The OW MMSC exploits a three-phase two level inverter as active power filter, Fig. 5. 6, while the OW MMMC uses a five-leg two level inverter (TLI5), Fig. 5. 7. The main difference between the two configuration is that, the load sharing between the two motor can be controlled by exploiting the TLI5.

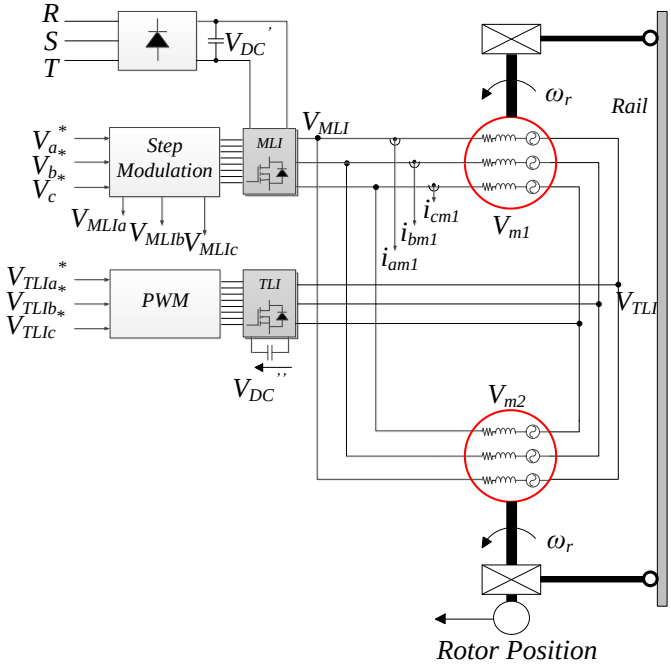

Fig. 5. 6 Proposed OW MMSC

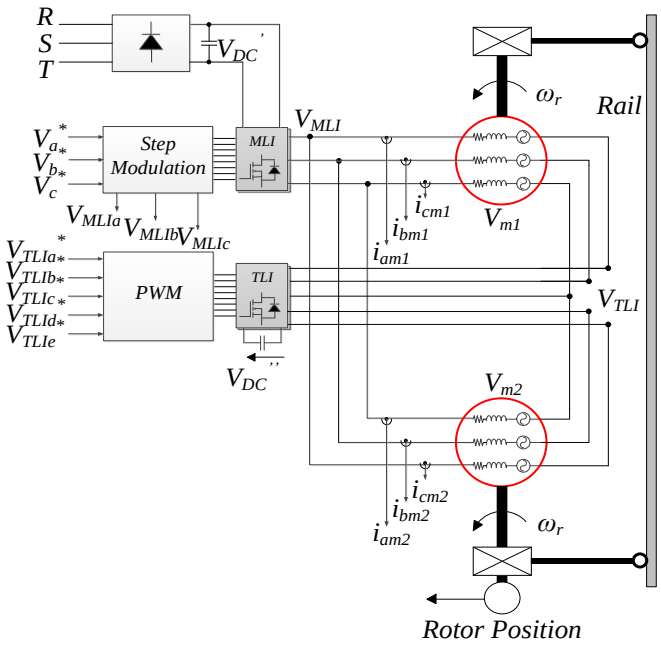

Fig. 5. 7 Proposed OW MMMC

5.1.1Open-end Winding Multi-Motor Single Converter

The dual machine structure of Fig. 5. 6 consists of two Open-end Winding (OW) induction motors, IM1 and IM2, connected on one side to a Multi-Level Inverter (MLI) and on the other side to a Two-Level Inverter (TLI). Both machines are rigidly mechanically coupled, which means that they run at the same mechanical speed ω_r, moreover, they are also electrically connected in parallel, thus an independent torque control is impossible. Fig. 5. 8 shows the equivalent circuit of the proposed OW MMSC. The two motors are fed by the same three-phase set of voltages, thus:

$$\begin{aligned} V_{am2} &= V_{am1} \\ V_{bm2} &= V_{bm1} \\ V_{cm2} &= V_{cm1} \end{aligned} \tag{5.2}$$

According to the AHMLI approach, a staircase voltage modulation based on a harmonic elimination technique is adopted on the MLI in order to minimize switching losses, while the TLI exploits a high frequency PWM strategy to shape the motor currents. The voltage control system is shown in Fig. 5. 9. In order to eliminate voltage harmonics generated by the MLI staircase voltage modulation from the motors phase voltages the reference voltage of the TLI PWM modulator is set to:

$$V_{TLIabc}^{*} = V_{MLIabc} - V_{abc}^{*} \tag{5.3}$$

being V_{abc}^{*} the fundamental component of the reference voltage.

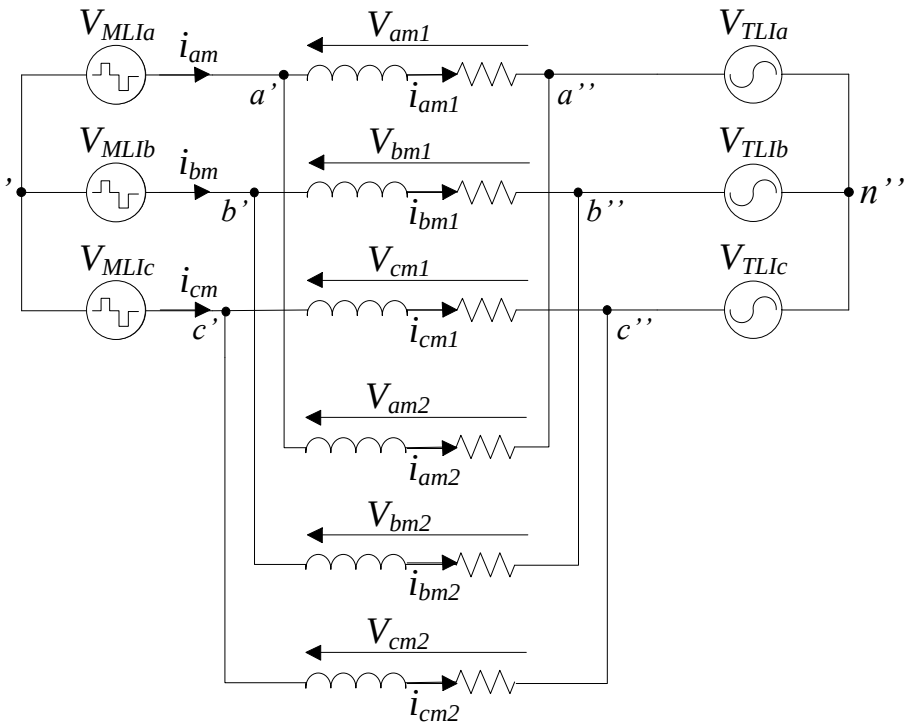

Fig. 5. 8 Equivalent circuit of the proposed OW MMSC

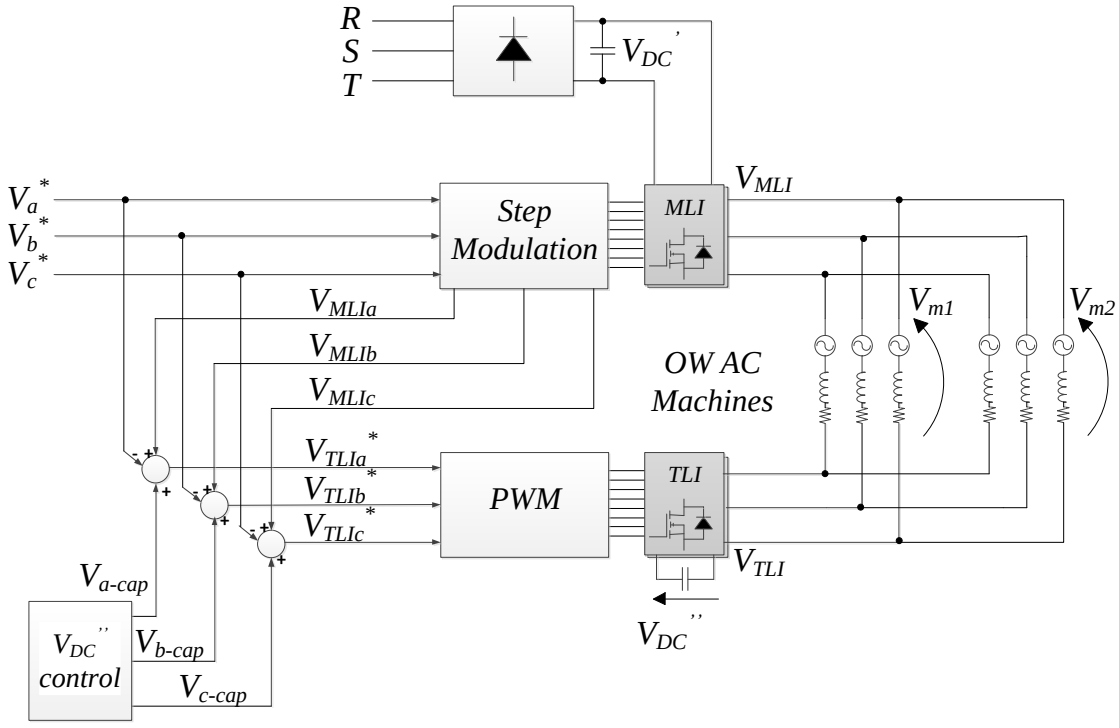

Fig. 5. 9 Voltage control system for the proposed OW MMSC

Simulation tests proved the consistence of the proposed approach in a constant *V/f* induction motor control application. A 5LI is used as main inverter, with V_{DC}'=500 V and a TLI as active filter operating at 5kHz, V_{DC}''=70 V. Since the two motor are rigidly coupled, the mechanical equation is given by:

$$T_{e1} + T_{e2} = T_L + j\frac{d\omega_r}{dt} + \mathrm{F}\omega_r \tag{5.4}$$

being ω_r the common mechanical speed of the two motors, T_{e1} and T_{e2} the electromagnetic torques of IM1 and IM2 respectively, T_L the load torque and F the friction coefficient. Fig. 5. 10 shows the mechanical speed of both motor while Fig. 5. 11 depicts the electromagnetic torques T_{e1} and T_{e2} when a 10 Nm load torque is applied to the motors shaft. The stator currents i_{abcm1}, i_{abcm2}, the total phase currents of both motors and the phase voltage are shown in Fig. 5. 12 and Fig. 5. 13, respectively. The MLI generates a staircase phase voltage, Fig. 5. 14(left) and, while, the difference between the MLI output voltage V_{MLIabc} and the fundamental voltage V_{abc}^* is produced by the TLI, Fig. 5. 14(right). Since the two motors are of the same type and size, they produce the same torque, while running at the same speed. Therefore, the harmonic compensation terms V_{TLIabc}* are the same for both motors. The phase motor voltages of the two motors V_{abcm} assume the waveforms depicted in Fig. 5. 15(left). Fig. 5. 15 (right) shows in detail the motor stator currents, whose waveforms are almost sinusoidal.

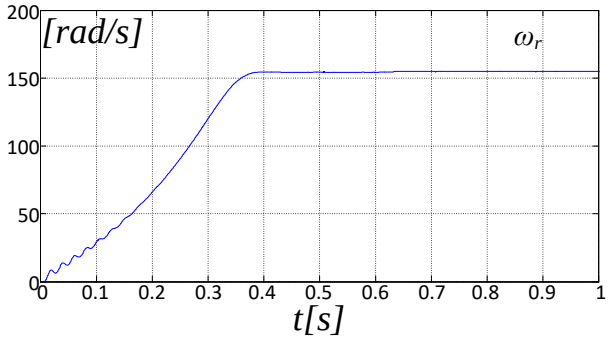

Fig. 5. 10 OW MMSC V/f control: Mechanical speed of IM1 ω_{r1}(left). Mechanical speed of IM1 ω_{r2} (right)

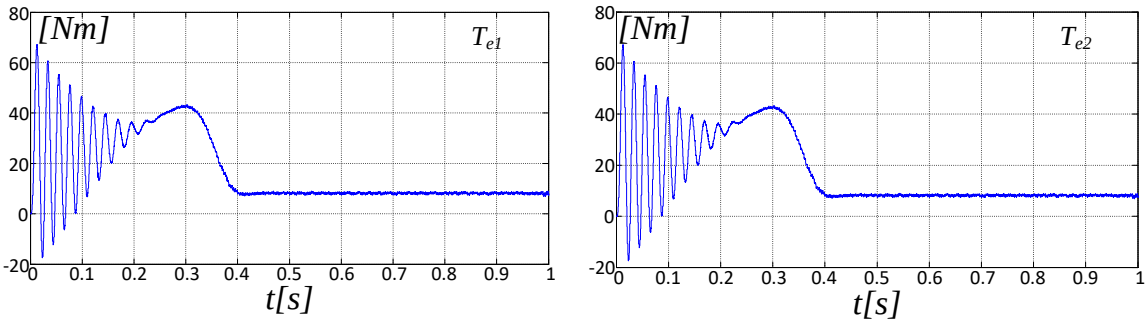

Fig. 5. 11 OW MMSC V/f control: Electromagnetic Torque of IM1 T_{e1}(left). Electromagnetic Torque of IM1 T_{e2} (right)

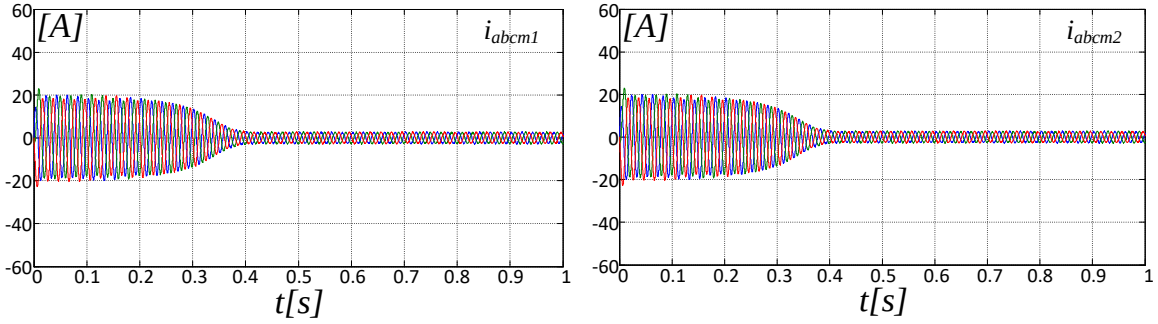

Fig. 5. 12 OW MMSC V/f control: Phase motor currents of IM1i_{abcm1}(left). Phase motor currents of IM1i_{abcm2}(right).

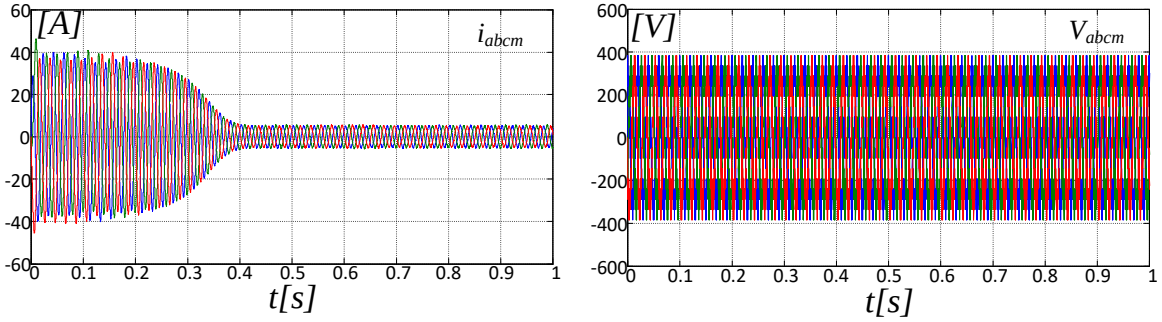

Fig. 5. 13 OW MMSC V/f control: Phase total motor currents of both motors i_{abcm}(left). AHMLI output phase voltages V_{abcm}(right).

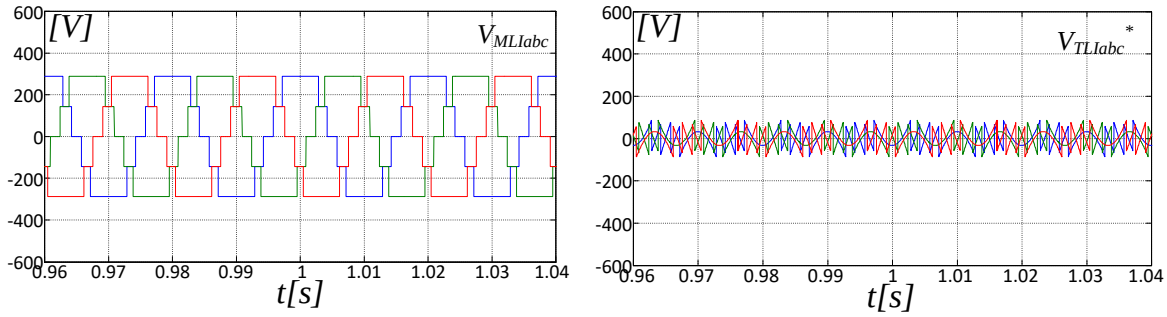

Fig. 5. 14 OW MMSC V/f control: MLI Staircase output phase voltages V_{MLIabc}(left). TLI reference voltages V_{TLIabc}(right)*

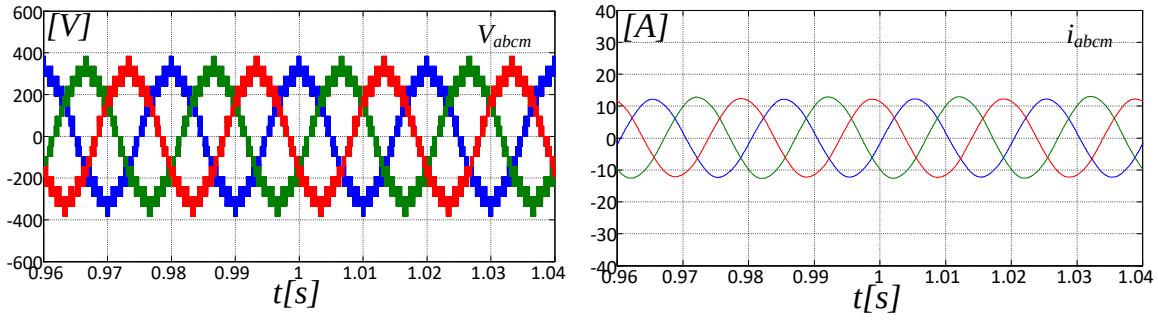

Fig. 5. 15 OW MMSC V/f control: AHMLI output phase voltages V_{abcm}(left). Phase currents of both motors i_{abcm}(right)

A comparison between the AHMLI system, a system with two wye-connected motors fed by a PWM MLI and a system with two wye-connected motors fed by a Step modulated MLI, has been accomplished in terms of current harmonic content and torque ripple. The stator currents and the torque ripple of the two motors are shown in Fig. 5.

16, Fig. 5. 16, Fig. 5. 17, Fig. 5. 16, Fig. 5. 20 and Fig. 5. 21. The first two systems give substatially the same results, while the third one shows a remarkably larger torque ripple, because the stator currents contain higher low order harmonic components, Fig. 5. 20 and Fig. 5. 21.

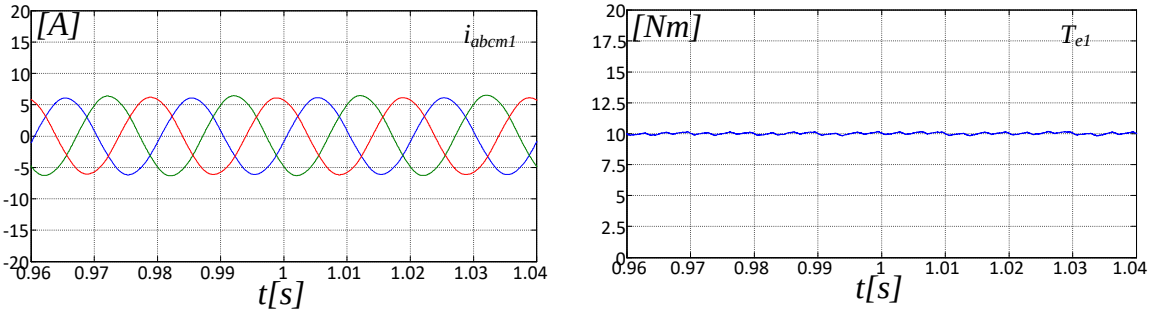

Fig. 5. 16 OW MMSC V/f control: Motor phase currents of IM1 i_{abcm1} (left). Torque ripple of IM1 T_{e1}(right)

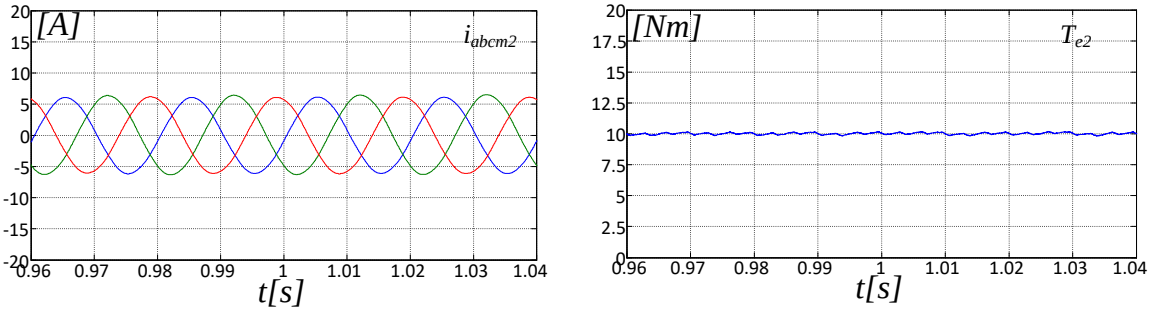

Fig. 5. 17 OW MMSC V/f control: Motor phase currents of IM2 i_{abcm2} (left). Torque ripple of IM2 T_{e2}(right)

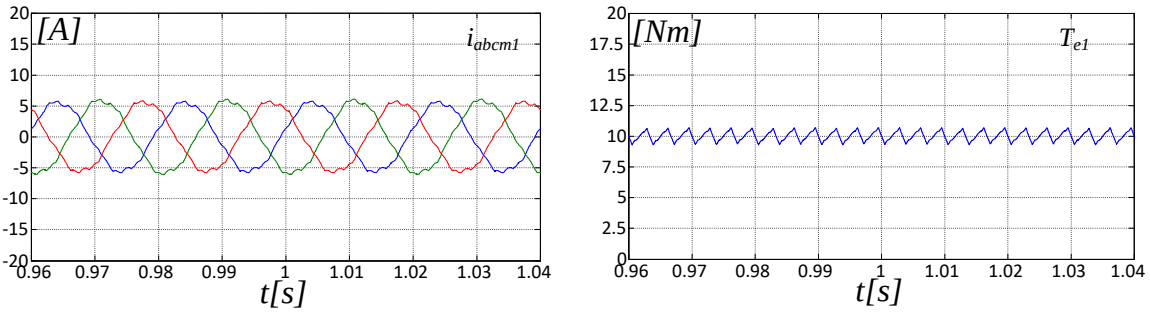

Fig. 5. 18 PWM MMSC V/f control: Motor phase currents of IM1 i_{abcm1} (left). Torque ripple of IM1 T_{e1}(right)

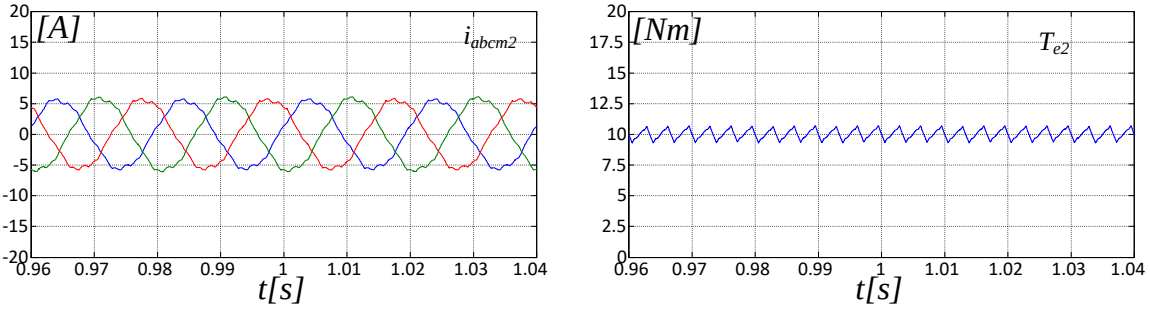

Fig. 5. 19 PWM MMSC V/f control: Motor phase currents of IM2 i_{abcm2} (left). Torque ripple of IM2 T_{e2}(right)

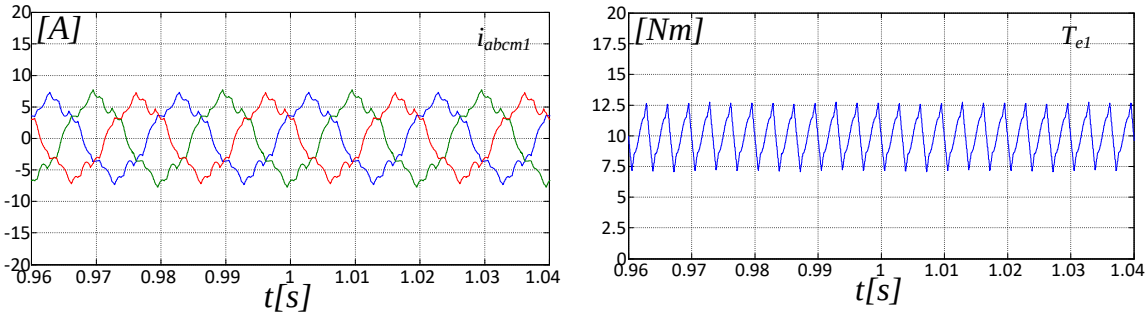

Fig. 5. 20 Wey-connected MLI Step modulated MMSC V/f control: Motor phase currents of IM1 i_{abcm1} (left). Torque ripple of IM1 T_{e1}(right)

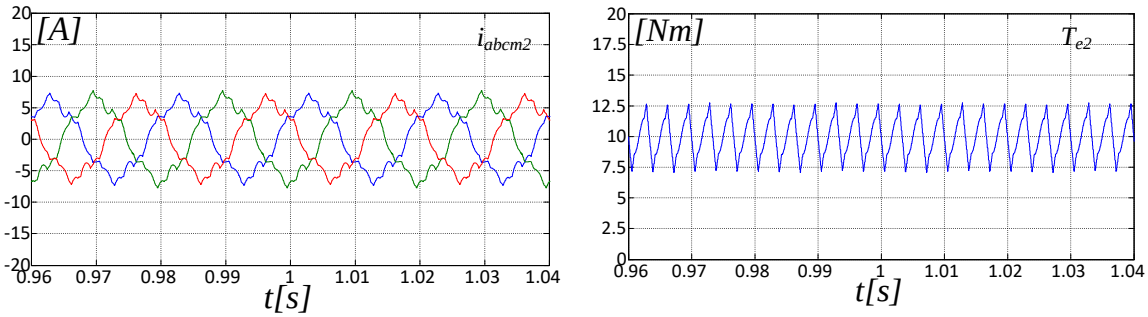

Fig. 5. 21 Wey-connected MLI Step modulated MMSC V/f control: Motor phase currents of IM2 i_{abcm2} (left). Torque ripple of IM1 T_{e2}(right)

A suitable current control strategy has been developed starting from the voltage control system of Fig. 5. 9. As schematized in Fig. 5. 22, it belongs to the class of synchronous current regulators, acting on rotating d,q axes components of the current and encompasses two different subsystems, respectively acting on the MLI and the TLI. The current feedback consists of the sum of stator currents of IM1 and IM2, as it is supposed that they are the same. The MLI current control subsystem is tasked to decouple the q,d axes regulation and is of the predictive type. The q,d axes voltage references are the back EMF components E_q* and E_d*, which, assuming the two machines identical, are estimated as:

$$\begin{aligned} E_q^* &= \omega_{\lambda r} L_s i_d^* \\ E_d^* &= -L_K \omega_{\lambda r} i_q^* \\ \omega_{\lambda r} &= \frac{Rr}{Lr}\frac{iq^*}{id^*} + \omega_r \end{aligned} \tag{5.5}$$

and:

$$L_K = \left(\frac{L_r L_s - L_m^2}{L_r}\right) \tag{5.6}$$

where: $\omega_{\lambda r}$ and ω_r are respectively the rotor flux angular speed and the rotor speed of the two machines, while *Ls*, *Lr* and *Lm* are respectively the stator, rotor and magnetizing inductances.

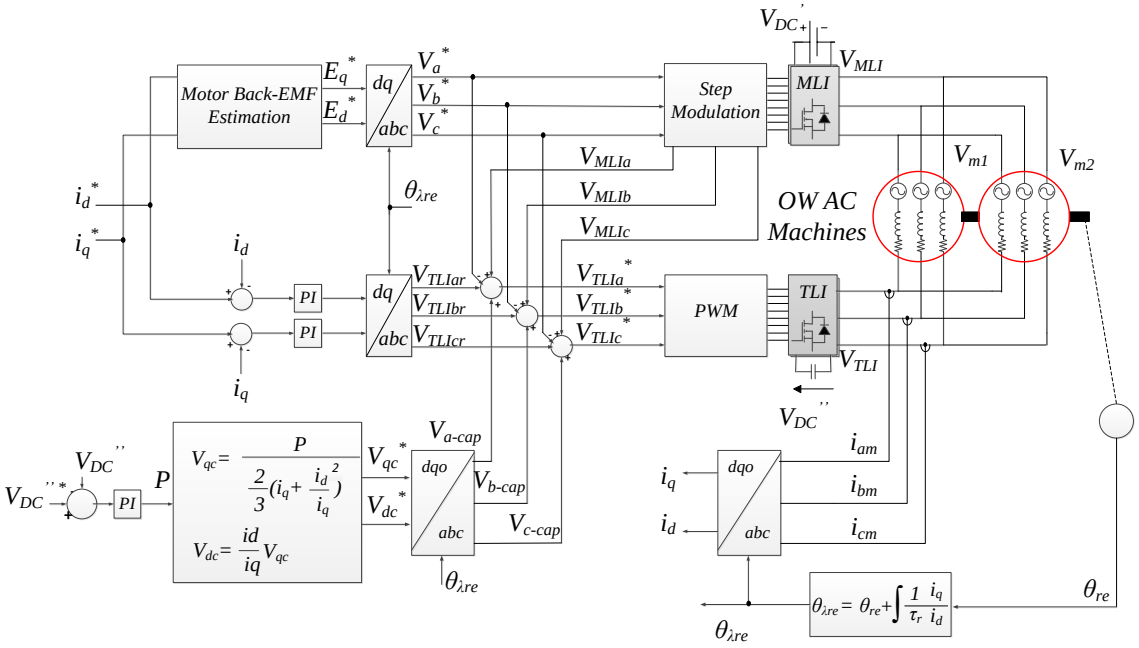

Fig. 5. 22 OW MMSC configuration current control system.

The TLI current control subsystem acts as the main closed loop regulator, controlling the total phase current taking advantage from the PWM fast dynamic and precision. Moreover, exploiting the same mechanisms introduced in the voltage control scheme, it predictively compensates low order stator voltage harmonics generated by the MLI and stabilizes V_{DC} ''. Thus, the reference voltage of the TLI is determined as:

$$V_{TLIabc}^{*} = V_{TLIabcr} + (V_{MLIabc} - V_{abc}^{*}) + V_{abc-cap} \tag{5.7}$$

being $V_{abc\text{-}c}$ the additional term needed to control the TLI DC-Bus voltage V_{DC} '' and $V_{TLIabcr}$ the output of the current control loop. The qd-axes reference currents are set to:

$$\begin{aligned} i_{d1}^{*} &= i_{d2}^{*} = i_d^{*} \\ i_q^{*} &= \frac{1}{2}(i_{q1}^{*} + i_{q2}^{*}) \end{aligned} \tag{5.8}$$

A speed reversal from ω_r *=-40rad/s* to ω_r *=40rad/s* accomplished by a 5LI+TLI MMSC system is shown in Fig. 5. 23 and Fig. 5. 24 for the two motors. The system features a good dynamic response. Moreover, q-axis and d-axis components of rotor flux of the two motors are almost coincident, as shown in Fig. 5. 24(right).

Experimental validations of the proposed OW MMSC drive structure have been performed on two scaled prototypes respectively 3LI+TLI and 5LI+TLI whose rated power is 3kVA. The two induction machines are mechanically coupled, while the drives are controlled by means of a single control board. The carrier frequency

of the sine-PWM is 10kHz, while a 1μs dead time is introduced. The DC-Bus V_{DC}' of the MLI is 400V, while $V_{DC}''=V_{DC}'/2(n-1)$. Induction motors parameters are listed in Table 5.1, while technical specification of IGBT assuming to equip the inverters are reported in Table 5.2. A 480mF floating capacitor is also utilized.

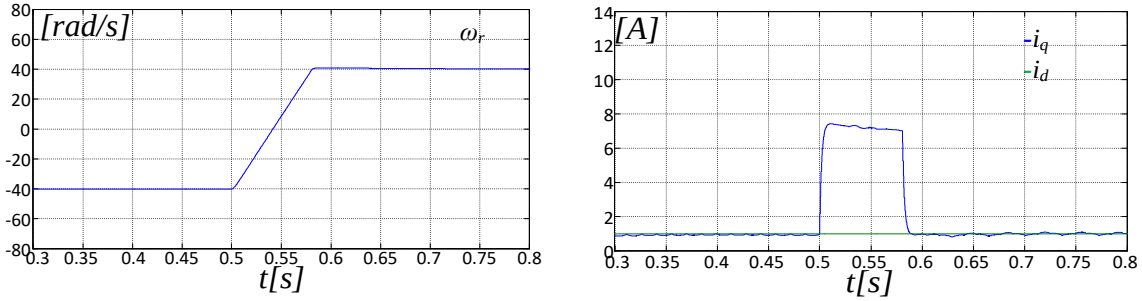

Fig. 5. 23 OW MMSC Speed reversal simulation test: Speed motor(left), qd-axes currents(right)

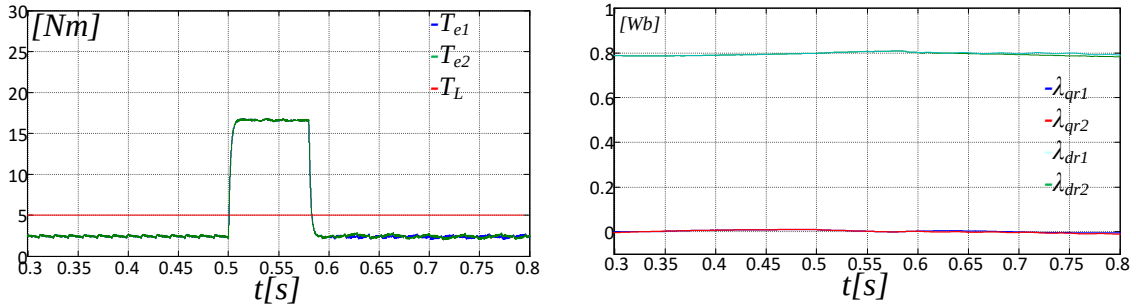

Fig. 5. 24 OW MMSC Speed reversal simulation test: Electromagnetic Torque of two motors and load torque(left), q-axis and d-axis components of rotor flux of the two motors(right)

Tab. 5.1 Induction Machine data.

Motor I								
Pn (HP)	***Vn (V)***	***pp***	***Ls (mH)***	***Lr (H)***	***Lm (H)***	***Rs (Ω)***	***Rr (Ω)***	***J (Kg.m²)***
50	*400*	*2*	*0.031*	*0.031*	*0.03*	*2.5*	*2.7*	*0.016*
Motor II								
Pn (HP)	***Vn (V)***	***pp***	***Ls (mH)***	***Lr (H)***	***Lm (H)***	***Rs (Ω)***	***Rr (Ω)***	***J (Kg.m²)***
50	*400*	*2*	*0.031*	*0.031*	*0.03*	*0.1*	*0.06*	*0.016*

Tab. 5.2 Inverter IGBT data

T_j (C°)	V_{ceo} (V)	R_{ce} (mΩ)	V_{feo} (mΩ)	R_{fe} (mΩ)	t_{ont} (ns)	t_{offT} (ns)	t_{offD} (ns)
150	*0.75*	*6.3*	*0.9*	*3.8*	*60*	*131*	*53*

A remarkable distortion of the stator current is observable in Fig. 5. 25, dealing with results obtained on the system supplied by a step modulated 5MLI. The test has been performed at ω_r =70rad/s and no load exploiting

a rotor flux field oriented control. When adopting the MMSC scheme of Fig. 5. 6, the THD is considerably improved, as clearly visible in Fig. 5. 27. In Fig. 5. 6, a comparison is made between two systems exploiting the proposed scheme, one equipped with a 3LI and the other with a 5LI.

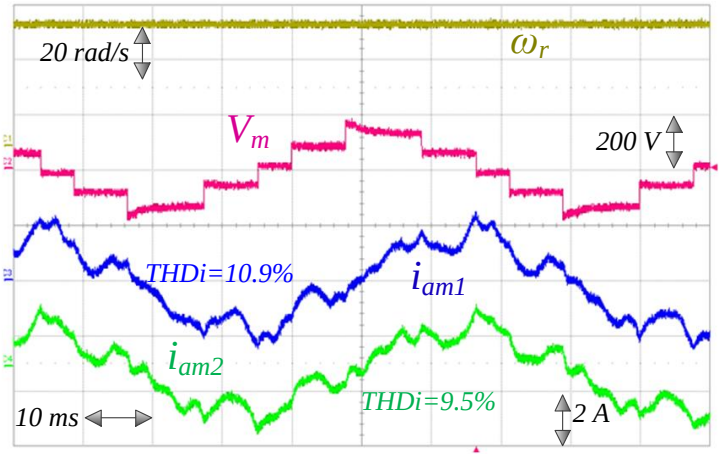

Fig. 5. 25 Steady state test: both motors are wye connected and fed by a step modulated 5LI.

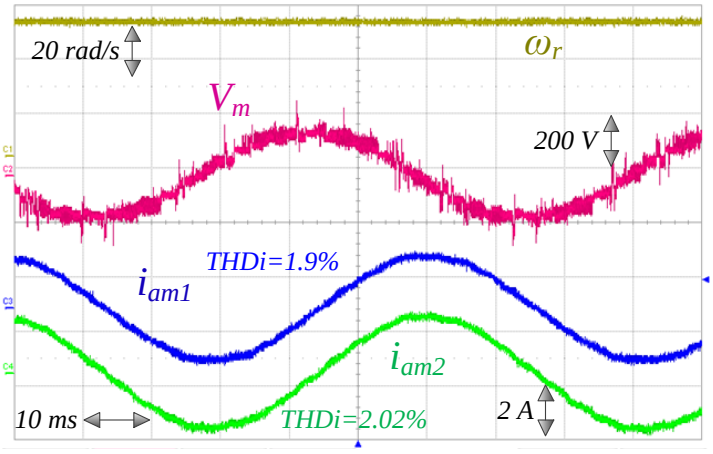

Fig. 5. 26 Steady state test with the proposed OW MMSC (5LI+TLI).

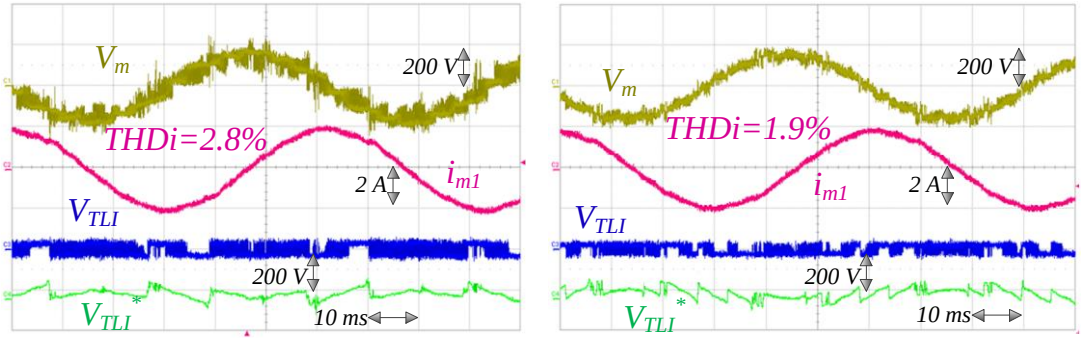

Fig. 5. 27 OW MMSC prototypes (3LI+TLI - left, 5LI+TLI - right): phase voltage V_{am}, phase current i_{am}, TLI reference V_{TLIa} and TLI output voltage V_{TLIa}.*

A speed reversal from -40 to 40rad/s is shown in Fig. 5. 28(left), performed on a MMSC drive featuring the 5LI+TLI configuration. Obtained results confirm the consistence of the field oriented control and the effectiveness of the floating capacitor voltage stabilization.

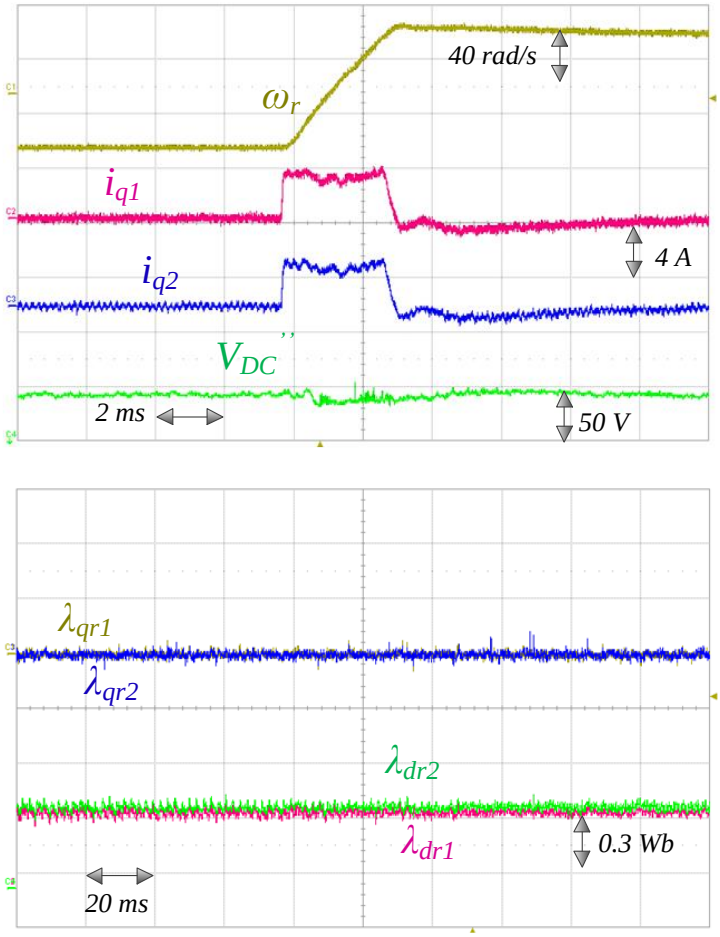

Fig. 5. 28 OW MMSC prototype 5LI+TLI: speed reversal between ω_r =-40rad/s and ω_r =40rad/s. id=2 A(up). Steady state at ω_r =50rad/s. id*=2 A, rotor fluxes of two motors(down).*

Total power losses of the OW MMSC configuration have been evaluated and compared with those of a more conventional system encompassing a 3-level inverter and two wye connected induction motors. The conventional system is operated either with a *10kHz* PWM, either with a step voltage modulation. Fig. 5. 29 deals with estimated total efficiency.

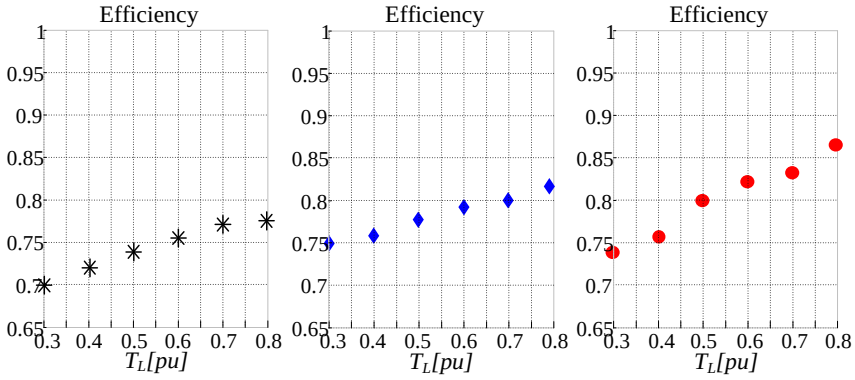

Fig. 5. 29 Total efficiency of the MMSC with: step operated 3LI (left), PWM operated 3LI (middle) and the proposed 3LI+TLI OW configuration (right).

It has been determined on the basis of computed motor (core and winding) and inverter (switching and on-state) power losses, by taking into consideration the harmonic content of stator currents and voltages up to the 90th harmonic. The proposed configuration scores a higher efficiency at medium and high loads, while at low loads it is comparable with that of the conventional system when it is PWM operated.

5.1.2 Open-end Winding Multi-Motor Multiple Converters

The AHMLI approach has also been exploited to carry out a Multi-Motor-Multi-Converters (MMMC) system. As shown in Fig. 5. 30, the three-phase TLI of the OW MMSC system is replaced by a Five-Leg Inverter (TLI5), which works as active filter and independently controls the stator current of the two motors [8], which are supplied on the other side by a single MLI.

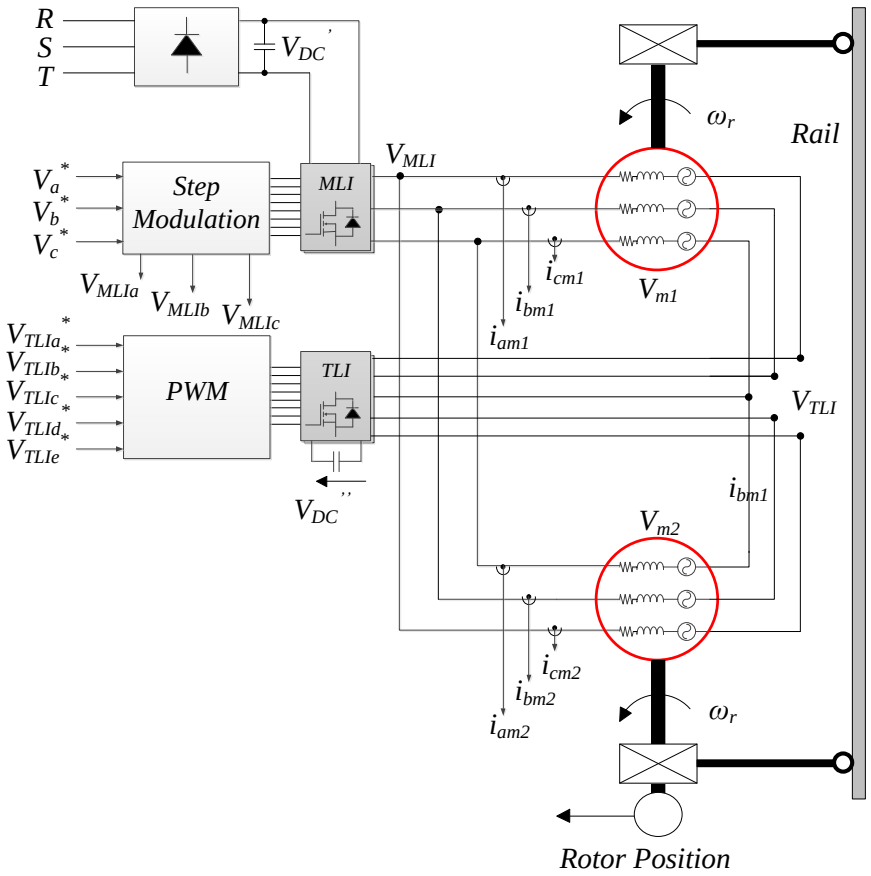

Fig. 5. 30 Proposed OW MMMC

This configuration enables a full control of the load sharing between two machines, which run at the same speed, as it is required by the large majority of cranes applications.

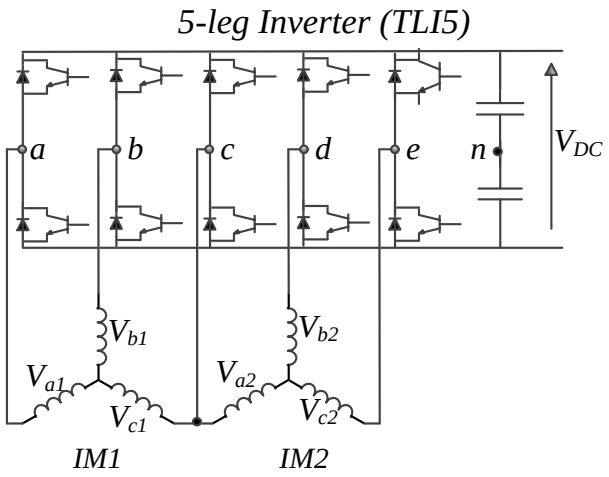

Fig. 5. 31 Conventional dual induction motors fed by five-leg inverter

A conventional system requires two different inverters, thus twelve power switches, to operate the two motors with an independent torque control. The five legs inverter, shown in Fig. 5. 31 is used instead, in order to reduce the amount of required power switches. Such a configuration uses a common leg to supply two phases belonging to different motors. In particular, in the scheme of Fig. 5. 31, the *C* legs acts as common leg.

The voltage vector applied to the two induction motors according to a stationary α, β reference frame is given by:

$$V_s = V_{s\alpha} + jV_{s\beta} = \sqrt{\frac{2}{5}}V_{DC}\left(V_a + V_b e^{\frac{j2\pi}{5}} + V_c e^{\frac{j4\pi}{5}} + V_d e^{\frac{j6\pi}{5}} + V_e e^{\frac{j8\pi}{5}}\right) \tag{5.9}$$

where V_a, V_b, V_c, V_d and V_e are the output inverter voltages.

A TLI5 may generate 2^5 (32) different voltage vectors, as depicted in Fig. 5. 32.

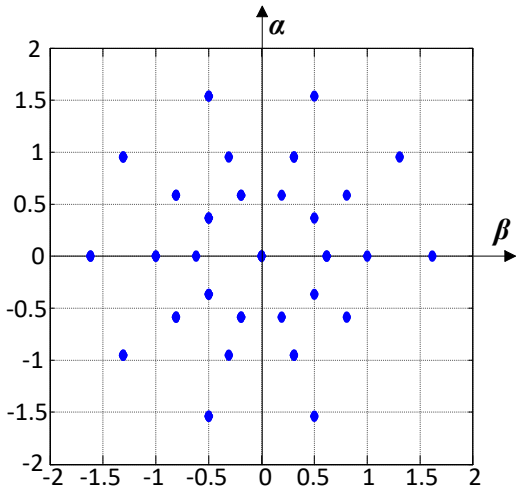

Fig. 5. 32 Space vector combinations of a conventional five-leg inverter

Two PWM strategies have been developed in [9]: PWM with cancellation of the voltage reference and PWM with addition of the voltage reference.

The first technique accomplishes the cancellation of the voltage reference of the common leg. The reference voltages of the two motors are:

$$\begin{aligned} V_a^* &= V_{a1}^* - V_{c1}^* \\ V_b^* &= V_{b1}^* - V_{c1}^* \\ Vc^* &= V_{c1}^* = V_{c2}^* = 0 \\ V_d^* &= V_{a2}^* - V_{c2}^* \\ V_e^* &= V_{b1}^* - V_{c2}^* \end{aligned} \tag{5.10}$$

The main drawback of this technique relies a reduction of the maximum reference voltage by a factor $1/\sqrt{3}$, if compared with the conventional two inverters systems [10].

The second technique is based on the addition of the phase voltage references of the two motors, thus the reference voltages are:

$$\begin{aligned} V_a^* &= V_{a1}^* + V_{c1}^* \\ V_b^* &= V_{b1}^* + V_{c1}^* \\ Vc^* &= V_{c1}^* + V_{c2}^* \\ V_d^* &= V_{a2}^* + V_{c1}^* \\ V_e^* &= V_{b1}^* + V_{c1}^* \end{aligned} \tag{5.11}$$

Fig. 5. 33 shows the output voltage control system, using the PWM strategy based on the addition of the voltage reference. As shown in Fig. 5. 30, V_{TLIa}^*, V_{TLIb}^*, V_{TLIc}^*, V_{TLId}^* and V_{TLIe}^* are the reference voltage of the TLI5 of the proposed OW MMMC system.

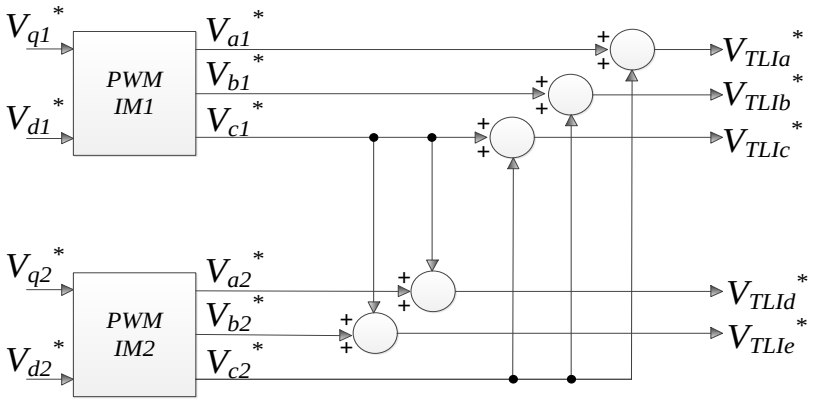

Fig. 5. 33 Output voltage control system for Pulse Width Modulation strategy based on the addition of the voltage reference

Fig. 5. 34 shows the equivalent circuit of the proposed OW MMMC system. V_{MLIa}, V_{MLIb} and V_{MLIc} are the MLI staircase output phase voltages while V_{TLIa}, V_{TLIb} $V_{TLIc,}$ V_{TLId} and V_{TLIe} are the TLI5 output phase voltages. The *c*-phase windings of the two motors are connected in parallel and supplied by the phase voltages V_{MLIc} and V_{TLIc}. By applying the Kirchhoff's current law at node n'' the following expressions are obtained:

$$\begin{aligned} &i_{am1}+i_{bm1}+i_{cm}+i_{am2}+i_{bm2}=0 \\ &i_{am}=i_{am1} \\ &i_{bm}=i_{bm1} \\ &i_{cm}=i_{cm1}=i_{cm2} \\ &i_{dm}=i_{bm2} \\ &i_{em}=i_{am2} \end{aligned} \tag{5.12}$$

where:

$$\begin{aligned} &i_{am1}+i_{bm1}+i_{cm1}=0 \\ &i_{am2}+i_{bm2}+i_{cm2}=0 \end{aligned} \tag{5.13}$$

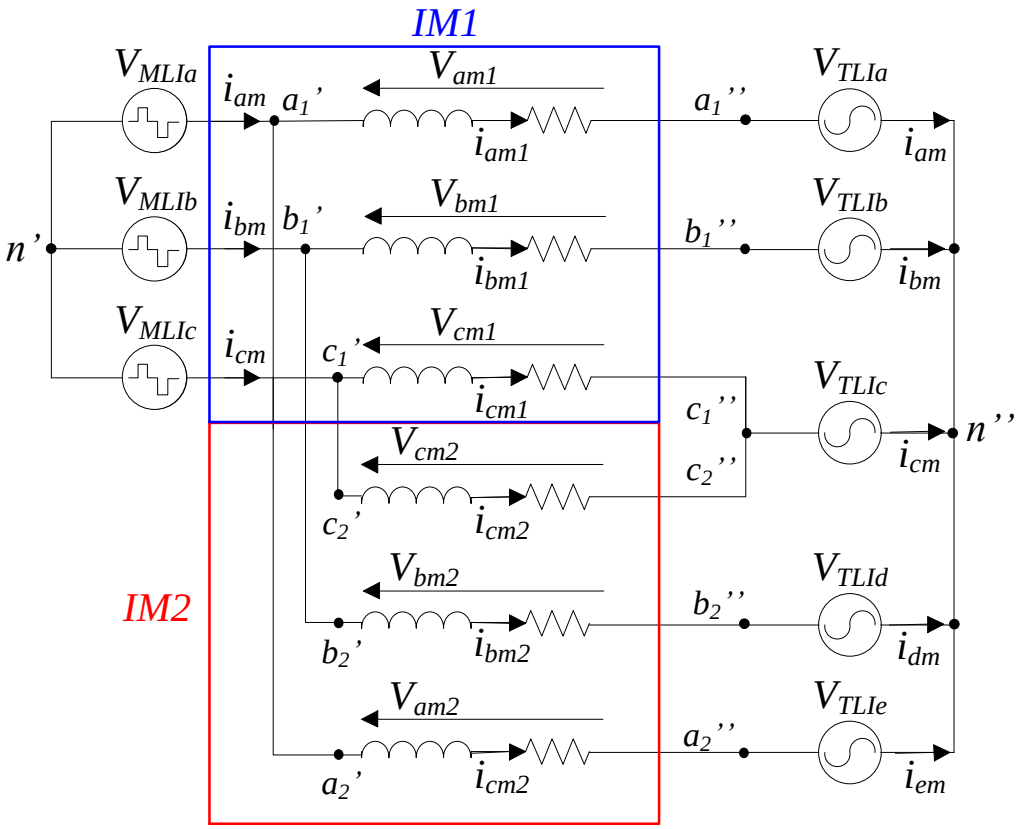

Fig. 5. 34 Equivalent circuit of the proposed OW MMMC

According the AHMLI approach, in order to compensate the undesired low order harmonic components generated by MLI step modulated, TLI reference voltages must be set to:

$$
\begin{aligned}
V_{TLIa}{}^{*} &= V_{MLIa} - V_{am} \\
V_{TLIb}{}^{*} &= V_{MLIb} - V_{bm} \\
V_{TLIc}{}^{*} &= V_{MLIc} - V_{cm} \\
V_{TLId}{}^{*} &= V_{MLIb} - V_{bm} \\
V_{TLIe}{}^{*} &= V_{MLIa} - V_{am}
\end{aligned}
\tag{5.14}
$$

being V_{am}, V_{bm} $V_{cm,}$ the fundamental components of the reference motor voltages, as shown in Fig. 5. 30. The output current control system is schematized in Fig. 5. 35.

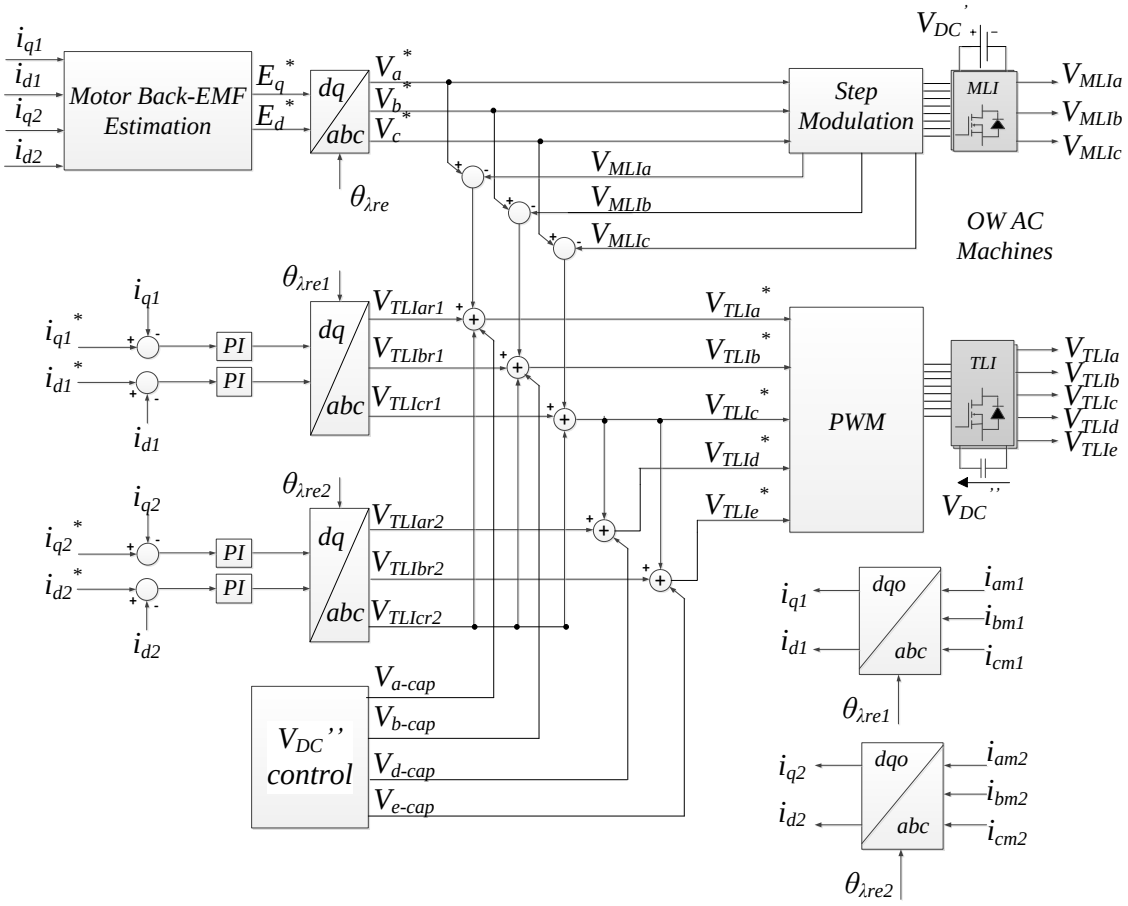

Fig. 5. 35 OW MMMC configuration current control system.

Assuming the two machines identical and running at the same speed, the q,d axes back EMF voltage references $E_q{}^{*}$ and $E_d{}^{*}$ are estimated as:

$$
\begin{aligned}
E_q{}^{*} &= \omega_{\lambda r} L_s i_d{}^{*} \\
E_d{}^{*} &= -L_K \omega_{\lambda r} i_q{}^{*} \\
\omega_{\lambda r} &= \frac{Rr}{Lr}\frac{iq^{*}}{id^{*}} + \omega_r
\end{aligned}
\tag{5.15}
$$

and:

$$L_K = \left(\frac{L_r L_S - L_m^2}{L_r}\right) \tag{5.16}$$

being $\omega_{\lambda r}$ and ω_r respectively the rotor flux angular speed and the rotor speed of the two machines, while L_s, L_r and L_m are respectively the stator, rotor and magnetizing inductance. According to the voltage control system of Fig. 5. 33, the reference voltages of the TLI5 are:

$$\begin{aligned}
V_{TLIa}^{*} &= V_{TLIar1} + (V_{MLIa} - V_a^{*}) + V_{a-cap} \\
V_{TLIb}^{*} &= V_{TLIbr1} + (V_{MLIb} - V_b^{*}) + V_{b-cap} \\
V_{TLIc}^{*} &= V_{TLIcr1} + V_{TLIcr2} + (V_{MLIc} - V_c^{*}) \\
V_{TLId}^{*} &= V_{TLIar2} + V_{TLIcr1} + V_{d-cap} \\
V_{TLIe}^{*} &= V_{TLIbr2} + V_{TLIcr1} + V_{e-cap}
\end{aligned} \tag{5.17}$$

being $V_{abde\text{-}c}$ additional terms to control the TLI DC-Bus voltage, $V_{TLIabc1}$ the output of the IM1 current controller $V_{TLIabc2}$ the output of the IM2 current controller.

The qd-axes reference currents are set to:

$$\begin{aligned}
i_{d1}^{*} &= i_{d2}^{*} = i_d^{*} \\
i_q^{*} &= \frac{1}{2}(i_{q1}^{*} + i_{q2}^{*})
\end{aligned} \tag{5.18}$$

In these conditions, the back-EMF voltages of the two motors are the same in amplitude, frequency and phase. They are synthetized by the MLI using a low switching frequency modulation. Low order voltage harmonic components generated by MLI low switching frequency modulation are compensated on both motors by the TLI5. If the two motors operate at a different speed $\omega_{r1} \neq \omega_{r2}$, back-EMF voltages of the two motor do not feature the same values of amplitude, frequency and phase. In this case a full compensation can be obtained on only one of the two motors. The effectiveness of the harmonic compensation depends in this case by the difference between the speeds of the two motors. Steady state simulation tests have been carried out operating the two motors at different speeds. Fig. 5. 36 shows the phase voltages of IM1 running at 157 rad/s and the phase voltages of IM2 operating at 125 rad/s. Since the harmonic compensation terms used are those of IM1, the stator current harmonic content of IM1 is better than that of IM2, as shown in Fig. 5. 37 and Fig. 5. 38. Moreover, the electromagnetic torque T_{e2} of IM2 is affected by a ripple, Fig. 5. 39.

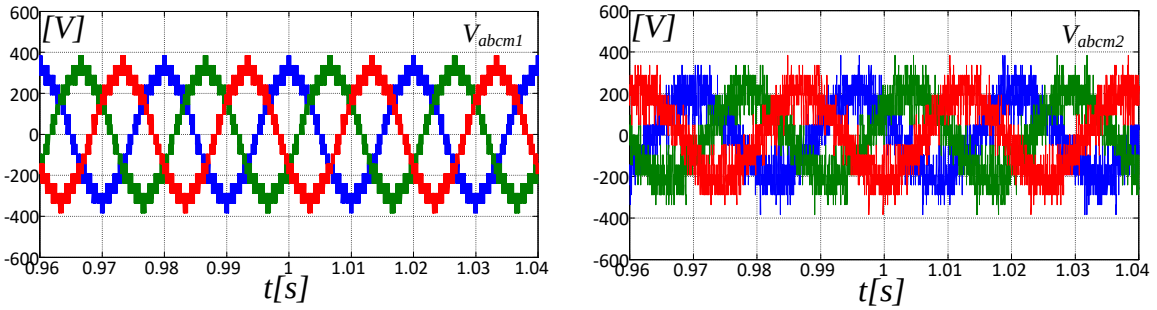

Fig. 5. 36 OW MMMC: Phase voltage of IM1 at 157 rad/s(left). Phase voltages of IM2 at 125 rad/s

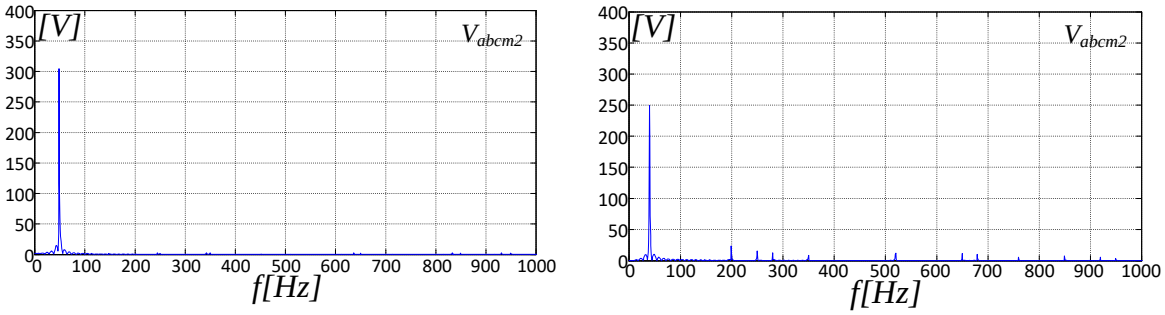

Fig. 5. 37 OW MMMC: Spectrum of Phase voltage of IM1 at 157 rad/s(left). Spectrum of Phase voltages of IM2 at 125 rad/s

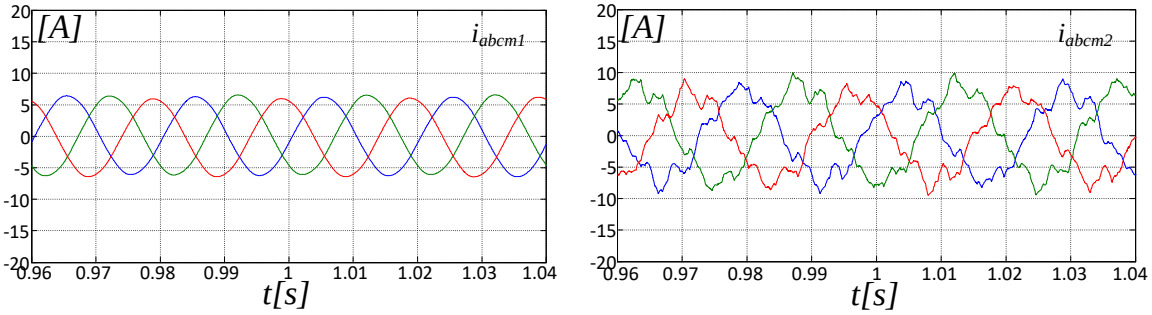

Fig. 5. 38 OW MMMC: Phase currents of IM1 at 157 rad/s(left). Phase currents of IM2 at 125 rad/s

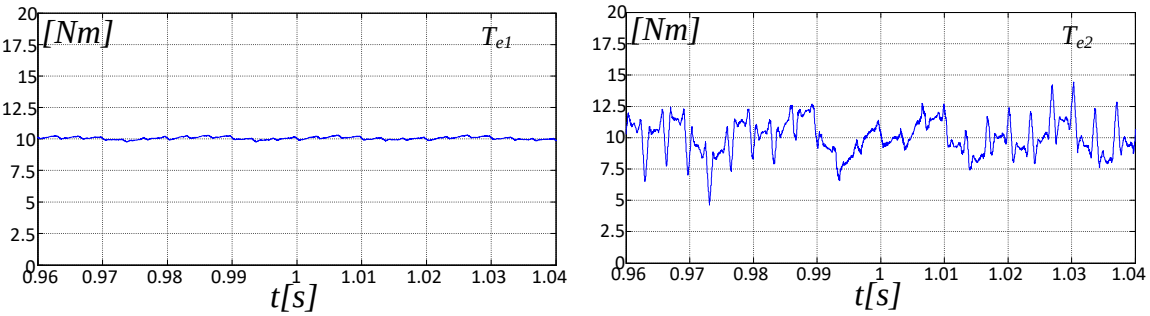

Fig. 5. 39 OW MMMC: Torque ripple of IM1 at 157 rad/s(left). Torque ripple of IM2 at 125 rad/s

A speed reversal simulation between -40 and 40rad/s is shown in Fig. 5. 40(left). Assuming a rigid mechanical coupling, both even and uneven load torque sharing have been considered. Fig. 5. 40(right) shows the phase

currents of the TLI5. The *c*-phase current is higher than the others, because it is the composition of the c-phase currents of the two machines. The dynamic response of the system with an even load current sharing is shown in Fig. 5. 41. Stator currents are shown in Fig. 5. 42, confirming the effectiveness of the active current shaping.

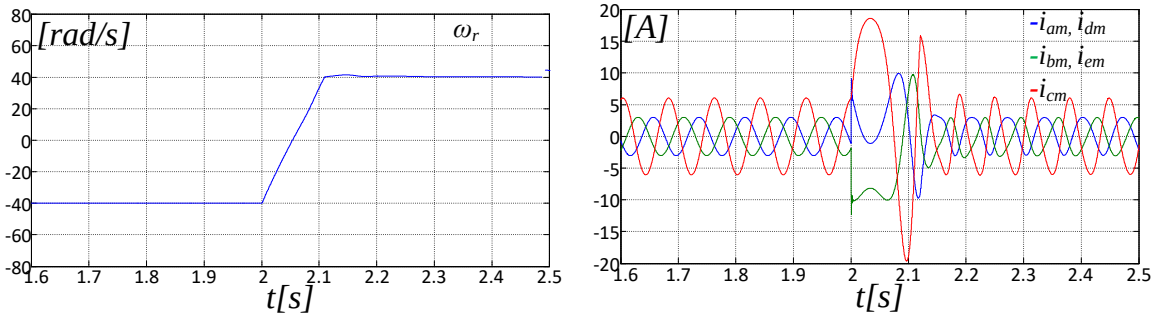

Fig. 5. 40 OW MMMC speed reversal simulation test between ωr =-40rad/s and ωr =40rad/s: Mechanical speed(left). TLI5phase currents(right)

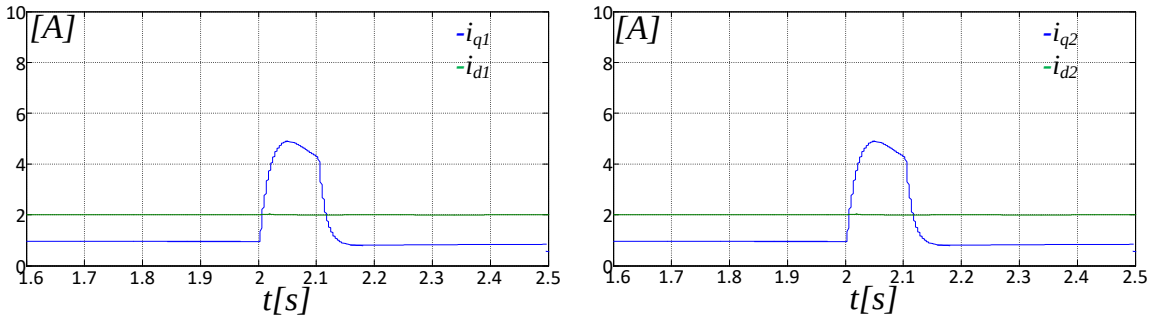

Fig. 5. 41 OW MMMC speed reversal simulation test between ωr =-40rad/s and ωr =40rad/s with uniform distribution of the load torque: qd-axes currents of IM1, iq1= 1A, id1=2A(left). qd-axes currents of IM2, iq2= 1A, id2=2A (right)

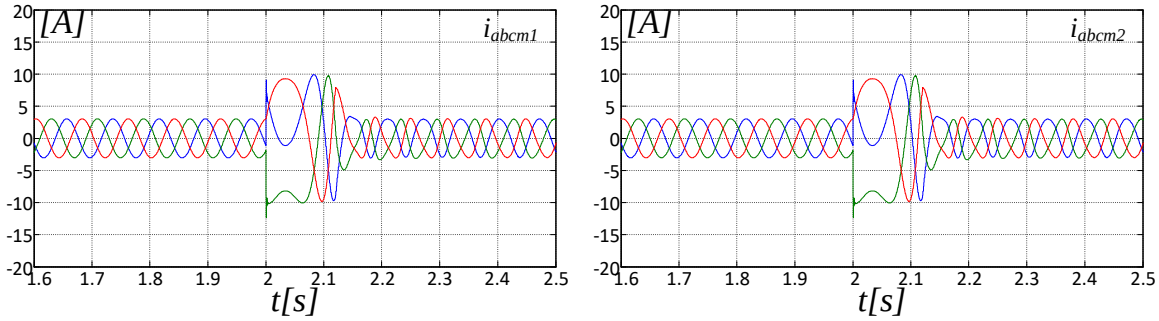

Fig. 5. 42 OW MMMC speed reversal simulation test between ωr =-40rad/s and ωr =40rad/s with uniform distribution of the load torque: phase currents of IM1, iq1= 1A, id1=2A(left). phase currents of IM2, iq2= 1A, id2=2A (right)

The consistence of the independent control of the two motors is shown in Fig. 5. 43 and Fig. 5. 44, dealing with a uneven load torque sharing between the two motors running at the same speed.

An experimental test where an even sharing of the load torque is established between the two motors is shown Fig. 5. 45. An uneven load sharing is instead considered in the test of Fig. 5. 46, where a 70% of the required torque is produced by IM1 and only a 30% by IM2. Phase currents of the two motors feature in the last case

different amplitudes and THD levels, as shown in Fig. 5. 47. Estimated motor back-EMF E_1 and E_2, as well the average back EMF E^*, computed according to eq. (5.15) are shown in Fig. 5. 48. Both steady state and dynamical torque and speed responses are quite satisfactory.

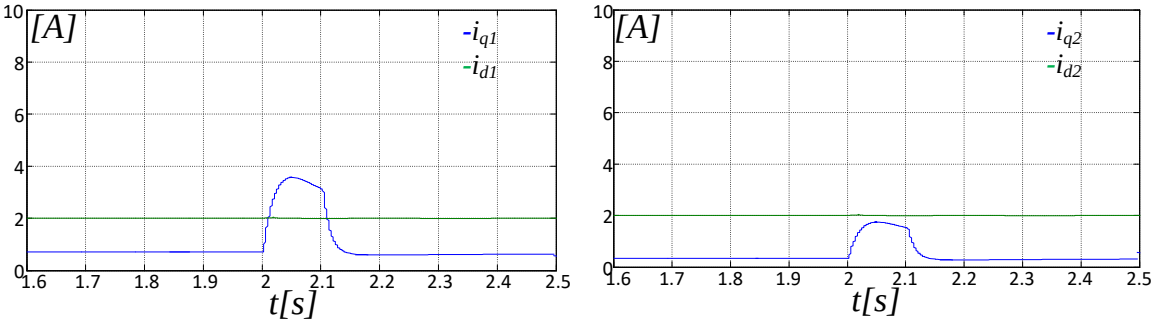

Fig. 5. 43 OW MMMC speed reversal simulation test between ωr =-40rad/s and ωr =40rad/s with non-uniform distribution of the load torque: qd-axes currents of IM1, iq1= 0.7A, id1=2A(left). qd-axes currents of IM2, iq2= 0.3A, id2=2A (right)

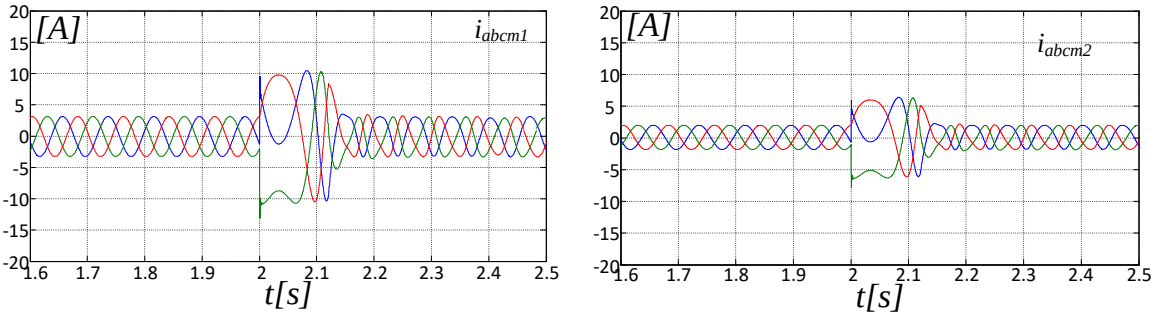

Fig. 5. 44 OW MMMC speed reversal simulation test between ωr =-40rad/s and ωr =40rad/s with uniform distribution of the load torque: phase currents of IM1, iq1= 0.7A, id1=2A(left). phase currents of IM2, iq2= 0.3A, id2=2A (right)

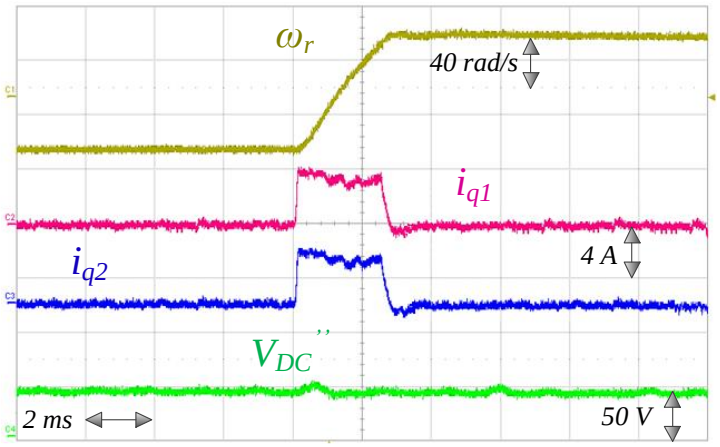

Fig. 5. 45 OW MMMC prototype 5LI+TLI5: speed reversal between ω_r =-40rad/s and ω_r =40rad/s. iq1=iq2=iq, id*=2 A*

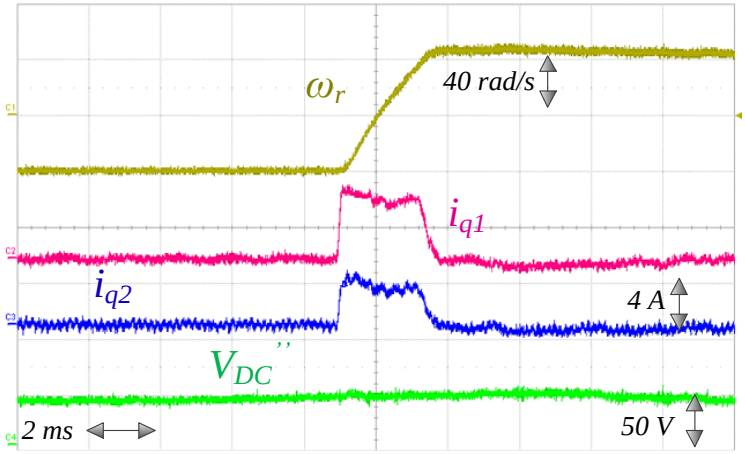

Fig. 5. 46 OW MMMC prototype 5LI+TLI5: speed reversal between ω_r =-40rad/s and ω_r =40rad/s. iq1=0.7iq, iq2=0.3iq*,id*=2A*

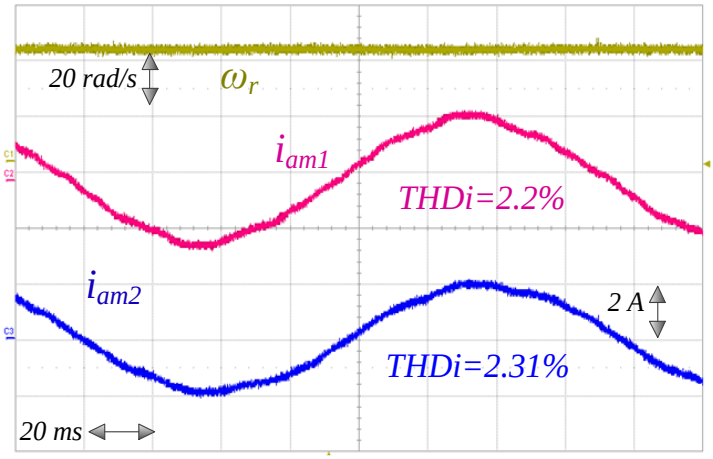

Fig. 5. 47 OW MMMC prototype 5LI+TLI5: speed reversal between ω_r =-40rad/s and ω_r =40rad/s. iq1=0.7iq, iq2=0.3iq*,id*=2A, phase currents*

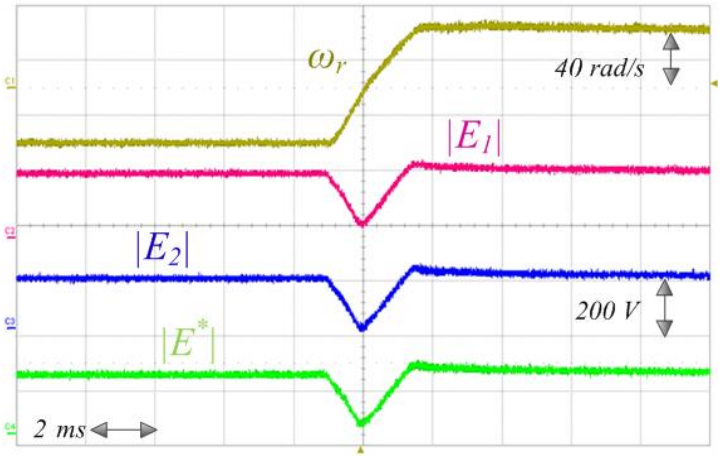

Fig. 5. 48 OW MMMC prototype 5LI+TLI5: speed reversal between ω_r =-40rad/s and ω_r =40rad/s. iq1=0.7iq, iq2=0.3iq*, id*=2 A, estimated Back-EMF*

5.2 References of Chapter 5

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6 Conclusions and recommended future work

The work has been focused on the study and development of a new multilevel converter topology, called Asymmetrical Hybrid Multilevel Inverter (AHMLI) and on the assessment of possible advantages coming from the exploitation of such a topology in different application fields. The developed topology is tailored around an electrical machine adopting an open end winding configuration. According to such an approach the stator,

or primary, winding of an electrical machine (motor, generator or transformer) is supplied on one end by a main multilevel converter, fully managing the active power stream, and, on the other end by a conventional two level inverter. The last acts as an active power filter, providing reactive power to the electrical machine and suitably shaping the phase currents. The AHMLI approach has been advantageously exploited either on electric motor drives, either on fully stationary systems, and even to realize a high efficiency rectifier for high speed generation systems. Remarkable improvements are achieved in all the considered cases over more conventional solutions in terms of power losses and power quality. Specifically, power losses reduction is obtained by adopting an original design strategy. The main multilevel inverter is, in fact, very efficiently operated at medium voltage with a low switching frequency and equipped with low on-state losses devices. The auxiliary two level inverter is, instead, operated at a remarkably lower voltage with a high frequency PWM technique and is equipped with low switching losses devices. In terms of phase voltage levels an AHMLI is equivalent to a PWM operated multilevel inverter with a larger number of power devices, but it is more efficient, thus reducing the cost and size. The consistency of the proposed topology in different fields of application has been exhaustively evaluated by simulation and experimental tests.

Obtained results can constitute the starting point for further investigations about the Asymmetrical Hybrid multilevel inverter structure. Specifically, overvoltage mitigation in industrial motor drives, high efficiency rectifiers and grid inverters for PV plants are fields of great potential.