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An Averaged-Value Model of an Asymmetrical Hybrid Multi-Level Rectifier

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Abstract: The development and the validation of an averaged-value mathematical model of an asymmetrical hybrid multi-level rectifier is presented in this work. Such a rectifier is composed of a three-level T-type unidirectional rectifier and of a two-level inverter connected to an open-end winding electrical machine. The T-type rectifier, which supplies the load, operates at quite a low switching frequency in order to minimize inverter power losses. The two-level inverter is instead driven by a standard sinusoidal pulse width modulation (SPWM) technique to suitably shape the input current. The two-level inverter also plays a key role in actively balancing the voltage across the DC bus capacitors of the T-type rectifier, making unnecessary additional circuits. Such an asymmetrical structure achieves a higher efficiency compared to conventional PWM multilevel rectifiers, even considering extra power losses due to the auxiliary inverter. In spite of its advantageous features, the asymmetrical hybrid multi-level rectifier topology is a quite complex system, which requires suitable mathematical tools for control and optimization purposes. This paper intends to be a step in this direction by deriving an averaged-value mathematical model of the whole system, which is validated through comparison with other modeling approaches and experimental results. The paper is mainly focused on applications in the field of electrical power generation; however, the converter structure can be also exploited in a variety of grid-connected applications by replacing the generator with a transformer featuring an open-end secondary winding arrangement.

Keywords: electrical drives; energy saving; multilevel power converters; permanent magnet synchronous generator; open-end winding configuration; voltage balancing; power factor

1. Introduction

Multi-level converters have proved in the last decades to be a viable alternative to conventional topologies in medium-voltage, high-power, industrial applications, but today, their field of applications is rapidly spreading toward low-power and low-voltage ranges. Main advantages of multi-level converters are basically those of an improved harmonic content of AC voltages and currents and of a reduction of power switch voltage ratings [1,2], the main drawback being a greater complexity. Open-winding (OW) configurations, consisting of an AC machine fed by two power converters [3–6], can be deemed as a special kind of multi-level converter [7]. Different configurations, control schemes, and modulation techniques dealing with OW systems have been discussed in the literature [8–10]. Some OW configurations embedding multi-level converters have also been recently developed [11–13]. Among them, a high efficiency asymmetrical hybrid multilevel inverter for motor drives has been presented and analyzed in [12] featuring a particular asymmetrical structure where two different kinds of converters are connected at the two sides of an OW AC machine with different functions. Specifically, a main multilevel converter supplies the load, and an auxiliary two-level inverter acts as

an active power filter. Such an approach has also been used in [13] to realize an asymmetrical hybrid unidirectional T-type rectifier (AHUTR) for gen-set applications, tailored around an open-end winding permanent magnet synchronous generator (PMSG), as shown in Figure 1. According to the AHUTR topology, the open-end winding PMSG on one side supplies the electrical load through the main converter, a T-type rectifier (TTR), also commonly known as a Vienna rectifier, and on the other side, it is connected to an auxiliary two-level inverter (TLI). The main converter processes the whole power delivered to the load, and thus, it is operated at the fundamental frequency in order to minimize the switching power losses. The TLI is instead driven by a high switching frequency PWM technique to suitably shape the phase currents. Therefore, a stable output DC voltage and almost sinusoidal input currents are obtained, achieving a higher efficiency than comparable conventional PWM rectifiers [12]. The AHUTR structure is also of general applicability, being exploitable in grid-connected applications by replacing the generator with a transformer featuring an open-end secondary winding, as shown in Figure 1, but it is more complex than conventional rectifiers, requiring suitable mathematical tools for control and optimization purposes. The aim of this work is thus to provide an essential tool for the design of the control system of an AHUTR by developing an averaged-value model (AVM) of the system. In general, averaged-value techniques approximate the model of a switching converter to a continuous system by considering the values taken by the variables along a switching period as constant. They are useful when designing and testing control algorithms, as well as to develop efficiency optimization techniques, because a high frequency dynamic analysis is not required, differently than power circuits and filters design. Specifically, an AHUTR AVM has been developed with the aim to support the design of effective solutions to maximize system efficiency, to provide a stable DC output voltage, to cancel low-order undesired harmonics from the phase currents, to equalize the Vienna rectifier DC bus capacitor voltages, and to control the TLI DC bus voltage. Furthermore, the developed model is valuable in tuning voltage and current regulators.

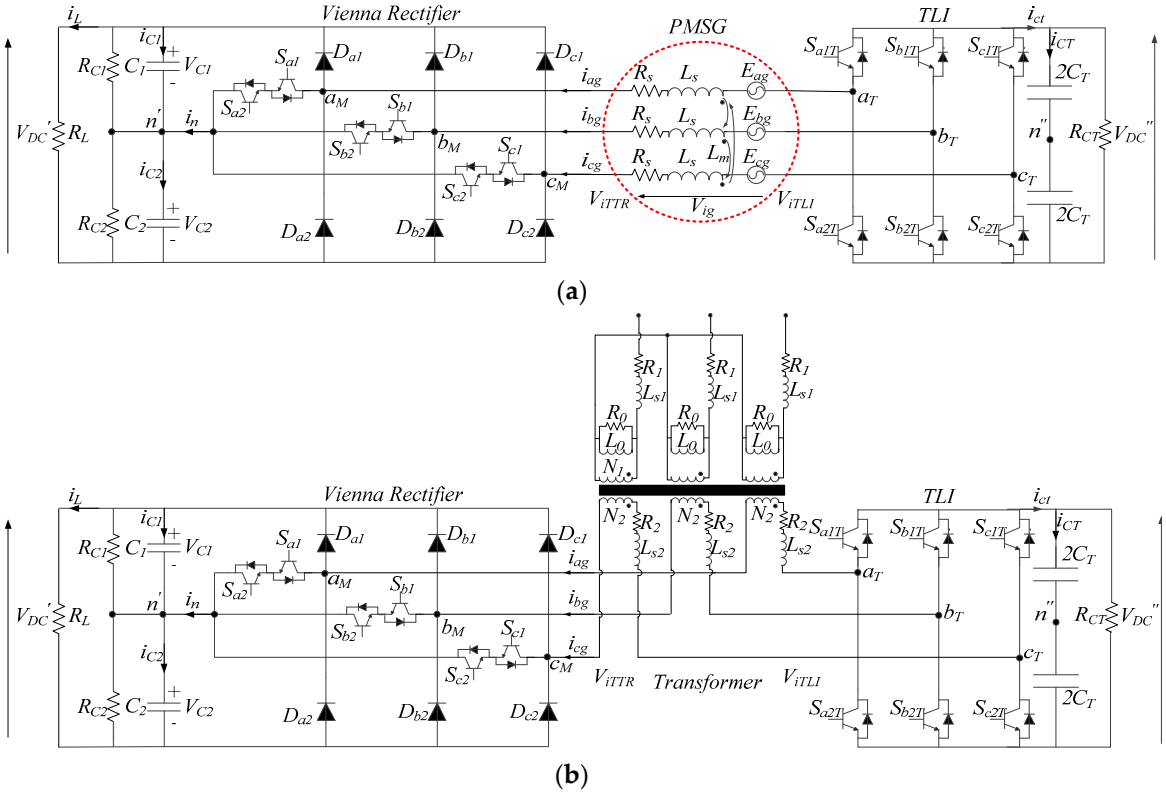


Figure 1. AHUTR for electrical power generation (**a**) and grid-connected (**b**) applications.

2. Asymmetrical Hybrid Unidirectional T-Type Rectifier

According to Figure 1, an AHUTR supplies the load through a Vienna rectifier switching at fundamental frequency. In electricity generation applications, this rectifier is connected to one end of an open winding electrical generator, very often a PMSG. For grid-connected applications, the electrical generator is replaced by a transformer with an open-end secondary winding. While remarkably reducing the switching power losses, low switching frequency operations would, however, produce highly distorted phase currents. This is prevented by an active power filter based on a conventional TLI, which is connected to the other end of the electrical machine winding. Such an inverter features a lower DC bus voltage compared to the Vienna rectifier and exploits a floating capacitor to reduce the complexity of the system and to prevent the occurrence of zero sequence currents [11–13]. The efficiency of the Vienna rectifier can be increased by using low on-state voltage drop power devices, thus optimizing the design of this converter for low conduction power losses. On the other hand, the design of the TLI can be optimized for high switching frequency operation, by using fast power devices with lower voltage ratings. A key feature of the AHUTR topology is that the voltages of the two Vienna rectifier DC bus capacitors can be independently regulated through the TLI, thus making unnecessary additional power converters or special PWM strategies.

In the AHUTR topology, three bidirectional switches S_{ij}, (i = a, b, c and j = 1, 2) are connected between the midpoint n' of the Vienna rectifier and the rectifier poles [14]. The generic i-phase voltage V_{iTTR} between the rectifier input terminal i_M and the mid-point n'' of the Vienna rectifier DC bus is given by

$$V_{iTTR} = \frac{l_i' - 1}{2} V_{DC}', \; l_i' = 0, 1, 2 \tag{1}$$

where V_{DC}' is the DC bus voltage. Hence, three different levels can be taken by the Vienna rectifier input voltage, namely: $-V_{DC}'/2$, $V_{DC}'/2$, and 0, according to the rectifier i-pole state l_i'.

On the TLI side, the voltage between the TLI i-phase output terminal i_T and the mid-point n' of the TLI DC bus is given by:

$$V_{iTLI} = \frac{2l_i'' - 1}{2} V_{DC}'', \; l_i'' = 0, 1 \tag{2}$$

providing two voltage levels, namely, $-V_{DC}''/2$ and $V_{DC}''/2$, according to the inverter i-pole state l_i''.

The voltage across a phase winding is given by

$$V_{ig} = V_{iTTR} - V_{iTLI} - V_{n'n''} = \frac{l_i'' - 1}{2} V_{DC}' - \frac{2l_i'' - 1}{2} V_{DC}'' - V_{n'n''} \tag{3}$$

where V_{DC}' and V_{DC}'' are the DC bus voltages of the Vienna rectifier and the TLI, respectively, and $V_{n'n''}$ is the voltage between the mid points n' and n'' of the two DC buses, which can be expressed as

$$V_{n'n''} = \frac{1}{3}(V_{aTTR} + V_{bTTR} + V_{cTTR}) - \frac{1}{3}(V_{aTLI} + V_{bTLI} + V_{cTLI}). \tag{4}$$

According to (2) and (3), the OW structure of Figure 1, featuring twelve power switches, is equivalent to a six-level neutral point clamped (NPC) or flying capacitor (FC) converter, which would, however, encompass thirty power switches [12]. As shown in Figure 2, the AHUTR requires a complex control system to suitably coordinate the operations of the two converters in order to regulate the DC output voltage, to cancel low-order harmonics from phase currents, to equalize the Vienna rectifier DC bus capacitor voltages, and to control the TLI DC bus voltage [14,15].

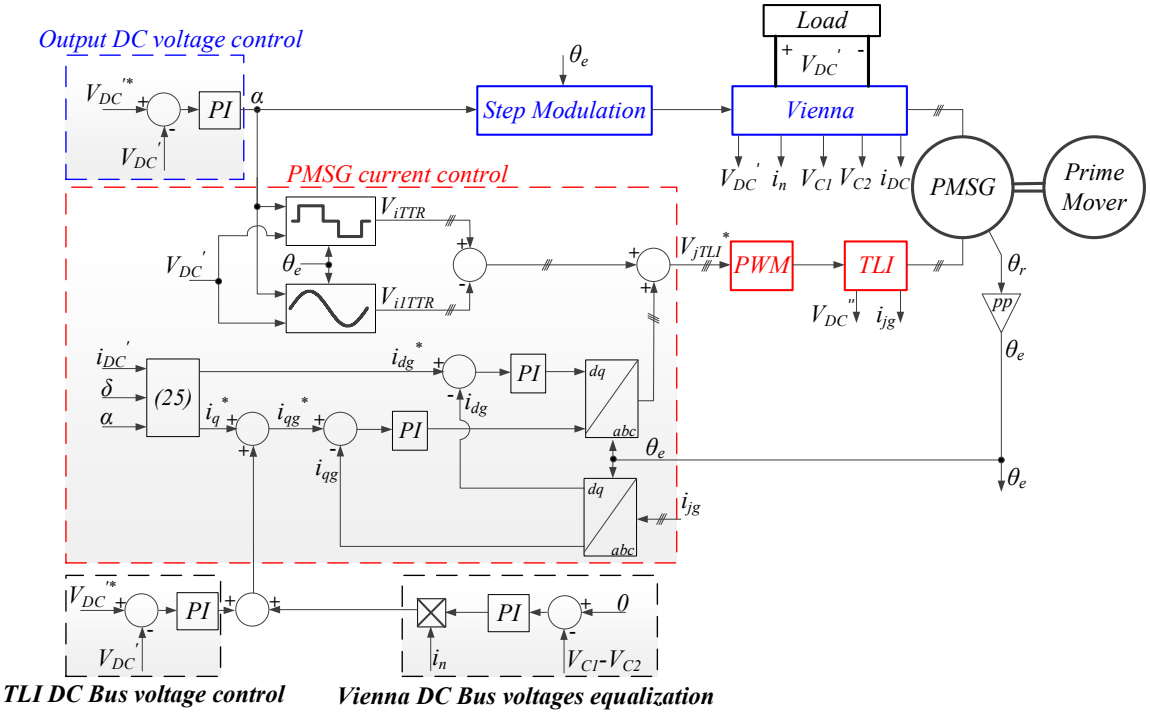


Figure 2. Block diagram of the control system of the AHUTR for electrical power generation applications.

3. Averaged-value Model of the System

The averaged-value mathematical model of the system includes three sub-models: of the electrical machine, of the Vienna rectifier, and of the TLI.

3.1. Open-Winding PMSG Model

It is assumed that the stator windings produce sinusoidal magnetomotive forces; moreover, effects of the saturation of the magnetic core are neglected. Under these assumptions, the surface-mounted PMSG model in an orthogonal *qd* reference frame synchronous to the rotor flux is given by the following sets of Equations:

$$\begin{aligned} V_{qs} &= R_s i_{qs} + \tfrac{d}{dt}\lambda_{qs} + \omega_{re}\lambda_{ds} \\ V_{ds} &= R_s i_{ds} + \tfrac{d}{dt}\lambda_{ds} - \omega_{re}\lambda_{qs} \end{aligned} \tag{5}$$

$$\begin{aligned} \lambda_{qs} &= L_s i_{qs} \\ \lambda_{ds} &= L_s i_{ds} + \lambda_{pm} \end{aligned} \tag{6}$$

$$\begin{aligned} T_e &= \tfrac{3}{2} pp(\lambda_{ds} i_{qs} - \lambda_{qs} i_{ds}) \\ T_e - T_L &= J\tfrac{d}{dt}\omega_r + F\omega_r \end{aligned} \tag{7}$$

where i_{qs}, i_{ds}, V_{qs}, V_{ds}, λ_{qs}, and λ_{ds} are the components of stator current, voltage, and flux in the *qd* axis; L_s is the stator inductance; λ_{pm} is the linkage flux of permanent magnets; T_e is the electromagnetic torque; J is the total mechanical inertia; F is the rotor friction; $\omega_{re} = pp\omega_r$ is the rotor speed; and pp is the amount of pole pairs. The rotational terms $\omega_{re}\lambda_{ds}$ and $\omega_{re}\lambda_{qs}$ account for the *qd* axis back-emf E_q and E_d, respectively.

The averaged-value PMSG phase voltage V_{ig} is obtained as the difference between the fundamental harmonic $\overline{V}_{iTTR}$ of the Vienna rectifier input voltage and the fundamental harmonic $\overline{V}_{iTLI}$ of the TLI output voltage. The voltage $V_{n'n''}$ between the mid points of the two DC buses can be neglected for averaged-value analysis, since it only includes high frequency harmonics [13].

PMSG phase voltages can be expressed in a *qd* synchronous reference frame to the back-EMF vector as a function of *qd* components of voltages $\overline{V}_{iTTR}$ and $\overline{V}_{iTLI}$ by:

$$\begin{vmatrix} \overline{V}_{qTTR} \\ \overline{V}_{dTTR} \end{vmatrix} = \frac{2}{3} \begin{vmatrix} \cos(\omega_{re}t) & \cos(\omega_{re}t - \frac{2}{3}\pi) & \cos(\omega_{re}t + \frac{2}{3}\pi) \\ \sin(\omega_{re}t) & \sin(\omega_{re}t - \frac{2}{3}\pi) & \sin(\omega_{re}t + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{vmatrix} \begin{vmatrix} \overline{V}_{aTTR} \\ \overline{V}_{bTTR} \\ \overline{V}_{cTTR} \end{vmatrix} \tag{8}$$

$$\begin{vmatrix} \overline{V}_{qTLI} \\ \overline{V}_{dTLI} \end{vmatrix} = \frac{2}{3} \times \begin{vmatrix} \cos(\omega_{re}t) & \cos(\omega_{re}t - \frac{2}{3}\pi) & \cos(\omega_{re}t + \frac{2}{3}\pi) \\ \sin(\omega_{re}t) & \sin(\omega_{re}t - \frac{2}{3}\pi) & \sin(\omega_{re}t + \frac{2}{3}\pi) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{vmatrix} \times \begin{vmatrix} \overline{V}_{aTLI} \\ \overline{V}_{bTLI} \\ \overline{V}_{cTLI} \end{vmatrix} \tag{9}$$

$$\overline{V}_{qg} = \overline{V}_{qTTR} - \overline{V}_{qTLI},\ \overline{V}_{dg} = \overline{V}_{dTTR} - \overline{V}_{dTLI} \tag{10}$$

A block scheme of the PMSG model is shown in Figure 3.

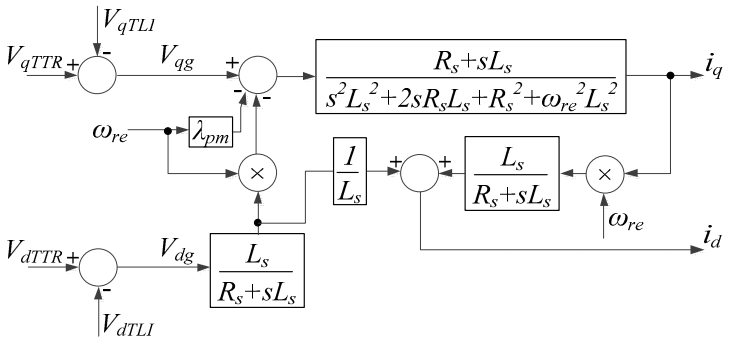


Figure 3. Block scheme of the permanent magnet synchronous generator (PMSG) model.

Similarly, a three-phase open secondary winding transformer (OSWT) can be modeled in an orthogonal *qd* reference frame synchronous to the primary voltage vector according to:

$$\begin{aligned} V_{q1} &= R_1 i_{q1} + \tfrac{d}{dt}\lambda_{q1} + \omega_e \lambda_{d1} \\ V_{d1} &= R_1 i_{d1} + \tfrac{d}{dt}\lambda_{d1} - \omega_e \lambda_{q1} \\ V_{q2} &= R_2 i_{q2} + \tfrac{d}{dt}\lambda_{q2} + \omega_e \lambda_{d2} \\ V_{d2} &= R_2 i_{d2} + \tfrac{d}{dt}\lambda_{d2} - \omega_e \lambda_{q2} \end{aligned} \tag{11}$$

$$\begin{aligned} \lambda_{q1} &= L_{s1} i_{q1} + L_m i_{q2} \\ \lambda_{d1} &= L_{s1} i_{d1} + L_m i_{d2} \\ \lambda_{q2} &= L_{s2} i_{q2} + L_m i_{q1} \\ \lambda_{d2} &= L_{s2} i_{d2} + L_m i_{d1} \\ L_{s1} &= L_{l1} + L_m \\ L_{s2} &= L_{l2} + L_m \end{aligned} \tag{12}$$

where i_{q1}, i_{d1}, i_{q2}, and i_{d2} are the q- and d-axis components of the primary and secondary winding currents, while V_{q1}, V_{d1}, V_{q2}, V_{d2} and λ_{q1}, λ_{d1}, λ_{q2}, λ_{d2}, are the q- and d-axis components of the primary and secondary winding voltages and fluxes. L_{s1} and L_{s2} are the self-inductances and L_m is the magnetization inductance. The angular frequency of the grid voltage is indicated as ω_e. The secondary windings are connected to the TTR and TLI, and thus, the phase winding voltages are given by:

$$\overline{V}_{q2} = \overline{V}_{qTTR} - \overline{V}_{qTLI},\quad \overline{V}_{d2} = \overline{V}_{dTTR} - \overline{V}_{dTLI} \tag{13}$$

3.2. Vienna Rectifier Model

The Vienna rectifier switches at the fundamental frequency, according to Table 1, where θ_e is the angular displacement of the fundamental harmonic of the winding phase voltage and α is the switching angle of S_{ij}, ($i = a, b, c$ and $j = 1, 2$).

Table 1. Vienna rectifier switching table.

Phase *a*	$0 < \theta_e < \alpha$ $\pi - \alpha < \theta_e < \pi + \alpha$ $2\pi - \alpha < \theta_e < 2\pi$	if $i_{ag} > 0$ => S_{a1} ON S_{a2} OFF if $i_{ag} < 0$ => S_{a1} OFF S_{a2} ON
Phase *b*	$2/3\pi < \theta_e < \alpha + 2/3\pi$ $5/3\pi - \alpha < \theta_e < 5/3\pi + \alpha$ $2/3\pi - \alpha < \theta_e < 2/3\pi$	if $i_{bg} > 0$ => S_{b1} ON S_{b2} OFF if $i_{bg} < 0$ => S_{b1} OFF S_{b2} ON
Phase *c*	$4/3\pi < \theta_e < \alpha + 4/3\pi$ $1/3\pi - \alpha < \theta_e < 1/3\pi + \alpha$ $4/3\pi - \alpha < \theta_e < 4/3\pi$	if $i_{cg} > 0$ => S_{c1} ON S_{c2} OFF if $i_{cg} < 0$ => S_{c1} OFF S_{c2} ON

Assuming the output voltage $V_{DC}{}'$ is constant, actual values of Vienna rectifier input phase voltages V_{iTTR} are thus given by:

$$V_{iTTR} = S_{ij}\frac{l_{ij} - 1}{2}V_{DC}{}', \quad \begin{matrix} -\alpha < \varphi_{TTR} < \alpha \\ l_{ij} = 0, 1, 2. \end{matrix} \tag{14}$$

To avoid improper operations leading to extra power losses and voltage distortion, the angular displacement φ_{TTR} between the fundamental harmonics of voltage V_{iTTR} and current must be set lower than $|\alpha|$. Dealing with an electrical power generation application, a vector diagram of AC variables is shown in Figure 4a, where φ is the phase displacement between the PMSG back-EMF $\overline{E}_g$ and the current $\overline{I}$. δ represents the angle between the voltage $\overline{V}_{TTR}$ and the q axis, and is set to allow a reactive power flow between the Vienna rectifier and PMSG, associated to the inductive elements of the electrical machine.

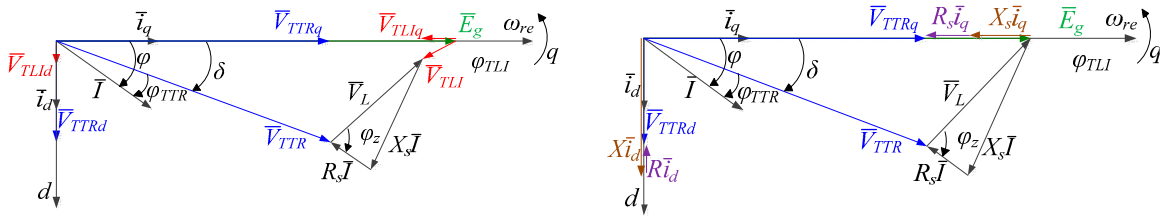


Figure 4. Vector diagram of AC variables: (**a**) considering V_{TLI}, (**b**) neglecting V_{TLI}.

Neglecting, for simplicity, the voltage V_{TLI} generated by the auxiliary inverter, which is an independent variable and whose amplitude is significantly lower than V_{i1TTR}, the amplitude of the fundamental harmonic of the TTR input voltage V_{i1TTR} is obtained as a function of the switching angle α and DC bus voltage $V_{DC}{}'$ as follows:

$$|\overline{V}_{i1TTR}| = \frac{2}{\pi}V_{DC}{}'\cos(\alpha), \; m_{TTR} = \frac{|V_{i1TTR}|}{V_{DC}{}'} \tag{15}$$

where m_{TTR} is the modulation index of the Vienna rectifier. According to the vector diagram of Figure 4b, *qd* components of the voltage can be written as:

$$\begin{array}{c} \left\{ \begin{array}{l} \overline{V}_{qTTR} = \left|\overline{V}_{i1TTR}\right|\cos(\delta) \\ \overline{V}_{dTTR} = \left|\overline{V}_{i1TTR}\right|\sin(\delta) \end{array} \right., \left\{ \begin{array}{l} \bar{i}_q = \left|\overline{I}\right|\cos(\varphi) \\ \bar{i}_d = \left|\overline{I}\right|\sin(\varphi) \end{array} \right., \left\{ \begin{array}{l} \overline{E}_{qg} = \left|\overline{E}_g\right| \\ \overline{E}_{dg} = 0 \end{array} \right., \\ \left\{ \begin{array}{l} X\bar{i}_q = -\left|X_s\overline{I}\right|\sin(\varphi) \\ X\bar{i}_d = +\left|X_s\overline{I}\right|\cos(\varphi) \end{array} \right., \left\{ \begin{array}{l} R\bar{i}_q = -\left|R\overline{I}\right|\cos(\varphi) \\ R\bar{i}_d = -\left|R\overline{I}\right|\sin(\varphi) \end{array} \right. \end{array} \quad (16)$$

while the active and reactive powers are given by:

$$\left\{ \begin{array}{l} P_{TTR} = \frac{3}{2}\left|\overline{V}_{i1TTR}\overline{I}\right|\cos(\delta - \varphi) \\ Q_{TTR} = \frac{3}{2}\left|\overline{V}_{i1TTR}\overline{I}\right|\sin(\varphi - \delta) \end{array} \right., \left\{ \begin{array}{l} P_R = -\frac{3}{2}R\left|\overline{I}\right|^2 \\ Q_X = -\frac{3}{2}X\left|\overline{I}\right|^2 \end{array} \right., \left\{ \begin{array}{l} P_g = \frac{3}{2}\left|\overline{E}_{qg}\overline{I}\right|\cos(\varphi) \\ Q_g = \frac{3}{2}\left|\overline{E}_{qg}\overline{I}\right|\sin(\varphi) \end{array} \right. \quad (17)$$

where P_{TTR} and Q_{TTR} are the active and reactive power, respectively, processed by the Vienna rectifier, P_R and Q_X are the active power wasted in the stator resistance R and the reactive power due to the PMSG synchronous reactance X_s, respectively, while P_g and Q_g are the active and reactive power delivered by the PMSG, respectively.

Neglecting the rectifier power losses, the AC power generated by the PMSG is equal to the sum of the power dissipated in the DC bus capacitor resistances R_{C1} and R_{C2} and the power delivered to the load R_L. In the Laplace domain, $V_{DC}{}'$ and the capacitor voltages V_{C1} and V_{C2} are thus given by

$$\left\{ \begin{array}{l} V_{DC}{}'(s) = \sqrt{R_L\left(P_{AC}(s) - \frac{V_{C1}^2(s)}{R_{C1}} - \frac{V_{C2}^2(s)}{R_{C2}}\right)} \\ V_{C1}(s) = V_{DC}{}'(s)\frac{sR_{C1}(1+R_{C2}C_2)}{R_{C1}+R_{C1}+sR_{C1}R_{C2}(C_1+C_2)} \\ V_{C2}(s) = V_{DC}{}'(s) - V_{C1}(s) \\ P_{AC}(s) = \frac{3}{2}\left(V_{qTTR}(s)i_q(s) + V_{dTTR}(s)i_d(s)\right) \end{array} \right. \quad (18)$$

where i_n is mainly given by the difference between the currents flowing through the two DC bus capacitors and it can be also computed as the sum of the currents flowing through the three branches of the Vienna rectifier:

$$i_n = S_{aj}i_{ag} + S_{bj}i_{bg} + S_{cj}i_{cg} \quad (19)$$

The averaged-value of i_n during a switching period T is given by

$$\bar{i}_n = \frac{1}{T}\left(T_{ONaj}i_{ag} + T_{ONbj}i_{bg} + T_{ONcj}i_{cg}\right) = \left(d_{aj}i_{ag} + d_{bj}i_{bg} + d_{cj}i_{cg}\right) \quad (20)$$

where $d_{ij} = T_{ONij}/T$ are the duty cycles of the bidirectional switches S_{ij}, according to Table 2. Figure 5 shows some simulations dealing with balanced and unbalanced DC bus voltages operations, while a block diagram of the Vienna rectifier mathematical model is shown in Figure 6.

Table 2. d_{aj}, d_{bj} and d_{cj}.

Sector I	Sector II	Sector III	Sector VI	Sector V	Sector IV
$V_{a1TTR} > 0$ $V_{b1TTR} < 0$ $V_{c1TTR} < 0$	$V_{a1TTR} > 0$ $V_{b1TTR} > 0$ $V_{c1TTR} < 0$	$V_{a1TTR} < 0$ $V_{b1TTR} > 0$ $V_{c1TTR} < 0$	$V_{a1TTR} < 0$ $V_{b1TTR} > 0$ $V_{c1TTR} > 0$	$V_{a1TTR} < 0$ $V_{b1TTR} < 0$ $V_{c1TTR} > 0$	$V_{a1TTR} > 0$ $V_{b1TTR} < 0$ $V_{c1TTR} > 0$
$d_{aj} = \frac{V_{a1TTR}}{V_{DC}{}'}$	$d_{aj} = -\frac{V_{a1TTR}}{V_{DC}{}'}$	$d_{aj} = -\frac{V_{a1TTR}}{V_{DC}{}'}$	$d_{aj} = -\frac{V_{a1TTR}}{V_{DC}{}'}$	$d_{aj} = \frac{V_{a1TTR}}{V_{DC}{}'}$	$d_{aj} = \frac{V_{a1TTR}}{V_{DC}{}'}$
$d_{bj} = \frac{V_{b1TTR}}{V_{DC}{}'}$	$d_{bj} = \frac{V_{b1TTR}}{V_{DC}{}'}$	$d_{bj} = -\frac{V_{b1TTR}}{V_{DC}{}'}$	$d_{bj} = -\frac{V_{b1TTR}}{V_{DC}{}'}$	$d_{bj} = -\frac{V_{b1TTR}}{V_{DC}{}'}$	$d_{bj} = -\frac{V_{b1TTR}}{V_{DC}{}'}$
$d_{cj} = -\frac{V_{c1TTR}}{V_{DC}{}'}$	$d_{cj} = -\frac{V_{c1TTR}}{V_{DC}{}'}$	$d_{cj} = \frac{V_{c1TTR}}{V_{DC}{}'}$	$d_{cj} = \frac{V_{c1TTR}}{V_{DC}{}'}$	$d_{cj} = \frac{V_{c1TTR}}{V_{DC}{}'}$	$d_{cj} = -\frac{V_{c1TTR}}{V_{DC}{}'}$

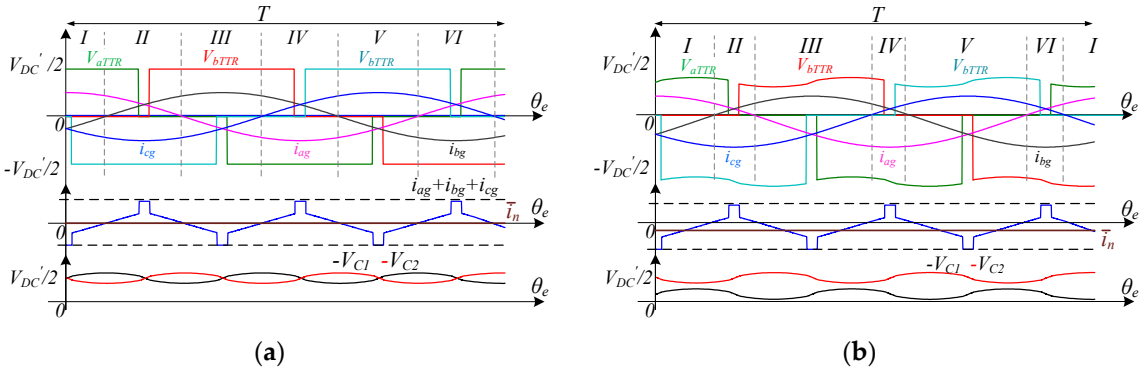


Figure 5. Averaged-value i_n, i_{abcg}, V_{c1}, V_{c2}, and V_{iTTR}. (**a**) Balanced DC bus voltages, and (**b**) unbalanced DC bus voltages.

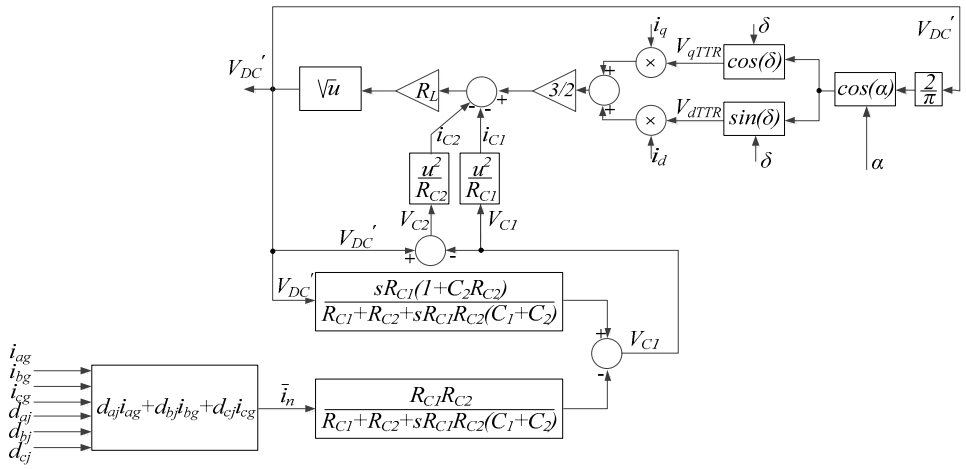


Figure 6. Block diagram of the Vienna rectifier model.

A non-null average i_n leads to unbalanced DC bus voltages [16–18]; moreover, the mean value of fundamental voltages V_{a1TTR} becomes negative if $V_{C1} < V_{C2}$ or positive if $V_{C2} < V_{C1}$. This is included in the TTR model by adding the term $\Delta V_{DC}{}' = V_{C1} - V_{C2}$:

$$\begin{cases} V_{a1TTR} = |V_{a1TTR}|\sin(\theta_e) + \Delta V_{DC}{}' \\ V_{b1TTR} = |V_{b1TTR}|\sin(\theta_e - \frac{2}{3}\pi) + \Delta V_{DC}{}' \\ V_{c1TTR} = |V_{c1TTR}|\sin(\theta_e + \frac{2}{3}\pi) + \Delta V_{DC}{}' \end{cases} \tag{21}$$

According to Table 2, by replacing (21) into (20), $\bar{i}_n$ is given by

$$\bar{i}_n = \begin{cases} m_{TTR}0.5I\left[-\cos(\varphi_{TTR}) - 2\cos(2\theta_e - \frac{4\pi}{3} - \varphi_{TTR})\right] - 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e - \frac{2\pi}{3} - \varphi_{TTR}), & 0 < \theta_e < \frac{\pi}{3} \\ m_{TTR}0.5I[\cos(\varphi_{TTR}) + 2\cos(2\theta_e - \varphi_{TTR})] - 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e - \varphi_{TTR}), & \frac{\pi}{3} < \theta_e < \frac{2\pi}{3} \\ m_{TTR}0.5I\left[-\cos(\varphi_{TTR}) - 2\cos(2\theta_e - \frac{2\pi}{3} - \varphi_{TTR})\right] - 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e + \frac{2\pi}{3} - \varphi_{TTR}), & \frac{2\pi}{3} < \theta_e < \pi \\ m_{TTR}0.5I\left[\cos(\varphi_{TTR}) + 2\cos(2\theta_e - \frac{4\pi}{3} - \varphi_{TTR})\right] + 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e - \frac{2\pi}{3} - \varphi_{TTR}), & \pi < \theta_e < \frac{4\pi}{3} \\ m_{TTR}0.5I[-\cos(\varphi_{TTR}) - 2\cos(2\theta_e - \varphi_{TTR})] - 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e - \varphi_{TTR}), & \frac{4\pi}{3} < \theta_e < \frac{5\pi}{3} \\ m_{TTR}0.5I\left[\cos(\varphi_{TTR}) + 2\cos(2\theta_e - \frac{2\pi}{3} - \varphi_{TTR})\right] + 2I\frac{\Delta V_{DC}{}'}{V_{DC}{}'}\sin(\theta_e + \frac{2\pi}{3} - \varphi_{TTR}), & \frac{5\pi}{3} < \theta_e < \pi \end{cases} \tag{22}$$

3.3. TLI Model

A key task of the TLI present in the AHUTR topology is to compensate all low-order voltage harmonics generated by the step-modulated Vienna rectifier [12]. For this reason, the TLI reference

phase voltage is equal to the difference between the AC side input voltage V_{iTTR} and its fundamental component V_{i1TTR}, as shown in Figure 7.

$$V_{iTLI}{}^{*} = V_{iTTR} - V_{i1TTR} \tag{23}$$

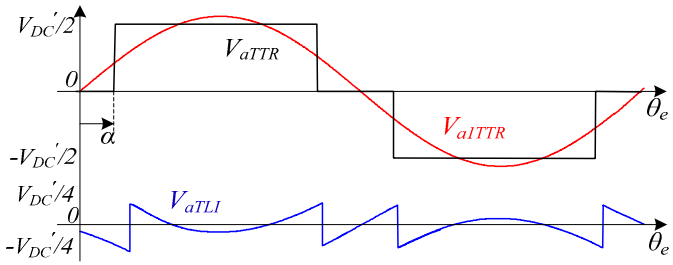


Figure 7. Two-level inverter (TLI) reference voltage for active power filtering.

Phase voltages V_{iTTR} encompass some zero sequence components, such as the 3rd, 9th, 27th, and 81st, that will not result in corresponding currents in the PMSG because the considered open-end winding topology is composed by two isolated converters. Hence, these harmonics can be neglected in the TLI reference voltages $V_{iTLI}{}^{*}$. This leads to a reduction of TLI DC bus voltage and, accordingly, to a positive impact on TLI losses. TLI reference voltages $V_{abcTLI}{}^{*}$ are thus given by

$$\begin{cases} V_{aTLI}{}^{*}(n,\theta_e) = \sum\limits_{n=5,7,11,13} b_{an} \times \sin(n\theta_e - \varphi_n) \\ V_{bTLI}{}^{*}(n,\theta_e) = \sum\limits_{n=5,7,11,13} b_{bn} \times \sin(n\theta_e - \varphi_n - \frac{2\pi}{3}) \\ V_{cTLI}{}^{*}(n,\theta_e) = \sum\limits_{n=5,7,11,13} b_{cn} \times \sin(n\theta_e - \varphi_n + \frac{2\pi}{3}) \end{cases} \tag{24}$$

Figure 8 shows the $V_{aTLI}{}^{*}$ waveform when considering a different set of zero sequence components. For each case, the minimum V_{DC}''/V_{DC}' requirement has been computed as shown in Figure 9, while current and voltage THDs are provided in Figure 10. At medium-high values of the modulation index m_{TTR}, a proper suppression of the effects of the low-order voltage harmonics produced by the Vienna rectifier is simply achieved by compensating the 5th and 7th harmonics. However, at low m_{TTR}, additional harmonics must be considered to keep the THDs suitably low.

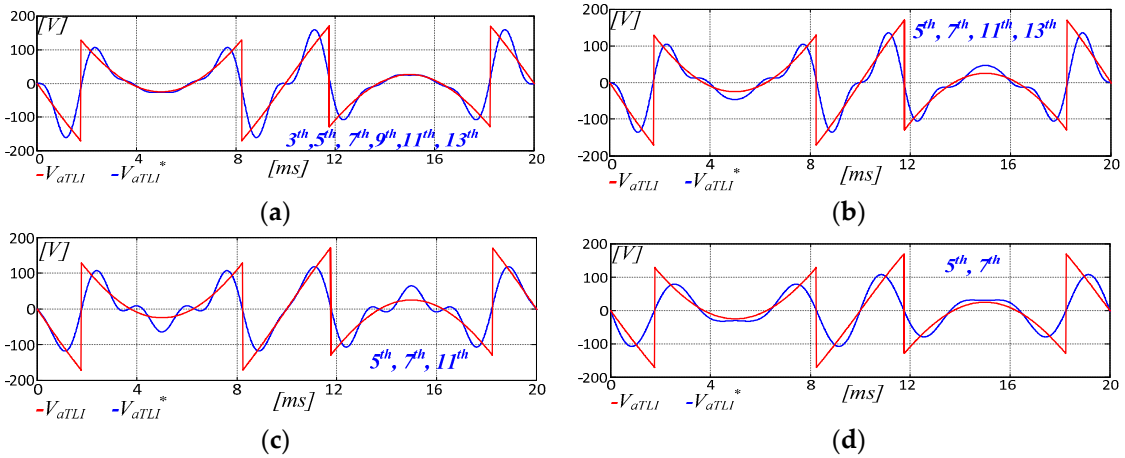


Figure 8. TLI reference voltage approximation. (**a**) 3rd, 5th, 7th, 9th, 11th, 13th. (**b**) 5th, 7th, 11th, 13th. (**c**) 5th, 7th, 11th. (**d**) 5th, 7th.

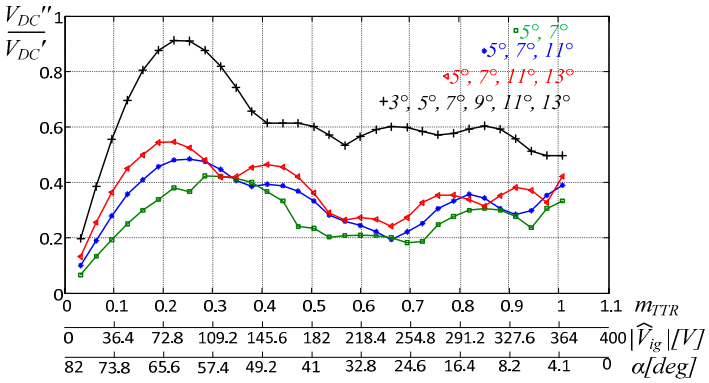


Figure 9. Minimum V_{DC}''/V_{DC}' requirement vs. peak amplitude of PMSG phase voltage, m_{TTR}, and α.

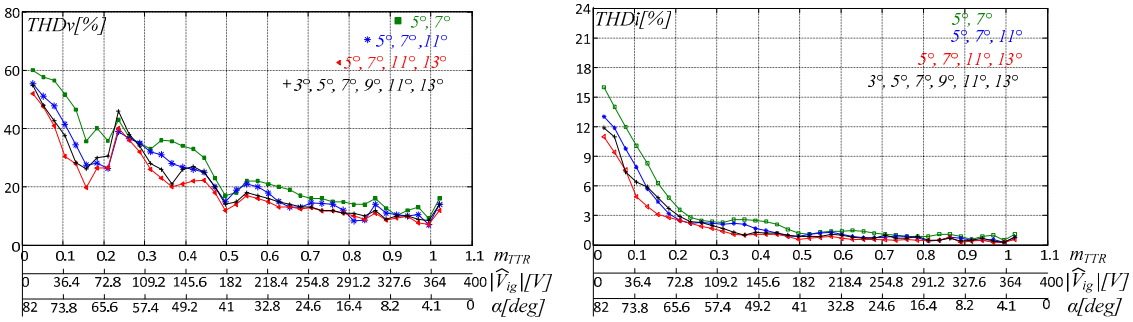


Figure 10. *THDv* and *THDi* vs. the peak amplitude of PMSG phase voltage.

As shown in Figure 2, a closed loop input current control system is added to the predictive filter in order to cope with unmodeled non-linearities and improve the input current waveform as well as the system dynamic response. By equaling the active power generated by the PMSG to the output DC power, the reference q-axis current i_q^* is computed from actual values of α, δ and the output DC current i_{DC} as:

$$i_q^* = \frac{\pi i_{DC}}{3\cos(\alpha)\cos(\delta)},\ i_d^* = 0 \tag{25}$$

The d-axis reference current i_d^* can be simply set to zero or suitably determined in case of interior permanent magnet structures in order to operate the PMSG according to a maximum power per ampere strategy.

Another key function of the TLI is to balance the voltage across the DC bus capacitors of the Vienna rectifier, making unnecessary additional circuits. As shown in Figure 2, this goal is obtained by acting on the q-axis component of the TLI reference current in order to control the amplitude of i_n, which is given by the difference between the currents flowing through the two DC bus capacitors.

The DC side of the TLI is modeled by balancing the AC and DC side power, neglecting the power switches losses (Equation (26)). The TLI DC-link includes the resistance R_{CT} representing the floating capacitor losses, while V_{qTLI} and V_{dTLI} are the voltage components of TLI V_{jTLI} in the qd axis, as shown in Figure 11.

$$\begin{cases} P_{AC} = P_{DC2} = \frac{3}{2}\left(V_{qTLI}i_q + V_{dTLI}i_d\right) \\ P_{DC2} = V_{DC}''i_{DC}'' + \frac{{V_{DC}''}^2}{R_{CT}} = V_{DC}''C_T s V_{DC}'' + \frac{{V_{DC}''}^2}{R_{CT}} = \frac{3}{2}\left(V_{qTLI}i_q + V_{dTLI}i_d\right) \end{cases} \tag{26}$$

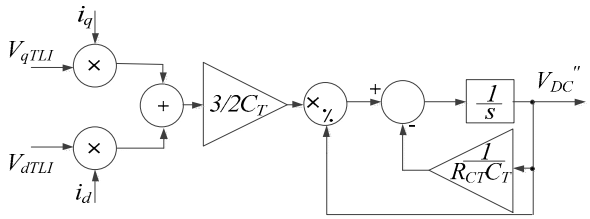


Figure 11. Block diagram of TLI model.

4. Model Validation

An electric power generation application has been considered for validating the value-averaged model. Specifically, the proposed model represented with the blocks scheme of Figure 12 has been implemented in a Simulink environment and compared to a detailed model of the system developed in the same environment exploiting the SimPower System Toolbox, which is a circuit-based modeling platform widely used for the simulation of power electronic converters, electromechanical systems, and their control systems. The last model includes both converter topologies. The control scheme used on both models is shown in Figure 2, including low-order harmonic compensation and DC bus capacitor voltages balancing [14]. Simulation settings are summarized in Table 3, where $k_{P\alpha}$ and $k_{I\alpha}$ are the proportional and integral gains of the output DC voltage controller, while k_{Piq}, $k_{Iiq,}$ k_{Pid}, and k_{Iid} are the proportional and integral gains of *qd* PMSG current regulators; k_{Pin} and k_{Iin} are the proportional and integral gains of the Vienna rectifier DC bus voltage equalization system; and k_{PTLI} and k_{ITLI} are the proportional and integral gains of the TLI DC Bus voltage controller. Figures 13 and 14 show simulation results obtained with the SimPower System model and the averaged-value model, showing a purposely generated Vienna rectifier DC bus voltage unbalance with the balance system not activated. Specifically, capacitor voltages V_{C1} and V_{C2}, which at the beginning are equal because R_{C1} and R_{C2} are both set to 1000 Ω, diverge after t = 3 s because R_{C2} is changed to 600Ω in order to generate the voltage unbalance. The i_n current is zero when capacitor voltages are balanced and greater than zero after t = 3 s, while DC bus voltages V_{DC}' and V_{DC}'' do not vary. A zoomed-in view of the balanced and unbalanced steady-state operations of Figures 13 and 14 are shown in Figures 15 and 16, confirming a good matching between the results obtained with the two models. Figures 15d and 16d show the instantaneous Vienna rectifier power losses P_{TTR}, TLI power losses P_{TLI}, and PMSG power losses P_{Lg} during balanced DC bus capacitors. A one-time variation of the references of the output voltage and the TLI DC bus voltage is considered in Figures 17 and 18, while a load variation is shown in Figures 19 and 20. The results achieved with the two models are very close, but using the averaged-value model, the simulation time is roughly one third. In particular, all simulations have been accomplished on an Intel®CoreTM i7 CPU with 2.60 GHz and 16 GB RAM running a 64-bit Windows 10 operating system. Simulation results shown in Figures 13–20 required three minutes computing time using the SimPower System model with a 10^{-6} s time step. A 10^{-5} s time step can be used with the averaged-value model, because high frequency voltage and current harmonics are neglected, leading to only ten seconds to accomplish the same simulation.

Table 3. System parameters.

PMSG		Vienna		TLI	Control Gains
Power Rating	3 kW	IGBT Ratings	600 V, 20 A	200 V, 10 A	$K_{P\alpha}$ = 0.1, $K_{I\alpha}$ = 10
Rated Voltage	575 V_{DC}	DC-Link Voltage	200 V	100 V	K_{Piqg} = 80, K_{Iiqg} = 1000
Rated Current	6.5 A	DC Bus Capacitors	470 µF (C_1, C_2)	470 µF (C_T)	K_{Pidg} = 80, K_{Iidg} = 1000
Phase Inductance	20 mH	Load	50 Ω	//	K_{Pin} = 0.2, K_{Iin} = 2
Stator Resistance	4.3 Ω	Capacitors Resistance	1000 Ω (R_{C1}, R_{C2})	600 Ω (R_{CT})	K_{PTLI} = 2, K_{ITLI} = 30
PM Flux	0.57 Wb	Switching Frequency	50 Hz	40 kHz	

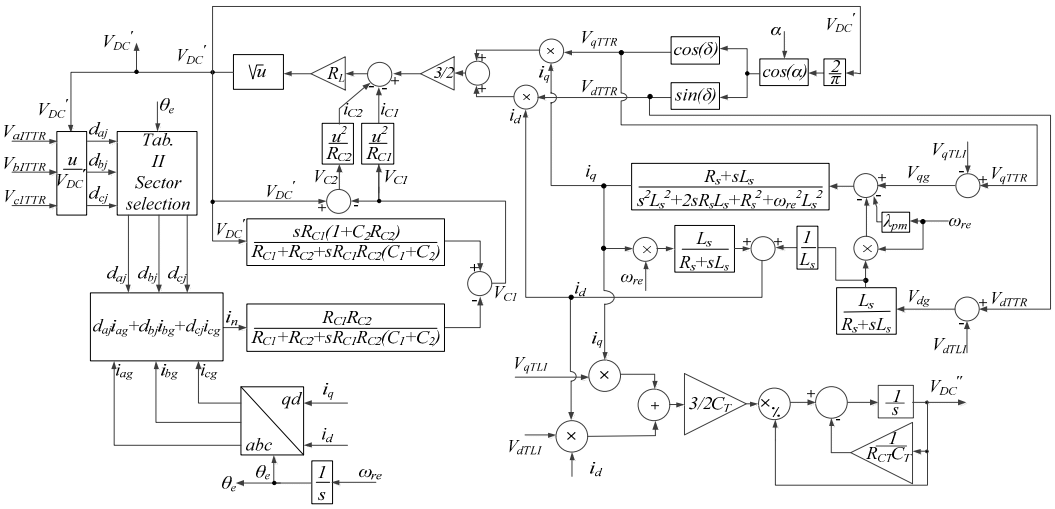


Figure 12. Block diagram of the developed averaged-value model.

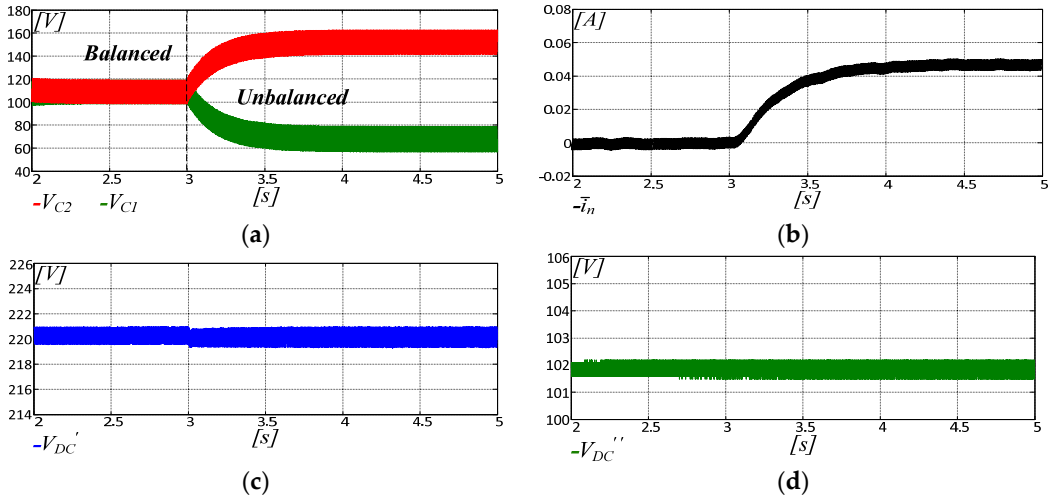


Figure 13. SimPower System model. (**a**) DC bus capacitor voltages V_{C1} and $V_{C2.}$ (**b**) $i_n = i_{C1} - i_{C2}$. (**c**) output voltage V_{DC}'. (**d**) TLI DC bus voltage V_{DC}''.

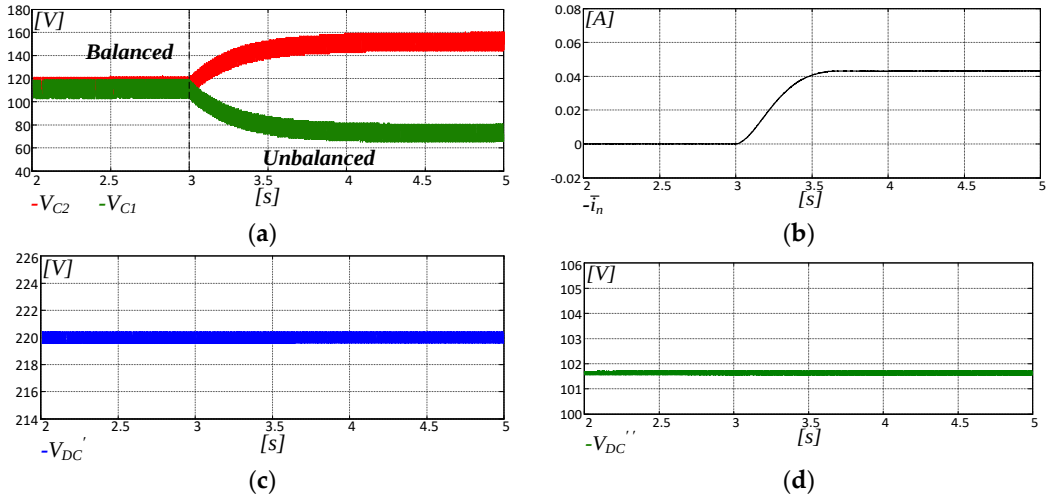


Figure 14. Averaged-value model. (**a**) DC bus capacitor voltages V_{C1} and $V_{C2.}$ (**b**) $i_n = i_{C1} - i_{C2}$. (**c**) output voltage V_{DC}'. (**d**) TLI DC bus voltage V_{DC}''.

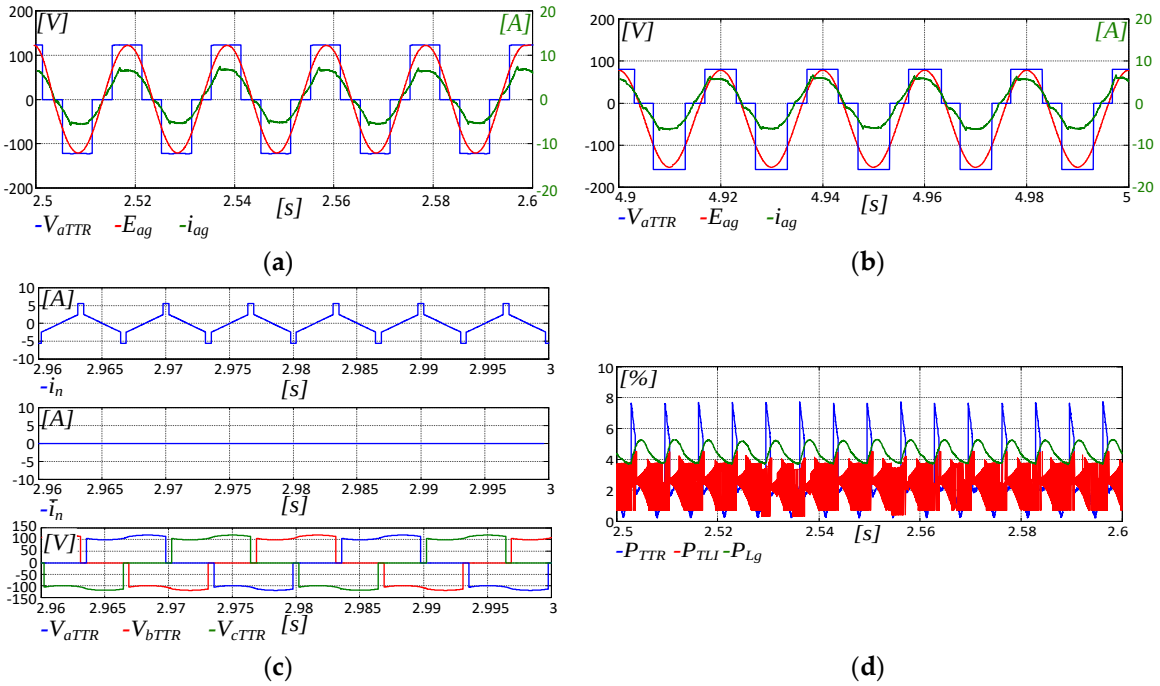


Figure 15. SimPower System model. (**a**) Balanced DC bus capacitor voltage operations, V_{aTTR}, E_{ag}, and i_{ag}. (**b**) Unbalanced DC bus capacitor voltage operations. (**c**) Current i_n, average value $\bar{i}_n$, and AC input Vienna voltages V_{iTTR}. (**d**) TRR power losses P_{TTR}, TLI power losses P_{TLI}, and PMSG power losses P_{Lg}.

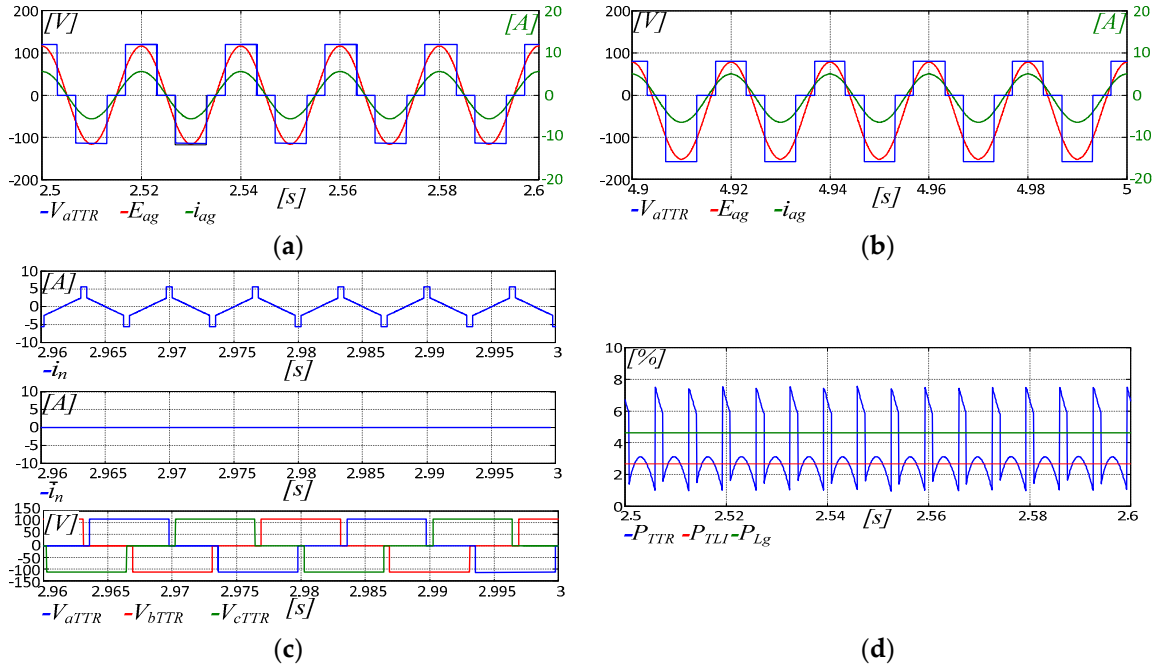


Figure 16. Averaged-value model. (**a**) Balanced DC bus capacitor voltage operations, V_{aTTR}, E_{ag}, and i_{ag}. (**b**) Unbalanced DC bus capacitor voltage operations. (**c**) Current i_n, average value $\bar{i}_n$, and AC input Vienna voltages V_{iTTR}. (**d**) TRR power losses P_{TTR}, TLI power losses P_{TLI}, and PMSG power losses P_{Lg}.

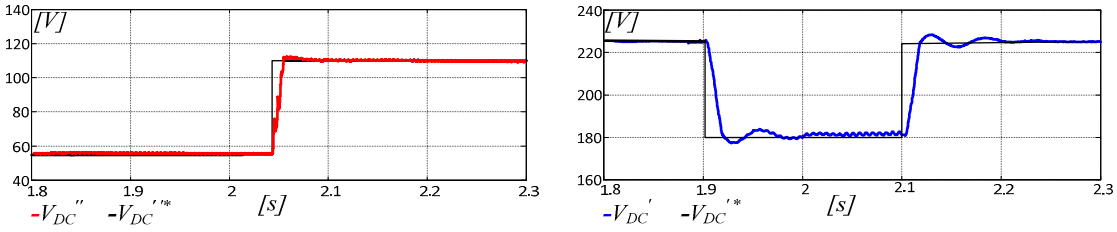


Figure 17. SimPower System model. One-time variation of V_{DC}' and V_{DC}'' references. (**a**) TLI DC bus voltage V_{DC}''. (**b**) Output voltage V_{DC}'.

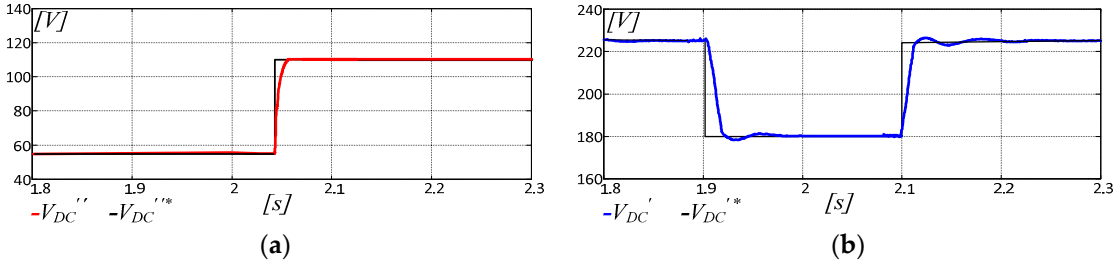


Figure 18. Averaged-value model. One-time variation of V_{DC}' and V_{DC}'' references. (a) TLI DC bus voltage V_{DC}''. (**b**) Output voltage V_{DC}'.

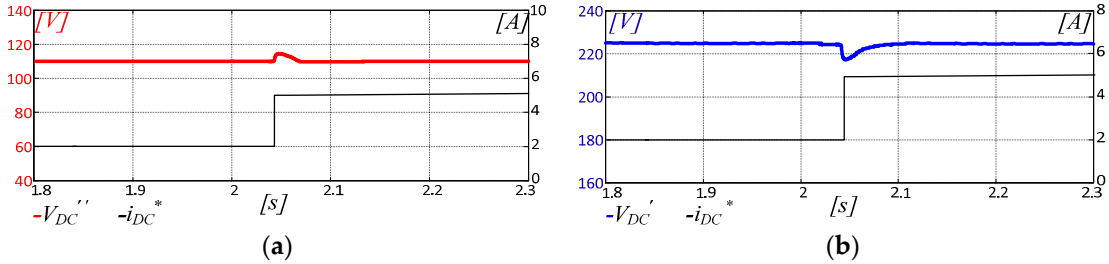


Figure 19. SimPower System model. Load variation i_{DC}^{*}. (**a**) TLI DC bus voltage V_{DC}''. (**b**) Output voltage V_{DC}'.

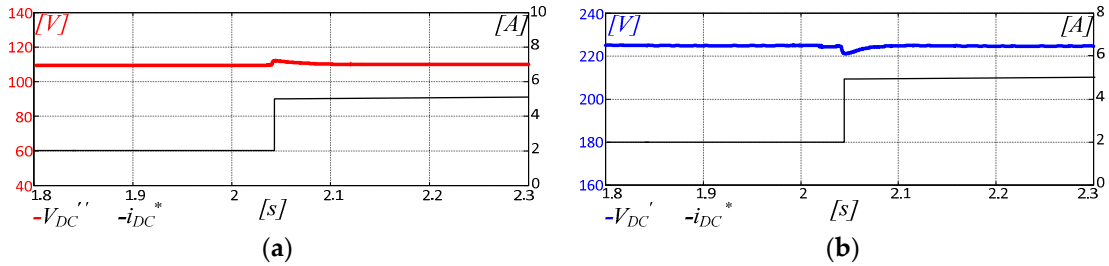


Figure 20. Averaged-value model. Load variation i_{DC}^{*}. (**a**) TLI DC bus voltage V_{DC}''. (**b**) Output voltage V_{DC}'.

Figure 21 displays the maximum errors between the quantities carried out by the two models, confirming a good accuracy of the proposed average model in a wide range of load conditions.

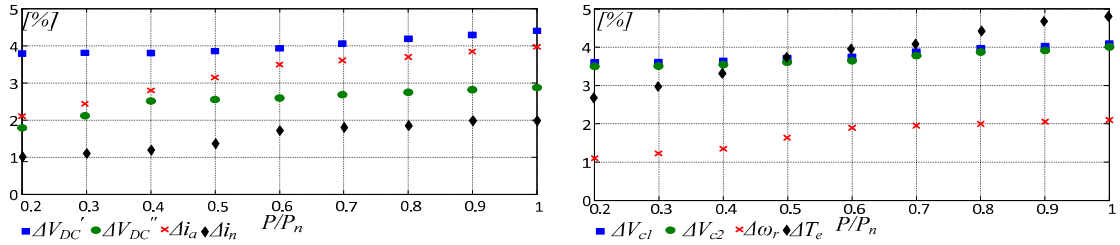


Figure 21. Percentage error between SymPower System and averaged model vs. the power expressed in per unit P/P_n. (**a**) Errors of V_{DC}', V_{DC}'', i_a, and i_n. (**b**) Errors of V_{c1}, V_{c2}, ω_r and T_e. Note: ω_r = 200 rad/s, V_{DC}' = 400 V, and V_{DC}'' = 100 V.

5. Experimental Assessment

The accuracy of the AHUTR analytical model has also been verified comparing the results from the model with those from an experimental test rig consisting of 1kW AHUTR supplying an open-end-winding PMSG, mechanically coupled to a 2.6 kW PM synchronous motor drive used as a prime mover. Technical specifications of the PMSG are given in Table 4. This AHUTR supplied DC loads at 400V through the Vienna rectifier equipped with insulated gate bipolar transistors (IGBTs) whose technical data are listed in Table 5. The TLI was realized with low-voltage power metal-oxide-semiconductor field-effect transistor (MOSFETs) and operated at 40 kHz, V_{DC}'' = 100 V. Technical data of the power MOSFETs are reported in Table 6. The TLI floating capacitor and both capacitors C_1, C_2 were equal to 470µF. The DC load was modified using a variable power resistor. A single dSPACE DS1103 control board was used to control the Vienna rectifier and the TLI, while a 2048 ppr encoder was used to measure the rotor position θ_r of the PMSG. The experimental setup is shown in Figure 22. The currents and voltages were measured by using a dedicated sensing board equipped with the current transducer LEM LA 55-P and voltage transducer LEM LV 25-P.

Table 4. PMSG technical data.

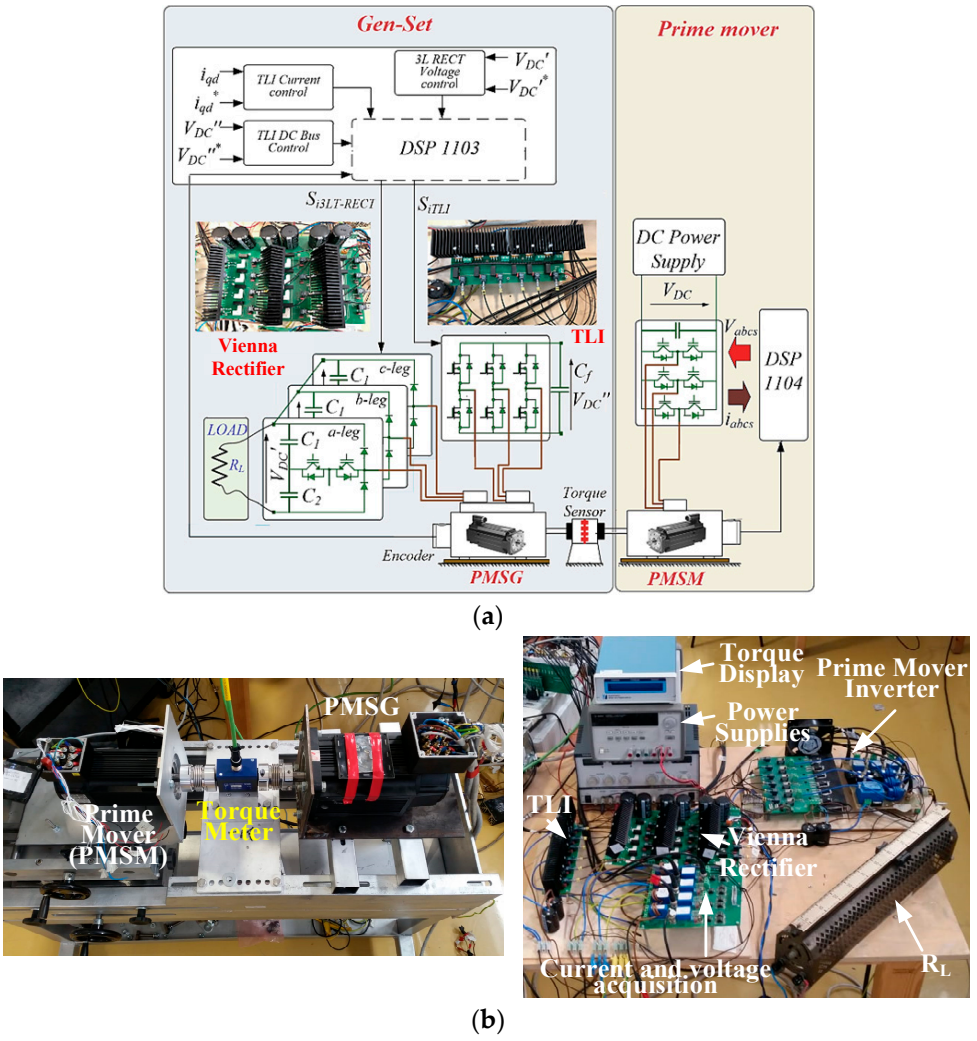
P_n (kW)	L_s (mH)	V_s (V)	R_s (Ω)	I_s (A)	λ_{PM} (Wb)	ω_r (krpm)	Pole Pairs
1	20	565	4.8	6.5	1.53	2	3

Table 5. Technical specifications of STGW30NC60KD IGBT.

V_{ce} (V)	$V_{ce}(on)$ (V)	i_{RMS} (A)	t_{rise} (ns)	t_{fall} (ns)
600	2.1	30	27	160

Table 6. Technical specifications of IRFB5615PBF MOSFET.

V_{DS} (V)	R_{DS} (m)	I_D (A)	t_{rise} (ns)	t_{fall} (ns)
150	32	35	8.9	17.2



(**a**)

(**b**)

Figure 22. Experimental test bench. (**a**) Block scheme. (**b**) Experimental setup.

The experimental results shown in Figure 23 were obtained by imposing a transient voltage to V_{DC}' from 400 V to 320 V by keeping a constant resistor value R_L = 80 Ω and with the PMSG spinning at ω_r = 200 rad/s. Note a satisfying accuracy in the mechanical and electrical quantities estimated by the model. The voltage V_{DC}'' was properly modified by the control algorithm in order to keep the optimal ratio between the DC bus voltages V_{DC}' and V_{DC}''. A different test is displayed in Figure 24 in which a speed transient was forced by acting on the prime mover. More specifically, the rotational speed ω_r was changed from 200 rad/s to 260 rad/s while the resistive load was still kept constant. Even in this case, the model accurately predicted the behavior of the drive, both at steady-state and transient. The DC bus voltages were both affected by the speed variation, but the feedback control loops restored the reference values. A step load variation was imposed in the test of Figure 25, where the DC load was purposely doubled by switching from T_L = 2 Nm to T_L = 4 Nm. In this case, a more remarkable difference was observed between the model and the experimental results. Finally, the effectiveness of the model to predict the balancing of the voltages across the DC bus capacitors is shown in Figure 26. Initially, the balancing algorithm described in the previous sections was inactive, and thus, the voltages at the terminals of C_1 and C_2 were significantly different. At the instant t^*, the voltage-balancing approach was activated, nullifying $V_{C1} - V_{C2}$. The results of Figure 26 confirm the capability of the model to accurately simulate even this critical issue of the AHUTR. Maximum percentage errors between the outputs of the SimPower System and the averaged-value model are

summarized in Table 7, where the quantities with the suffix Δ are the errors in estimating $V_{DC}{}'$, ω_r, T_e, $V_{DC}{}''$, i_n, V_{c1}, and V_{c2}.

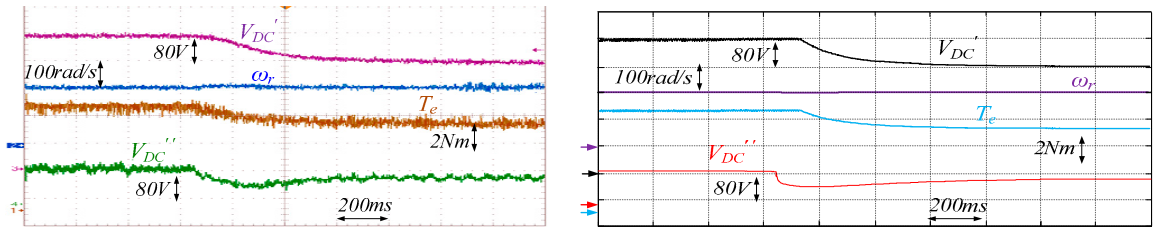


Figure 23. Voltage transient of $V_{DC}{}'$ from 400 V to 320 V under a constant resistor value R_L = 80 Ω. Output voltage $V_{DC}{}'$, TLI DC bus voltage $V_{DC}{}''$, rotor speed ω_r, electromagnetic torque T_e. (**a**) Experimental results. (**b**) Simulation results.

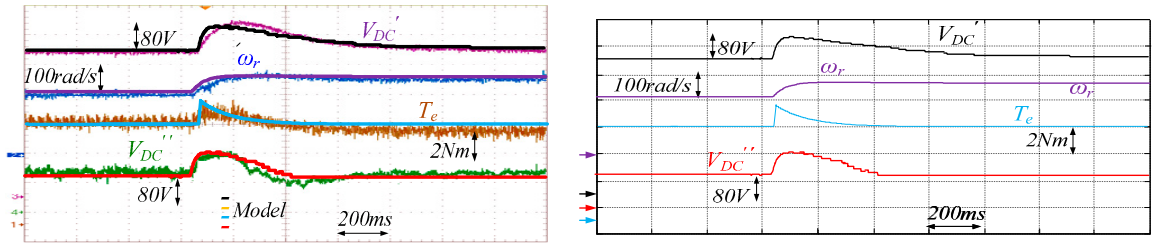


Figure 24. Speed transient from ω_r = 200 rad/s to ω_r = 260 rad/s under a constant resistor value R_L = 80 Ω and $V_{DC}{}'$ = 400 V, $V_{DC}{}''$= 100 V. Output voltage $V_{DC}{}'$, TLI DC bus voltage $V_{DC}{}''$, rotor speed ω_r, electromagnetic torque T_e. (**a**) Experimental results. (**b**) Simulation results.

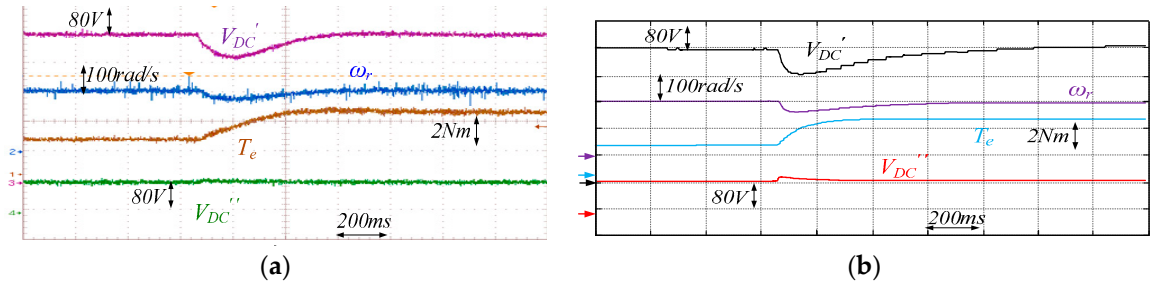


Figure 25. Load transient from T_L = 2 Nm to T_L = 4 Nm at ω_r = 200 rad/s and $V_{DC}{}'$ = 400 V, $V_{DC}{}''$ = 100 V. Output voltage $V_{DC}{}'$, TLI DC bus voltage $V_{DC}{}''$, rotor speed ω_r, electromagnetic torque T_e. (**a**) Experimental results. (**b**) Simulation results.

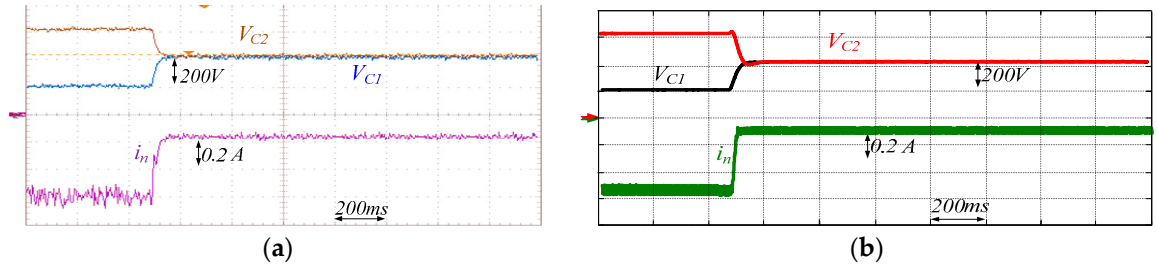


Figure 26. DC bus voltage balancing: T_L = 4 Nm, ω_r = 200 rad/s and $V_{DC}{}'$= 400 V, $V_{DC}{}''$ = 100 V. V_{c1}, V_{c2} and i_n. (**a**) Experimental results. (**b**) Simulation results.

Table 7. Errors between experimental results and those obtained with the averaged-value model.

Test	$\Delta V_{DC}'$ (%)	$\Delta\omega_r$ (%)	ΔT_e (%)	$\Delta V_{DC}''$ (%)	$\Delta i_n'$ (%)	ΔV_{C1} (%)	ΔV_{C2} (%)
Figure 22	2.2	1.9	3.7	4.7	/	/	/
Figure 23	2.1	2.6	5	7.7	/	/	/
Figure 24	4.5	4.9	6	5	/	/	/
Figure 25	/	/	/	/	6.6	10	4

6. Conclusions

The asymmetrical hybrid unidirectional T-type rectifier is more efficient than a conventional PWM rectifier, mainly due to line frequency operation of the main converter, a T-type rectifier. However, it features a more complex structure composed of three main components, namely a TTR, a TLI, and an open winding electric machine, all interacting. The development of an accurate averaged-value mathematical model of the AHUTR topology aimed to optimally design control and management algorithms has been faced in the paper. Simulations and experimental results show that the proposed model is able to reproduce the static and dynamic behavior of the AHUTR with good accuracy. Furthermore, the obtained mathematical representation made a fast analysis of the system during TTR DC bus voltage unbalance operations possible. This has been exploited to design an active balancing system acting on the TLI side—a task which would be time-consuming with circuit-oriented simulator models. Furthermore, the averaged-value model has been used to define the entire AHTUR control and management system tasked to deal with efficiency maximization, input power factor control, TTR DC bus capacitor voltage balance, and the control of TLI floating DC bus voltage.

Author Contributions: This work was carried out in collaboration between all authors. S.F., G.S. and A.T. designed the study, wrote the manuscript and analyzed simulations and experimental results. A.S. undertook all of the experimental measurements.

Conflicts of Interest: The authors declare no conflict of interest.

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