Low-Noise Programmable Voltage Source

Krzysztof Achtenberg [1],*, **Janusz Mikołajczyk** [1], **Carmine Ciofi** [2], **Graziella Scandurra** [2] **and Zbigniew Bielecki** [1]

[1] Institute of Optoelectronics, Military University of Technology, 00908 Warsaw, Poland; janusz.mikolajczyk@wat.edu.pl (J.M.); zbigniew.bielecki@wat.edu.pl (Z.B.)

[2] Department of Engineering, University of Messina, 98166 Messina, Italy; cciofi@unime.it (C.C.); gscandurra@unime.it (G.S.)

* Correspondence: krzysztof.achtenberg@wat.edu.pl

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Abstract: This paper presents the design and testing of a low-noise programmable voltage source. Such a piece of instrumentation is often required as part of the measurement setup needed to test electronic devices without introducing noise from the power supply (such as photodetectors, resistors or transistors). Although its construction is based on known configurations, here the discussion is focused on the characterization and the minimization of the output noise, especially at very low frequencies. The design relies on a digital-to-analog converter, proper lowpass filters, and a low-noise Junction Field-Effect Transistors (JFET) based voltage follower. Because of the very low level of output noise, in some cases we had to resort to cross-correlation in order to reduce the background noise of the amplifiers used for the characterization of the programmable source. Indeed, when two paralleled IF9030 JFETs are used in the voltage follower, the output noise can be as low as 3 nV/$\sqrt{\text{Hz}}$, 0.6 nV/$\sqrt{\text{Hz}}$ and 0.4 nV/$\sqrt{\text{Hz}}$ at 1 Hz, 10 Hz and 100 Hz, respectively. The output voltage drift was also characterized and a stability of ±25 μV over 3 h was obtained. In order to better appreciate the performance of the low-noise voltage source that we have designed, its noise performances were compared with those of a set-up based on one of the best low-noise solid-state voltage regulators available on the market. Actual measurements of the current noise in a type-II superlattice photodetector are reported in which the programmable source was used to provide the voltage bias to the device.

Keywords: low-noise voltage source; low-frequency noise; cross-correlation; field effect transistors; low-noise instrumentation; noise measurements

1. Introduction

Identification and measurement of noise signals are crucial for many electronic devices [1]. This is not only important for device characterization, but also for the study and a deep understanding of microscopic physical phenomena and technologies. For example, noise characterization is needed in order to understand the fundamental causes of the detection limit in spectroscopy [2,3], data link budgets in free-space optics, etc. In the case of biased devices (such as transistors [4,5], varistors [6], photodetectors [7–13] and other materials [14–17]), the noise introduced by the biasing devices is also very important because it can mask the noise generated by the devices being investigated or limit the performances of the designed instruments. Indeed, in order to perform reliable noise characterization, we need to resort to ultra-low-noise power supply units that introduce negligible noise levels compared to those generated by the device-under-test (DUT). The simplest implementation of such low-noise supplying units consists of resorting to batteries (often lead acid, NiCd or NiMH accumulators) that, under proper conditions, behave like very low-noise voltage sources. However, the fact that we can only use a combination of elementary cells limits the resolution that can be obtained in setting the

desired voltage. Moreover, the voltage changes with time because of discharge. To obtain an adjustable and stable voltage source, it is possible to use a set of batteries and a low-noise linear voltage regulator. This is a simple configuration, but low-noise solid-state regulators, while labeled "low-noise", are still characterized by large levels of noise, especially at low frequencies when compared to batteries [18–23]. The relatively high level of noise is also the reason why commercial voltage sources, while providing a high range of voltage settings, cannot be employed in many cases [24]. Very often, in order to overcome the limitations of commercial programmable sources, dedicated systems need to be designed for obtaining high sensitivity in the case of low-frequency noise measurements. A few of such voltage sources were described in the literature. In [25], a low-noise programmable voltage source is presented with a discrete resistor *R2R* ladder network digital–analog converter (DAC) and a cascaded JFET low-noise follower. Low noise is obtained based on a battery being used as a reference and the DAC being based on excess-noise-free discrete resistors. High output current in this source was obtained by resorting to a low-noise power buffer output at the output of the DAC. Its noise voltage spectral density (VSD) is about 10 nV/$\sqrt{\text{Hz}}$ at 1 Hz when delivering currents in the hundred mA range. In [26], an *RC* filter with 15 mF supercapacitors was used to effectively filter out, down to very low frequencies, the noise generated by a solid-state Digital to Analog Converter (DAC). A compensation circuit was also added in order to compensate for errors in the generated voltage due to the significant supercapacitor leakage current. The output noise of this voltage source was about 4.5 nV/$\sqrt{\text{Hz}}$ at 1 Hz and 3.5 nV/$\sqrt{\text{Hz}}$ above few Hz. A low-noise voltage reference was also presented in [27]. It is built of a high output current DAC, a lowpass supercapacitor filter, and a voltage follower. Its noise voltage is about 15 nV/$\sqrt{\text{Hz}}$ at 1 Hz and 1.2 nV/$\sqrt{\text{Hz}}$ at 1 kHz. Another solution proposed in [28] exploits the very low-noise SSM2220 transistors that, when connected as diodes and biased by a solid-state voltage reference (AD586), and provided that strict temperature control is obtained, can behave as a very low-noise, fixed-voltage reference, from which an adjustable low-noise voltage source can be obtained, with noise levels of about 7.7 nV/$\sqrt{\text{Hz}}$ and 3.9 nV/$\sqrt{\text{Hz}}$ at 1 Hz and 10 Hz, respectively. Another realization [29] relies on filtering out the noise at the output of a conventional DAC and using a low-noise JFET transistor IF3601 as an output buffer, with auxiliary subsystems employed to insure reduced transient times and high accuracy and stability. This last system is characterized by a noise level of 4.5 nV/$\sqrt{\text{Hz}}$ at 1 Hz and below 3.5 nV/$\sqrt{\text{Hz}}$ above 10 Hz. The performances of these systems, together with the performances that can be obtained with commercial instrumentation, are summarized in Table 1.

Table 1. Noise performances of some programmable voltage sources.

Output Voltage (V)	Noise VSD	References
0 to 5	14nV/$\sqrt{\text{Hz}}$ (0.1 Hz) <3 nV/$\sqrt{\text{Hz}}$ (above 1 Hz)	[29]
0 to 210	≈300 nV/$\sqrt{\text{Hz}}$ (1 Hz) 100 nV/$\sqrt{\text{Hz}}$ (10 Hz) 2 nV/$\sqrt{\text{Hz}}$ (1 kHz)	Keysight B2961A (values for 2 V range) [30]
±20	≈ 300 nV/$\sqrt{\text{Hz}}$ (1 Hz) <200 nV/$\sqrt{\text{Hz}}$ (10 Hz to 100 Hz) ≈70 nV/$\sqrt{\text{Hz}}$ (1 kHz)	Stanford Research SIM928 [31]
±15	<100 nV/$\sqrt{\text{Hz}}$ (10 Hz) ≈10 nV/$\sqrt{\text{Hz}}$ (100 Hz)	NF LP5393 [32]
0 to 8	1 mV/$\sqrt{\text{Hz}}$ (0.01 Hz) 31 nV/$\sqrt{\text{Hz}}$ (0.1 Hz) 10 nV/$\sqrt{\text{Hz}}$ (1 Hz)	[25]
0 to 8	4.5 nV/$\sqrt{\text{Hz}}$ (1 Hz) 3.5 nV/$\sqrt{\text{Hz}}$ (above few Hz)	[26]

Output Voltage (V)	Noise VSD	References
not defined	≈ 15 nV/$\sqrt{\text{Hz}}$ (1 Hz) ≈ 3 nV/$\sqrt{\text{Hz}}$ (10 Hz) 1.2 nV/$\sqrt{\text{Hz}}$ (1 kHz)	[27]
0 to 3.3	≈ 3 nV/$\sqrt{\text{Hz}}$ (1 Hz) 0.6 nV/$\sqrt{\text{Hz}}$ (10 Hz) 0.4 nV/$\sqrt{\text{Hz}}$ (1 kHz)	This work (with IF9030)

In this paper, a new design for the realization of a low-noise programmable voltage source is proposed. While the design is inspired from [29], a number of modifications are introduced that result in much lower levels of noise. While such a piece of instrumentation can be effective in many applications in the field of low frequency noise measurements, the design originated from the need for a low-noise bias source to be used for investigating the noise in a novel infrared detector at frequencies down to 1 Hz. Indeed, the effectiveness of the design we propose is demonstrated by the result of actual noise measurements performed on these devices.

The design of the new programmable source will be discussed in detail in the next section.

2. Design of the Proposed Low-Noise Voltage Source

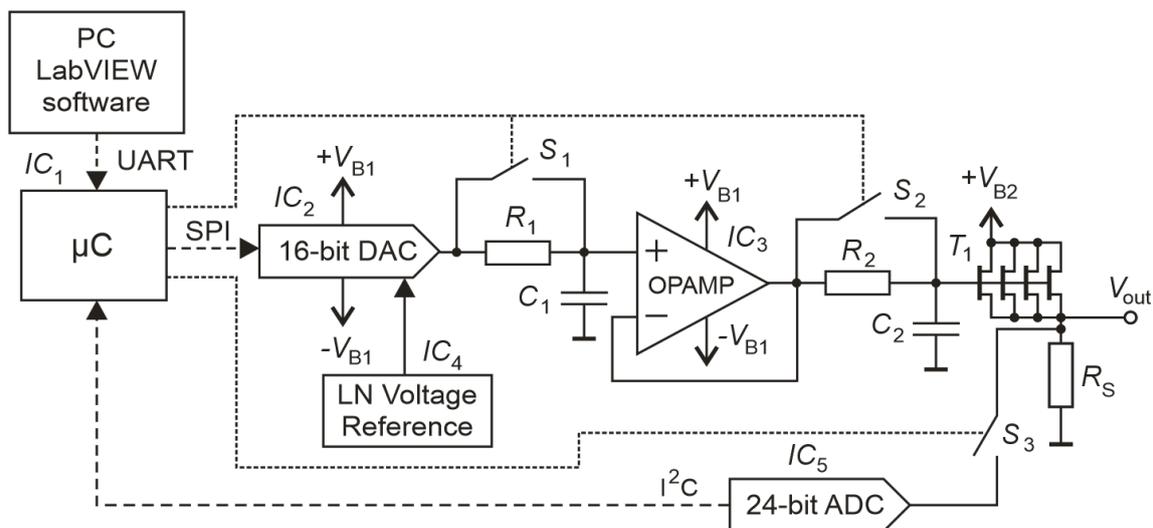The schematic diagram of the proposed voltage source is shown in Figure 1.

Figure 1. Schematic diagram of the proposed low voltage source.

The ATmega32 microcontroller (IC_1) supervising the operation of the system is controlled by a personal computer (PC) running a dedicated LabVIEW software via an insulated Universal Asynchronous Receiver-Transmitter (UART) interface to reduce interferences. For this purpose, we developed a simple board based on optocouplers (LTV817 by LITEON). The microcontroller drives the bipolar *DAC* model AD5761R (IC_2) used to generate a programmable voltage. The DAC is supplied by lead acid batteries to reduce interferences from external environment. In order to insure low temperature drift and longtime stability at the DAC output, the low-noise voltage reference ADR441B (IC_4) was used. It is characterized by a temperature coefficient as low as 1 ppm/°C (max. of 3 ppm/°C). In order to obtain low noise, the DAC output voltage is filtered using two-stage lowpass RC filters separated by a low drift JFET input OPA140 operational amplifier (IC_3). The corner frequency of the first lowpass stage ($R_1 C_1$) is 0.0023 Hz, while that of the second stage ($R_2 C_2$) is 0.0016 Hz. Overall, the two cascaded lowpass filters provide an attenuation of the noise coming from the DAC of more

than 60 dB at 0.001 Hz. The lowpass filters were built of film resistors and stable metallized polyester capacitors (WIMA MKS2). It must be noted that the resistances in the filers are sources of noise (thermal noise). However, at the output of an *RC* filter and well above the corner frequency, the voltage noise V_{nRC} is given by:

$$V_{nRC} = \sqrt{4kTR\frac{f_c^2}{f^2}},\tag{1}$$

where f is the frequency, $f_c = 1/(2\pi RC)$ and k is the Boltzmann constant. With the values of the resistors and capacitors used in our design, this contribution becomes negligible above 0.001 Hz.

In order to provide current to the load, the voltage at the output of the second RC filter is buffered by a low-noise source follower consisting of the selected four-paralleled 2SK3557-6s or two paralleled IF9030 JFET transistors. Their drains were supplied by high-capacity NiMH batteries. To minimize the current noise generated by gate leakage current, that increases as the drain-to-gate voltage increases, a relatively low-supply voltage ($V_{B2} \approx 6.5$ V) was used. Clearly, the DC voltage at the output of the system is not equal to the voltage at the output of the second filter because of the V_{GS} of the JFETs. The output voltage can however be monitored by the high-resolution (24-bit) analog–digital converter LTC2493 [33] (IC_5). In this way, the voltage of the DAC can be adjusted in order to obtain the desired output voltage. The S_1 and S_2 switches were used to speed up the charging/discharging process of filtering capacitors, which is particularly useful when setting any new output value. Finally, once steady state is obtained, the ADC input can be disconnected from the output in order to minimize interferences from the control system. The fact that the DAC can produce negative voltages makes it possible to obtain a 0 V output voltage. As far as the maximum output voltage is concerned, it mainly depends on the supply voltage V_{B2}, the R_S resistor, and the value of the pinch-off voltage $V_{GS(off)}$ of the JFET voltage of the used transistors. Note that, because the gate voltage (V_G) from DAC changes the bias point of the JFETs and hence the value of the their transconductance gain g_m, the output resistance R_{OUT} of the source depends on the generated voltage since $R_{OUT} = R_S \| (1/g_m)$. Parallelizing the JFETs at the output allows one to reduce the contribution of the noise introduced by the JFETs themselves by a factor $\sqrt{N}$ where N is the number of parallelized devices. We tested the system both with four parallelized 2SK3557-6 JFETs and with two parallelized IF9030s.

3. Test of the Designed Voltage Source

3.1. Measurement Setup

Since the main goal of this work is to demonstrate a very low-noise voltage source, the most important parameter to be characterize is, obviously, the level of noise that can be obtained at the output of the system in Figure 1. A block diagram of the measurement setup is reported in Figure 2. In order to reduce electro-magnetic interferences (EMI) during measurements, all devices and instrumentations were enclosed in a metal chamber. Moreover, in order to minimize the influence of low-frequency magnetic fields, mu-metal tape was used to completely cover the walls of the chamber. The instrumentation employed for measurements consists of a data acquisition card (National Instrument, model NI-6211 or simultaneously sampling NI-9215 in the case of cross-correlation measurements), a low-noise high input impedance amplifier (described in [34]), and a low-noise anti-aliasing filter (with a cutoff frequency of 20 kHz). Lead acid batteries ($V_{B1} = 6$ V; 5 Ah) were used to supply all devices and systems inside the chamber except the JFET drains, which were supplied by NiMH batteries. In the case of cross-correlation measurements, the low-noise amplifier was replaced by a two-channel low-noise amplifier. A dedicated software was developed to acquire signals and to calculate the voltage spectral density. The system software also allows one to monitor the charge state of all lead acid batteries in the measurement chamber. The connection between the PC and Low Noise (LN) source is made using and optically insulated link to reduce interferences. The Data Acquisition (DAQ) cards were connected to the PC using short cables and USB connectors placed at the chamber wall.
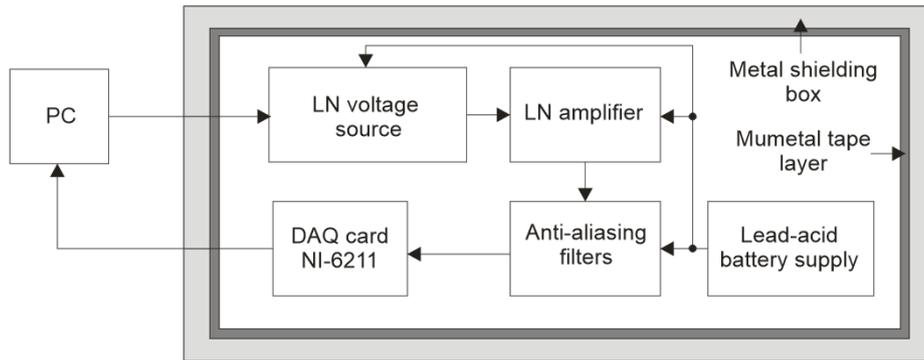
Figure 2. Block diagram of the measurement set-up.

3.2. Test Results

The results of noise characterization will be discussed with reference to the simplified equivalent circuit for noise analysis in Figure 3.
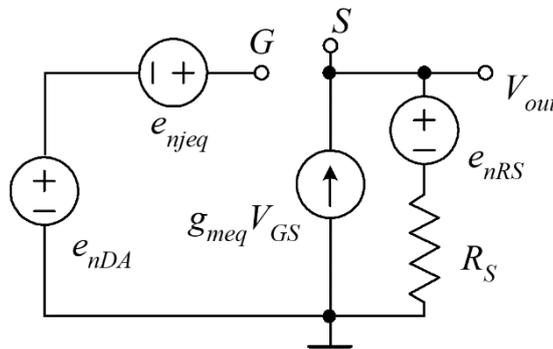

Figure 3. Equivalent circuit for noise calculation.

The noise source e_{nDA} represents the residual noise due to the Digital-to-Analog (DA) section after the filter R_2C_2; the noise sources e_{njeq} and g_{meq} are the equivalent input voltage noise and the equivalent trans-conductance of the parallel combination of the N JFETs at the output of the system in T_1, respectively; the noise source e_{nRS} represents the thermal noise of the resistance R_S. From Figure 3, the voltage noise e_{nout} at the output can be written as:

$$e_{nout} = \left(e_{nDA} + e_{njeq} + \frac{e_{nRS}}{g_{meq}R_S}\right)\frac{g_{meq}R_S}{1 + g_{meq}R_S} \tag{2}$$

As far as the value of g_{meq} is concerned, when N JFETs are parallelized as in Figure 1, we can obtain its estimate as a function of the overall drain current I_{DO} as follows:

$$I_{DO} = NI_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2; \ g_{meq} = \frac{dI_{DO}}{dV_{GS}} = Ng_{max}\sqrt{\frac{I_{DO}}{NI_{DSS}}} \ ; \ g_{max} = \frac{2I_{DSS}}{-V_P} \tag{3}$$

where I_{DSS} and V_P are the saturation current at $V_{GS} = 0$ and the pinch-off voltage of each single transistor, respectively. While, as it is very well known, the spread in the values of JFET parameters can be considerable, we can still refer to Equation (3) with the typical parameters from the datasheet for obtaining an estimate of the behavior of the devices used in this work. In particular, for the 2SK3557-6, we obtain $g_{max} = 35$ mA/V and $I_{DSS} = 12.25$ mA, while for the IF9030, we obtain $g_{max} = 150$ mA/V and $I_{DSS} = 100$ mA.

For testing, we concentrated our attention to voltages of 1 V or below, since the source we developed was primarily intended for performing noise measurement on an advanced superlattice Infrared (IR) photodetector, where the required bias voltages are typically below 1 V [8,10,13]. This is indeed the case also per the test experiments that will be presented in Section 4. As a first test, we measured the output noise for two different output voltage settings (50 mV and 1 V) and for two different values of the resistance R_S in Figure 1 (100 Ω and 1 kΩ) when four paralleled 2SK3557-6s were used for T_1 (noise measurements of this transistor can be found in [34]). The results of noise measurements in these cases are reported in Figure 4a,b for R_S = 100 Ω and R_S = 1 kΩ, respectively.
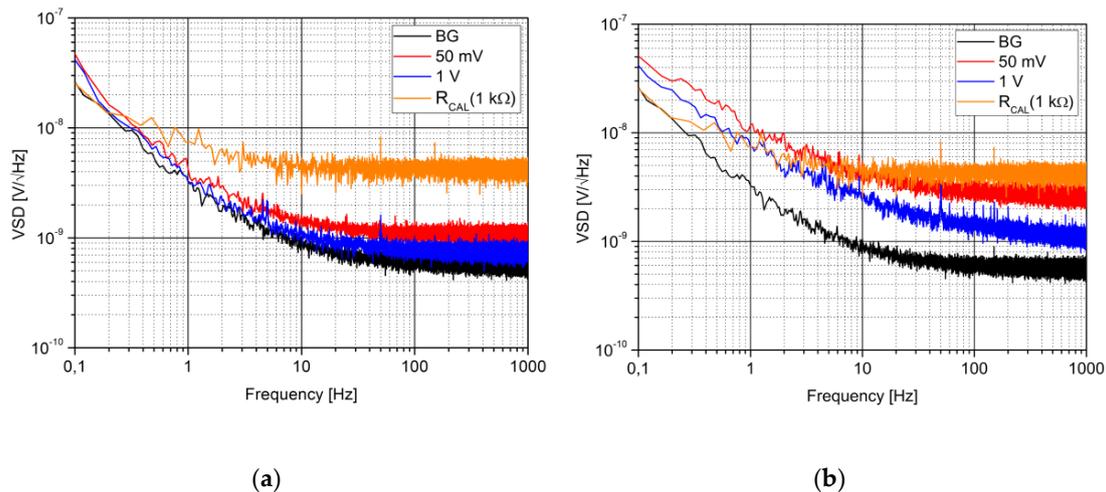

| (**a**) | (**b**) |

Figure 4. Voltage spectral density for two output voltages and four paralleled 2SK3557-6s used as an output JFET (Junction Field-Effect Transistor) buffer (T_1). The spectra with R_s = 100 Ω (**a**) and R_s = 1 kΩ (**b**) at the input of the amplifiers and the background noise (BG, input of the amplifier shorted) are also shown.

At higher frequencies (f > 100 Hz), because of the lowpass filters in the DA section, we can expect the contribution by e_{nDA} to be negligible. As far as the contribution of resistance is concerned, from Equations (2) and (3) it is clear that it depends on the value of the resistance and on the value of the bias current. In all explored cases, using Equations (2) and (3) it can be estimated that the contribution of the noise coming from the resistance R_S alone is a small fraction of the actual measured noise, thus leading to the conclusion that the noise above 100 Hz is essentially coincident with that introduced by the JFETs. For instance, in the case R_S = 1 kΩ, V_{out} = 50 mV, the noise at the output due to the resistance R_S alone can be estimated to be about 0.74 nV/√Hz, while the measured value in Figure 4b is about 3 nV/√Hz at 100 Hz. Moreover, we notice, as expected [35], that it consistently reduces as the bias current increases. As far as the lower frequency portion of the spectra is concerned, we observed that in the case of Figure 4a (R_S = 100 Ω), the noise is barely distinguishable from the background noise introduced by the measurement amplifier. In the case of Figure 4b, we can clearly distinguish the noise of the voltage source since it is well above the background noise of the measurement amplifier down to 0.001 Hz. It is important to observe that in the case of Figure 4b, we can conclude that the noise, in the low-frequency region, is mainly due to the JFET. In fact, if a significant contribution from e_{nDA} was present, it should also show in Figure 4a since the DA operates in almost the same condition for the same output voltage (small differences are only due to small differences in the V_{GS} required in the cases of R_S = 100 Ω and R_S = 1 kΩ). Since the noise introduced by the JFETs appears to be the most relevant source of noise, it is conceivable that by using JFETs characterized by better noise performances, we can obtain even lower levels of output noise. In order to test this hypothesis, we replaced the parallel combination of four 2SK3557-6s with the parallel combination of two ultra-low-noise JFET IF9030s (InterFET). These transistors are characterized by a *VSD* of about 1.5 nV/Hz, 0.6 nV/Hz and

0.5 nV/Hz for frequencies of 1 Hz, 10, and above 100 Hz, respectively [36]. In order to perform a meaningful comparison between two solutions in the case of $R_S = 100\ \Omega$ (that is, the case in which we obtain the lowest level of noise), it is mandatory to reduce the background noise of the voltage amplifier used for the measurement, otherwise, as can be seen in Figure 4a, we cannot obtain a correct estimation of the actual noise produced by the voltage source. In order to obtain a background noise below that introduced by the voltage preamplifier, we resorted to a cross-correlation approach. In this approach, two identical JFET input and low-noise voltage preamplifiers are employed. The voltage sources associated with each amplifier are uncorrelated to one another and their contribution to the final estimate of the noise to be measured can be reduced by proper averaging of the cross-spectrum between the two amplifying channels [37–39]. In our set-up, the gain of each channel was 80 dB and the equivalent input *VSD* of each amplifier was about 5 nV/$\sqrt{\text{Hz}}$, 1 nV$\sqrt{\text{Hz}}$ and 0.6 nV/$\sqrt{\text{Hz}}$ at 1 Hz, 10 Hz and above 100 Hz, respectively.

The results of noise measurements when using the cross-correlation approach in the same conditions as in Figure 4a ($R_S = 100\ \Omega$, $V_{out} = 50$ mV and 1 V) are reported in Figure 5a; the results obtained in the case in which the four 2SK3557-6s are replaced by two IF9030s in parallel are reported in Figure 5b.
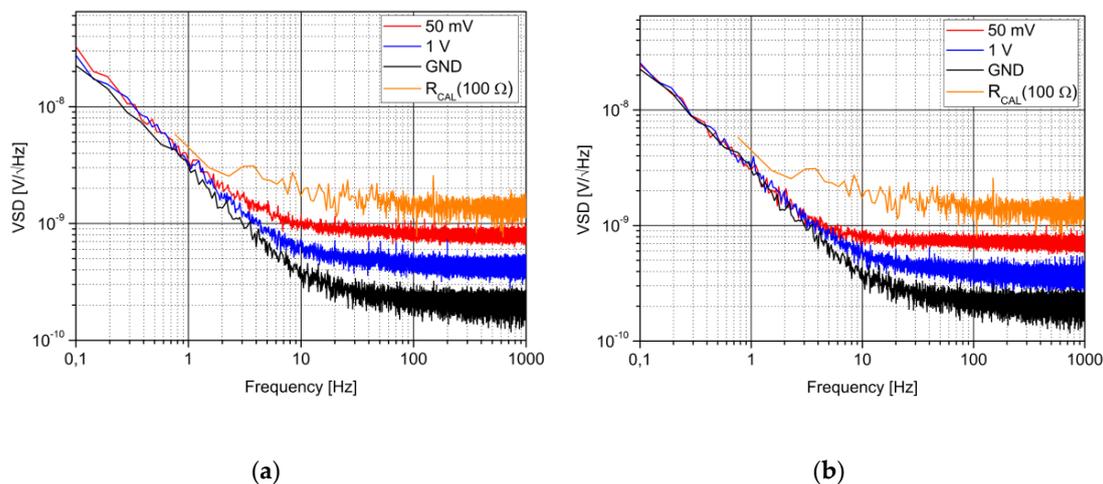

(**a**)　　　　　　　　　　　　　　　　　　　　　　　　(**b**)

Figure 5. Voltage spectral density for four paralleled 2SK3557-6s (**a**) and two paralleled IF9030s (**b**) as a T_1 in Figure 3 with $R_s = 100\ \Omega$. Measurements with the inputs of the amplifiers shorted ("GND") and with a 100 Ω resistor as a device-under-test (DUT), obtained with the very same measurement setting, are also shown for reference.

For a better comparison among the performances in the two cases, the values of the voltage noise recorded at 1 Hz, 10 Hz and 100 Hz are reported in Table 2. To test measurement set-up, in the first step, the VSDs of known "calibration resistors" R_{CAL} were extracted. For measurements with Ultra-Low Noise Amplifier (ULNA) and cross-correlation, 1 kΩ and 100 Ω were used respectively as a R_{CAL}. The obtained spectra correspond to thermal noise of the used resistors. In the case of cross-correlation, the shown spectra (Figure 5a,b) are characterized by lower resolution due to a shorter time of measurements (shorter data vector).

Table 2. Noise performances of the constructed low-noise voltage source.

	Transistor 2SK3557-6		Transistor IF9030	
	Vout = 50 mV	Vout = 1 V	Vout = 50 mV	Vout = 1 V
VSD at 1Hz	3 nV/Hz	3 nV/Hz	3 nV/Hz	3 nV/Hz
VSD at 10Hz	1 nV/Hz	0.7 nV/Hz	0.8 nV/Hz	0.6 nV/Hz
VSD at 100Hz	0.8 nV/Hz	0.5 nV/Hz	0.7 nV/Hz	0.4 nV/Hz

As expected, the configuration with two parallelized IF9030 JFETs results in less noise for the same output voltage ($R_S = 100\ \Omega$ in both cases). The results of cross-correlation noise measurements also show that below 1 Hz the voltage noise appears to be independent on the bias point and on the nature of the output transistors, thus suggesting that in this region it is the residual noise from the DA converter that sets the ultimate noise performances. Moreover, in this region some correlated components coming from measurement setup might also appear. With $V_{B2} = 6.4$ V, the maximum voltage that can be obtained at the output with $R_S = 100\ \Omega$ is 3.3 V (the DAC was programmed to ±3 V range to operate with lowest possible voltage noise at its output [33]).

While reaching excellent noise performances was the main goal of this work, in measurement applications the stability of the output voltage is also a key parameter. To test for stability, in the configuration with the 2SK3557-6, we set an output voltage of 1 V and after waiting for the stabilization of the system, we monitored the output voltage for three hours in the conditions used for noise measurements (Figure 6). The voltage was monitored by a KEITHLEY 2002 multimeter (measurement range: 2 V; measurement resolution: 10 nV). Over a period of three hours, the voltage remained within ±25 µV of the set voltage (1 V). During the test, the external temperature was monitored and remained within ±0.1 °C of the initial value. While the measured stability can be regarded as sufficient for many applications, better temperature stabilization and larger capacity batteries (to avoid excessive discharge in a given time) can be used to improve stability of the output voltage.
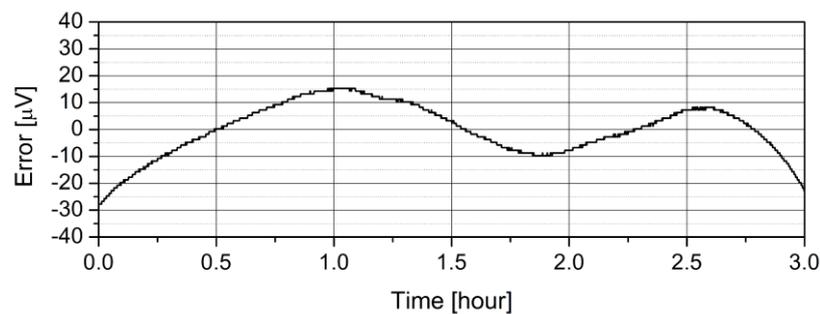

Figure 6. Voltage error vs. time in stabilized state of voltage source with the 2SK3557-6 JFET follower.

4. Noise Performances Comparison with Solid-State Voltage Sources

To better appreciate the noise performances of the proposed voltage source, we can compare it to what can be obtained by resorting to a commercial solid-state very low-noise linear regulator.

For this purpose, we resorted to the low drop out (LDO) regulator model LT3045 that was chosen as the one with the lowest reported level of output noise. Its output voltage can be set using a single resistor R_{SET}, as in Figure 7. This regulator is characterized by s voltage noise of 0.8 μV_{RMS} in the frequency range from 10 Hz to 100 kHz and a noise density of about 2 nV/$\sqrt{Hz}$ (10 kHz). In order to obtain a lower noise level and a higher output current, a few LT3045 regulators can be paralleled. In this regulator, the output noise voltage mainly depends on the capacity of C_{SET}. This capacitor shunts the thermal noise generated in resistor R_{SET} and filters out the noise from the internal current source. The circuit in Figure 7 used for testing was built according to the manufacturer application notes. For the capacity of C_{SET}, two paralleled ceramic capacitor X5Rs were used, providing a larger capacity than the one reported in the datasheet. The regulator was supplied using a lead acid battery for V_{IN} in Figure 7.

The measured *VSD* at the output of the circuit in Figure 7 is reported in Figure 8 for $V_{out} = 50$ mV and $V_{out} = 1$ V. A 1 kΩ wire-wound resistor was used as a load.
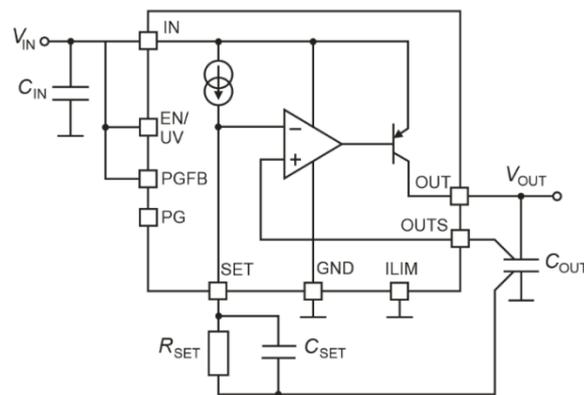
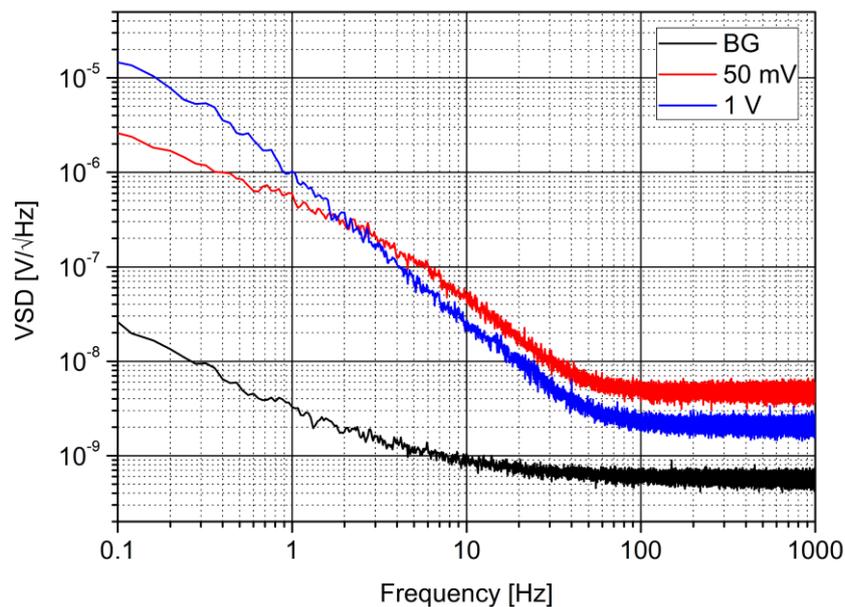**Figure 7.** Voltage source with linear regulator LT3045 [40].

Figure 8. *VSD* characteristics of the voltage source in Figure 7 for different output voltages (red and blue lines) and noise background (black line).

The results are comparable with the ones reported in the catalogue. It is clear, especially in the low frequency region (below 100 Hz), that the level of noise that can be obtained with our proposed design is much lower than what can be obtained with a circuit based on a low-noise solid-state regulator. On the other hand, the circuit in Figure 7 is extremely simple, and the level of noise obtained at the output is comparable to the ones than can be obtained by resorting to commercial programmable voltage sources. There are cases, however, when the availability of a very low-noise voltage source (LNVS) such as the one we propose is essential in order to obtain correct results in the characterization of electron devices. As an example, we employed both the LNVS and a source based on the LT3045 for the characterization of the noise in a type II superlattice photodetector (T2SL) [41]. The measurement setup for noise measurements is reported in Figure 9.
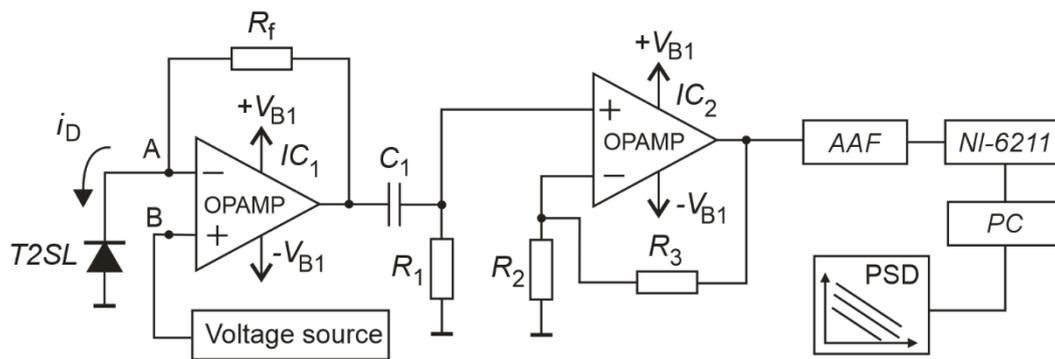
Figure 9. Schematic diagram of the Power Spectrum Density (PSD) measurements setup.

The setup in Figure 9 includes a low-noise trans-resistance amplifier (*IC*1) where the "voltage source" block is used to bias the device under test (DUT), the AC coupling filter (*C1R1*) and a low-noise voltage amplifier (*IC*2) followed by the acquisition and elaboration blocks in order to perform spectral estimation. The results of noise measurements for different bias voltage values when the LNVS and the LT3045-based source are used for biasing the T2SL are reported in Figure 10.
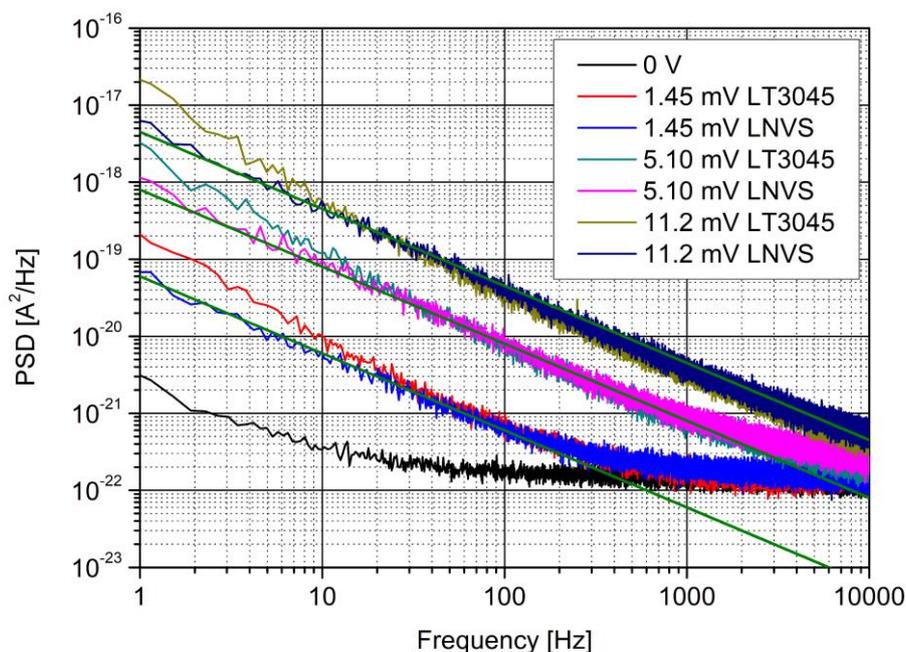

Figure 10. Current noise measurement results of the photodetector with a bias network using different voltage sources.

The curve labeled 0 V was obtained with node B grounded and represents the noise of the photodetector and the background noise of the system, excluding the noise coming from the voltage source. As it can be noticed, when the LNVS (with 2SK3557-6 JFETs at the output) is used for biasing the T2SL, pure flicker noise is obtained when the noise is large enough to rise above the background noise. When the voltage source based on LT3045 is used, instead, we can clearly notice the deviation in the measured noise due to the large noise introduced by the source in the frequency ranges below 10 Hz. It is clear that, without resorting to a very low-noise voltage source as the one we have developed, the interpretation of the measurement results would be much more difficult because of the significant influence of the noise introduced by the bias system.

5. Conclusions

In this paper the design, realization and testing of a low-noise programmable voltage source have been presented. The source is characterized by excellent noise performances when compared with other realizations presented in the literature. In the experimented system configuration, the output voltage can be set in the range from 0 to 3.3 V and a VSD as low as 3 nV/$\sqrt{Hz}$ (1 Hz), 0.6 nV/$\sqrt{Hz}$ (10 Hz) and 0.4 nV/$\sqrt{Hz}$ (100 Hz) when stetting the output voltage to 1 V is observed. Comparing the obtained results with earlier published low-noise voltage sources, better results were obtained, especially at frequencies above a few Hz.

The limitation in the maximum output voltage is a direct consequence of the fact that the supply voltage of the JFET-based output stage must ensure that the gate leakage current remains very small, as the leakage current depends on the drain-to-gate voltage difference. However, it is conceivable that, in future development, the possibility of changing the drain supply voltage can be changed as a function of the voltage range to be generated, thus extending the output range.

While the residual noise at frequencies above 10 Hz appears to be set by the type and number of JFETs used in the output buffer stage, the noise in the lower portion of the spectrum appears to be set by the DA section in the device. Future work will be devoted to improving the noise performances of the DA section.

The results of noise measurements on advanced devices have been used to prove the advantages that can be obtained with a very low-noise programmable voltage reference.

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