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DOCTORAL THESIS

Defects and traps electrical characterization in 4H-SiC PowerMOSFET

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INDEX

Introduction

Wide band gap materials, their unique properties, and applications

In power electronics, Silicon (Si) has been adopted as the mainstream technology over the last four decades; today, silicon power transistors and diodes are so widespread and pervasive that equipment based on this material is closely intertwined with our everyday lives. This adoption has allowed silicon to enjoy continuous technology and process improvements, supported by innovative packaging and interconnect technologies, that have enhanced thermal management and reduced parasitic effects for higher frequency operation.

By virtue of this unrelenting quest for improvement, silicon technology is about to [1] approach the theoretical limits of the Si material itself; however, power device requirements for many applications are at a point that the present Si-based power devices cannot handle.

In addition, the International Energy Agency (IEA) [2] has estimated that the demand for world energy consumption has doubled in the last decade, so new semiconductor devices such as silicon are needed for more efficient use of electricity and enabling the reduction of global environmental pollution and the conservation of fossil residues.

Based on the data reported in the latest IEA report on renewables "Renewables 2020 - Analysis and forecast to 2025" In 2020 renewable energies represented almost 90% of the increase in total energy capacity worldwide and in 2021 they will accelerate up to achieve the fastest growth in the past 6 years.

Moreover, 2020 was a record year for companies engaged in semiconductor manufacturing, according to the analysis published by TrendForce [3]. Preliminary estimates speak of a growth of 23.7% compared to the previous year, for a total value of 84.6 billion dollars.

The global pandemic has led to these results, with the market leading to higher than expected demand for technological products and all producers trying to keep up with consumer demands by also preparing for the additional demand expected for 2021.

Power electronics design has taken an interesting turn toward the adoption of wide-bandgap (WBG) devices such as gallium nitride (GaN) and silicon carbide (SiC). While silicon still dominates the market, the emergence of GaN and SiC devices will soon direct technology toward new, more efficient power solutions. Yole Développement estimates [4] that revenue from SiC devices will account, as shown in Fig.1.1 for more than 10% of the market by 2025, while revenue from GaN devices will claim more than 2% of the market by 2025.

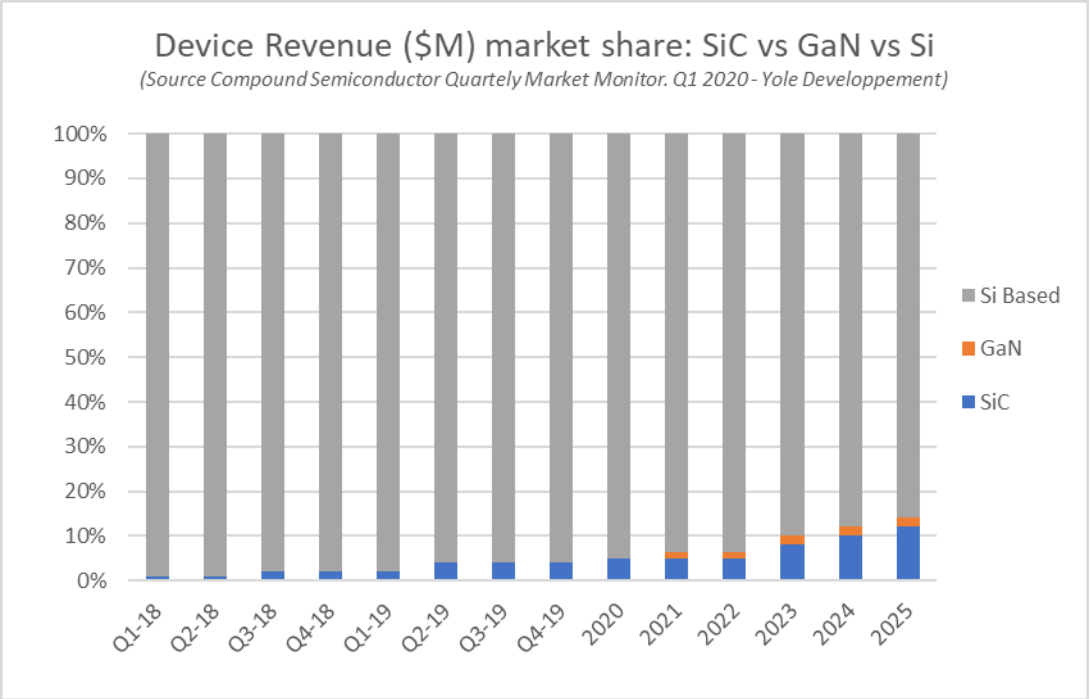

Fig. 1.1: SiC, GaN, Si Market share forecast until 2025

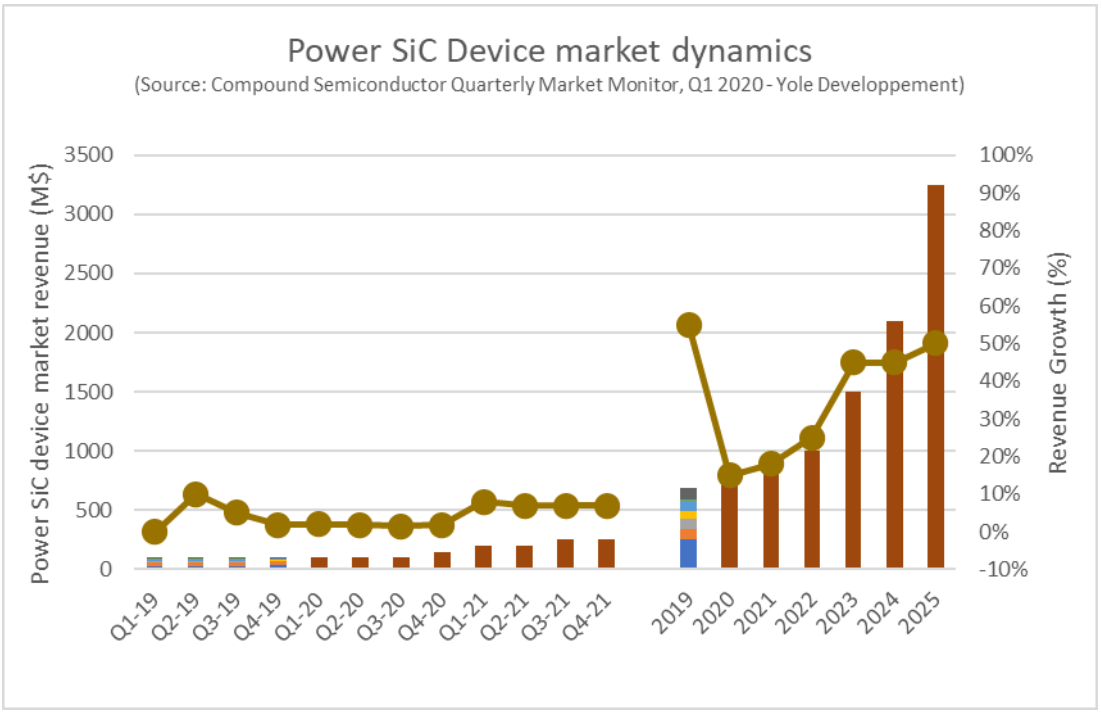

Fig.1.2: Power SiC Device market dynamics

Another reason on the increasing demanding for semiconductor devices over the past decade is due to the various changes in the auto industry that have drawn more attention to electric and hybrid vehicles. It was mainly driven by the Increasing oil prices and worries about a diminishing oil supply are creating a need for alternatives to traditional gasoline and diesel

engines. Consequently, more and more companies in the transportation industry are introducing electric or hybrid electric vehicles. In addition, the military is ready for allelectric warships and more-electric fighter planes.

Furthermore, the present silicon (Si) technology is reaching the material's theoretical limits and cannot meet all the requirements of the transportation industry.

The requirements include higher blocking voltages, switching frequencies, efficiency, and reliability. To overcome these limitations, new semiconductor materials for power device applications are needed. For high power requirements, widebandgap semiconductors like silicon carbide (SiC), gallium nitride (GaN), and diamond, with their superior electrical properties, are likely candidates to replace Si in the near future [5].

Wide bandgap (WBG) semiconductor materials [6] allow power electronic components to be smaller, faster, more reliable, and more efficient than their silicon (Si)-based counterparts. These capabilities make it possible to reduce weight, volume, and life-cycle costs in a wide range of power applications. Harnessing these capabilities can lead to dramatic energy savings in industrial processing and consumer appliances, accelerate widespread use of electric vehicles and fuel cells, and help integrate renewable energy onto the electric grid.

WBG semiconductors permit devices to operate at much higher temperatures, voltages, and frequencies—making the power electronic modules using these materials significantly more powerful and energy efficient than those made from conventional technologies.

WBG materials also emit light in the visible color range, an optical property useful for applications in solid-state lighting. Gallium nitride (GaN), for example, is an enabling material behind the ultra-high efficiency of light emitting diodes (LEDs) and laser.

WBG semiconductors are expected to pave the way for exciting innovations in power electronics, solid-state lighting, and other diverse applications across multiple industrial and clean energy sectors. Realizing the energy-saving potential of WBG semiconductors will require the development of cutting-edge manufacturing processes that can produce high-quality WBG materials, devices, and modules at an affordable cost. Investing in this innovative technology will help U.S. and European industry maintain a competitive edge. Other significant advantages are the following:

• WBG semiconductor-based unipolar devices are thinner and have lower on-resistances. Lower Ron also means lower conduction losses; therefore, higher overall converter efficiency is attainable.

• WBG semiconductor-based power devices have higher breakdown voltages because of their higher electric breakdown field; thus, while Si Schottky diodes are commercially available typically at voltages lower than 300 V, the first commercial SiC Schottky diodes are already rated at 600 V.

• WBG devices have a higher thermal conductivity (4.9 W/cm-K for SiC and 22 W/cm-K for diamond, as opposed to 1.5 W/cm-K for Si). Therefore, WBG-based power devices have a lower junction-tocase thermal resistance, Rth-jc. This means heat is more easily transferred out of the device, and thus the working device temperature is lower. GaN is an exception in this case.

• WBG semiconductor-based power devices can operate at higher temperatures comparing with silicon. The literature notes operation of SiC devices up to 600°C. Si devices, on the other hand, can operate at a maximum junction temperature of only 150°C.

• Forward and reverse characteristics of WBG semiconductor-based power devices vary only slightly with temperature and time; therefore, they are more reliable.

• WBG semiconductor-based bipolar devices have excellent reverse recovery characteristics. With less reverse recovery current, switching losses and electromagnetic interference (EMI) are reduced, and there is less or no need for snubbers. As a result, there is no need to use soft-switching techniques to reduce switching losses. GaN is an exception in this case.

• Because of low switching losses, WBG semiconductor-based devices can operate at higher frequencies (>20 kHz) not possible with Si-based devices in power levels of more than a few tens of kilowatts. [2]

WBG semiconductors are expected to pave the way for exciting innovations in power electronics, solid-state lighting, and other diverse applications across multiple industrial and clean energy sectors. Fig 1.3 and 1.4 show several applications where WBG materials are going to replace Silicon technology.

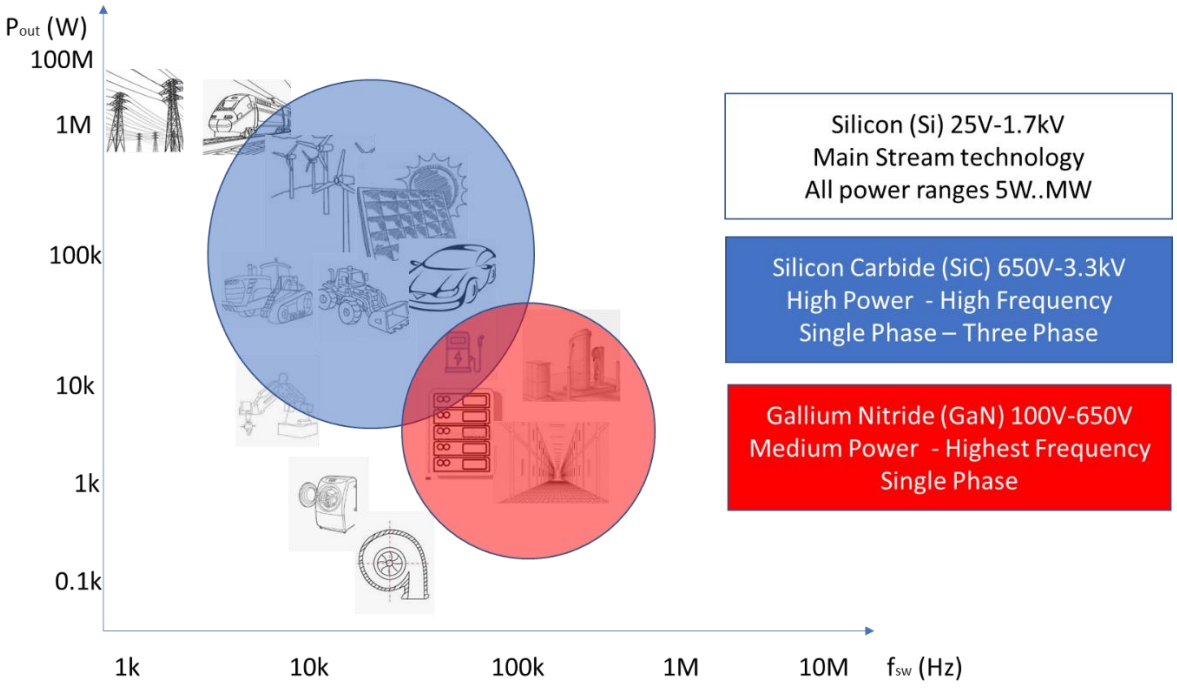

Fig. 1.3: Power and Frequency applications for WBG Materials

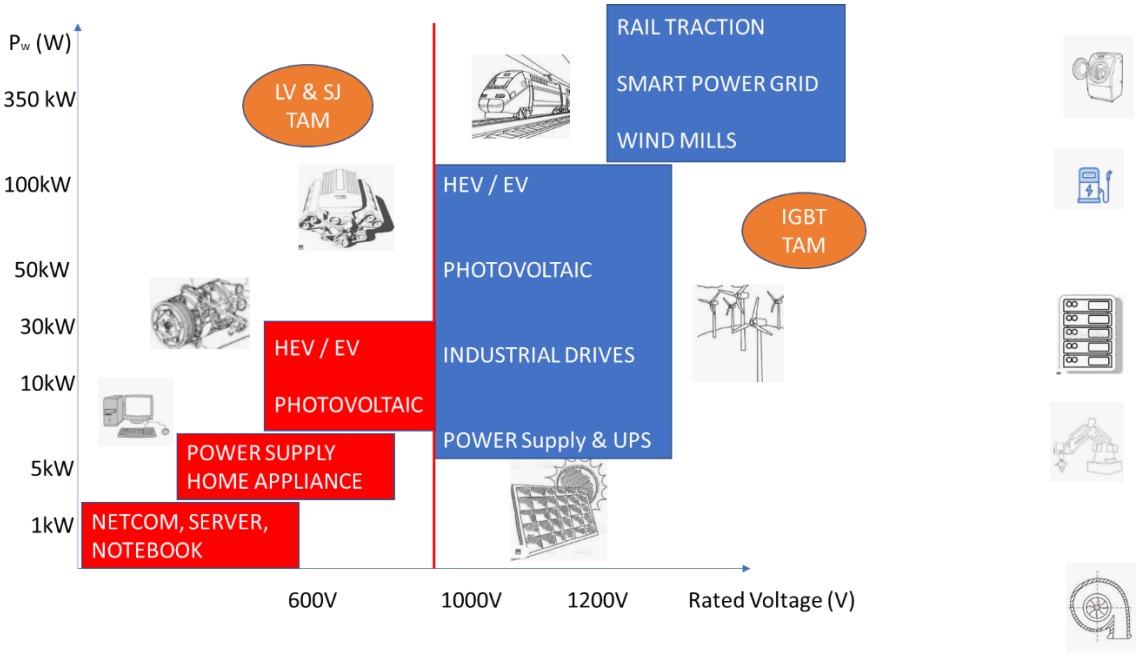

Fig. 1.4: Power and Related Voltages for WBG Materials (GaN in red and SiC in blue)

Realizing the energy-saving potential of WBG semiconductors will require the development of cutting-edge manufacturing processes that can produce high-quality WBG materials, devices, and modules at an affordable cost.

Diamond offers an exceptionally large band gap and unique thermal properties, but the research remains in the very early stages. SiC posseses high thermal conductivity and wide band gap that makes it ideal for generation of power switching devices. GaN offers a direct band gap and high frequency performance; because of which it finds great applications in optoelectronics and RF devices.

Various parameters of several semiconductor materials are shown in Table 1, where wide bandgap semiconductors clearly have advantages over Si. Amongst all the semiconductors, Diamond has also the widest band width. Consequently, it also has the highest electric breakdown field. The performance of GaN is approximately similar to SiC but on the basis of certain characteristics, SiC is generally preferred over GaN

As mentioned before and shown in table 1, the most important characteristics of a WBG device are [7]:

- **Drift region width** which reduces due to high electric breakdown field and higher doping density.
- **Lower On Resistance** which results in lower conduction losses therefore higher overall converter efficiency is attainable. On resistance of SiC polytypes and GaN devices is approximately 10 times less than that of Si devices.
- High saturated **drift velocity** which is directly proportional to high frequency switching capabilities and therefore the power devices based on WBG can be switched at higher frequencies.
- **Thermal conductivity** which, in WBG devices, is higher. The high thermal conductivity of SiC allows more efficient heat transfer from heat sink and yields a lower junction temperature.
- **Coefficient of Thermal Expansion** (CTE) which is a fractional change in length (or sometimes in volume when specified) of a material for a unit change in temperature. Semiconductor materials that have a closer CTE match to available electrically insulating ceramics can more easily be adapted for high power and wider temperature excurstion applications. The CTE for Diamond is 0.8 ppm/K which is very low as compared to typical package material CTE's.

Property	Si	6H-SiC	4H-SiC	GaN	Diamond
Bandgap Eg (eV)	1.1	3.03	3.26	3.45	5.45
Dielectric Constant, ε_r	11.9	9.66	10.1	9	5.5
Breakdown Field, E_c (kV/cm)	300	2500	2200	2000	10000
Electron mobility, μ_n (cm^2/Vs)	1500	500	1000	1250	2200
Hole mobility, μ_p ($cm^2/V\ s$)	600	101	115	850	850
Thermal Conductivity, λ (W/cm K)	1.5	4.9	4.9	1.3	22
Thermal Expansion ($x\ 10^{-6}$)/°K	2.6	3.8	4.2	5.6	1-2
Saturated E-Drift Velocity Vsat ($x10^7$ cm/s)	1	2	2	2.2	2.7

Table 1: Si, SiC, GaN and Diamond main characteristics

This thesis work focuses on the use of Silicon Carbide (SiC) devices in power electronics which has been proposed since the 60s, its wide band-gap and other features offering the prospect of high efficiency operation. However, some difficulties in manufacturing substrates for SiC wafers have delayed the development of SiC power devices. The main challenge stymying their adoption has been the cost of SiC wafers and SiC manufacturing problems of larger wafer diameter with low defect densities and high yield. The recent supply of good-quality SiC wafer substrates offered by different suppliers has helped to circumvent these issue.

In this frame, the attention paid to the understanding of the nature and origin of the defects and of the effects on the performances of the device at a reliability level becomes crucial to bridge the qualitative gap with the now consolidated Silicon-based devices. This work is therefore aimed at the study of the electrical analysis of extended and point defects and of the different methods of characterization of the same.

In Chapter I, we will talk about the properties of Silicon Carbide, the protagonist of our research.

In Chapter II, we will discuss silicon carbide related defects and defects in general and how these can affect the characteristics of SiC devices. In this chapter we will talk about "deep levels" and "shallow levels" which is the main classification of defects in SiC. In particular we will discuss about defects in SiC such as "stacking fault" and "micropipe" and how these impact the reliability of SiC devices.

In Chapter III we will talk about the methods used to investigate defects and the energy levels associated with them. In this chapter, we will talk about electrical defect characterization. Different measurement methods will be presented to characterize the so-called "fixed charges" in gate oxide and "interface charges" in SiO_2/SiC. These methods are effective both to be able to identify these charges, which are nothing more than defects in the material, such as the Capacitance-Voltage (CV) and conductance (GV) techniques, and to be able to qualify SiC devices in terms of reliability, for example Time Dependent Dielectric Breakdown (TDDB) test

In Chapter IV, we will talk about the results obtained through measurement techniques described in Chapter III.

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CHAPTER 1

Silicon Carbide properties

1.1 Silicon Carbide structure

Silicon carbide is a semiconductor consisting of [1] silicon and carbon atoms. One C atom is bound to four neighboring Si atoms, which are placed in the corners of a tetrahedron. Vice versa is the Si atom bound similarly to four C atoms. The Si-C bond is very strong due to its short bond length (1.89 Å) and its sp_3 hybridization; it has a nearly covalent character. However, slightly different electronegativity values for C and Si (EN(C) = 2.55 and EN(Si) = 1.9 after PAULING) imply a small ionic contribution (≈10%) to the SiC bond [2]. The stacking of the double layers, composed of one Si and one C layer, reaches a close packed structure, if the subsequent layer (B) is shifted with regards to the first layer (A), see Fig. 1.

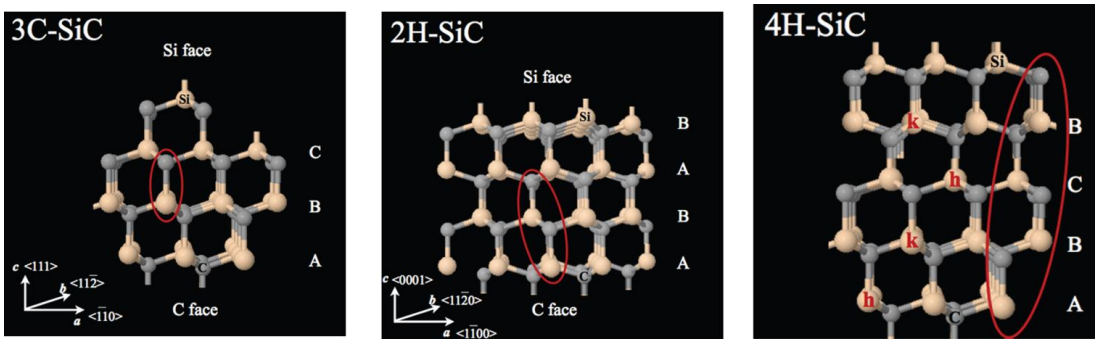

Fig. 1: Structure of some SiC polytypes. The view is from a direction perpendicular to the h111i direction of the cubic lattice, or the c-axis of the hexagonal lattices. Atoms in the primitive cells are circled in red. note the lack of inversion symmetry. The stacking sequence is displayed at right in Zdanov notation for all structures. Another convenient way of classifying polytypes labels each SiC bilayer according to its hexagonal (h) or cubic (k) character. The 3C and 2H polytypes are purely cubic and haxagonal, respectively. Note that the 4H polytype has 50% hexagonality [3].

The following layer can take position A again or a new one, C. The combination of the three possible positions results in hundreds of different theoretically possible sequences. In this thesis, the presented work is restricted to the most common ones (ABC), (ABCB) and (ABCACB). From the different stacking sequences in one direction (c-axis), different crystal modifications, labeled polytypes for SiC [4], are possible. The phenomenon of a material to exist in more than one crystal structure is known as polymorphism; for SiC the polymorphism is restricted to one dimension [5]. A common notation of all the polytypes composed of a number and a letter, was introduced by L. S. Ramsdell [2] in 1947. The number stands for a

amount of double layers in the unit cell and the letter represents structural information; C - cubic, H - hexagonal and R - rhombohedral. All lattice sites are equivalent in case of 3C-SiC, meaning that the local environment of each tetrahedron is purely cubic, labeled k after the Jagodzinski notation [2]. With its zincblende structure, the lattice parameter of 3C-SiC (a = 4.3596 Å) is determined by the edge of the cube. 2HSiC, which is very difficult to synthesize as stand-alone crystals [6], has a wurtzite structure and all lattice sites have a pure hexagonal environment, labeled h. All the other polytypes have both lattice sites with a quasi-cubic environment and lattice sites with a local hexagonal environment. In case of a hexagonal structure (4H- and 6H-SiC), the lattice parameter corresponds to the edge of the basal plane. The hexagonal site implies a twist (180 k and one h), 33 % in 6H (k1, k2 and h) and 0 % in 3C-SiC. Along with hexagonality, physical properties of the polytypes change, such as the size of the band gap. Goldberg et al. [2] determined following band gaps at room temperature, as shown in Table 1:

SiC Structure	**Energy gap**
4H-SiC	3.23 eV
6H-SiC	3.08 eV
3C-SiC	2.36 eV

Table 1: Energy gap of SiC structure

Choyke and co-authors [7] found an empirical relation between the size of the band gap, Eg, of different SiC polytypes and the fraction of hexagonality. Eg increases for polytypes with high amount of quasi hexagonal lattice sites. However, the measured band gap of 2H-SiC (Eg(2H-SiC) = 3.33 eV) should be even larger if following this relation.

Backes etal.[8] tried to theoretically explain this relation by a one-dimensional Kronig-Penney-like model.

The inequivalent sites can be resolved by photoluminescence measurements due to different ionization energies related to emissions from donors or acceptors residing on different sites [9]. It is much more difficult to detect defects located at different lattice sites by electrical measurements, such as conventional DLTS, where the energy resolution is only about 10 MeV.

1.2 Silicon Carbide Properties

The band structure of a semiconductor such as SiC depends on the considered polytype, as each polytype have a different spatial arrangement of the atoms. From the study of the band structure, it is possible to know [1].

• the value of the band gap

• the relative positions of the maximum of the valence band and of the minimum of the conduction band in the wave vector space, which leads to the distinction between direct and indirect gap semiconductors;

• the density of the states in the maximum of the valence band and in the minimum of the conduction band that determines the behavior of the Fermi level of the material.

The radar diagram (Fig. 2) graphically represents the physical properties of the three power devices described in Table 1 in the Introduction section [10]:

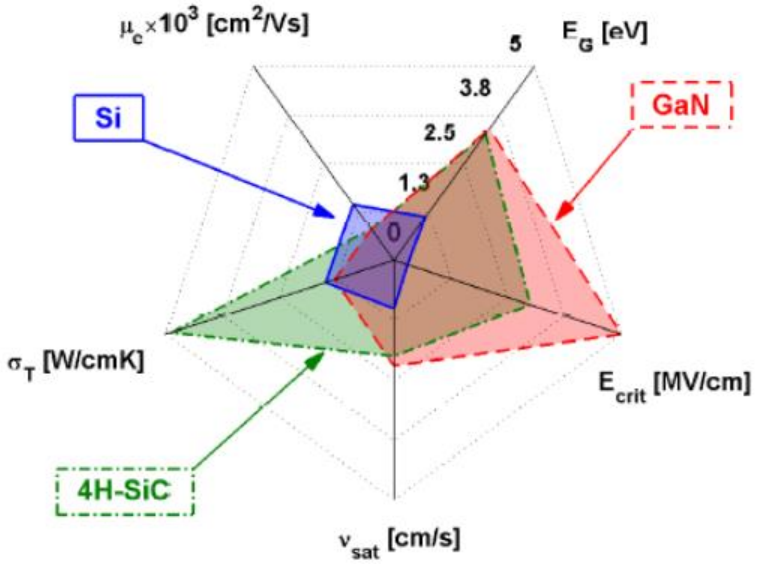

Fig. 2: The radar diagram graphically represents the physical properties of the three power devices [10].

Critical (or breakdown) electric field

The critical electric field is the maximum electric field applied to the junction before it causes the avalanche multiplication phenomenon, whereby the current passes through the device in an uncontrollable way, causing it to break. SiC has a large bandgap and is therefore able to withstand higher electric fields than Silicon. The breakdown field can be expressed in terms of applied voltage as follows [1].

$$V_B = \frac{E_{cr}^2}{2qN_d}\varepsilon_r\varepsilon_0$$

where N_d is the n-type doping performed, q is the charge of the electron, $\varepsilon = \varepsilon_r\varepsilon_0$ is the dielectric constant of the vacuum for the relative constant of the semiconductor used to make the diode, Ecr is the critical field, i.e. the maximum value of the electric field applicable to a junction of a given material [1].

Mobility of charge carriers

In SiC the mobility of electrons is much greater than that which characterizes holes and for this reason it is more convenient to make the active regions of the components with an n-type rather than a p-type doping. However, the values of this parameter are not constant, but show a strong dependence on the doping profile adopted and on the temperature at which the device is operating (similarly to what happens in Si) [1]. In particular, the mobility decreases as the concentration of the dopant species increases and this situation is essentially due to the increase in the scattering of the charge carriers by the donor atoms or ionized acceptors. Similarly, this parameter decreases with increasing temperature due to the greater scattering of phonons. The following two Fig.s depict the trend (experimentally traced) of the mobility of electrons for both 4H-SiC and Silicon, respectively as a function of doping and temperature [1].

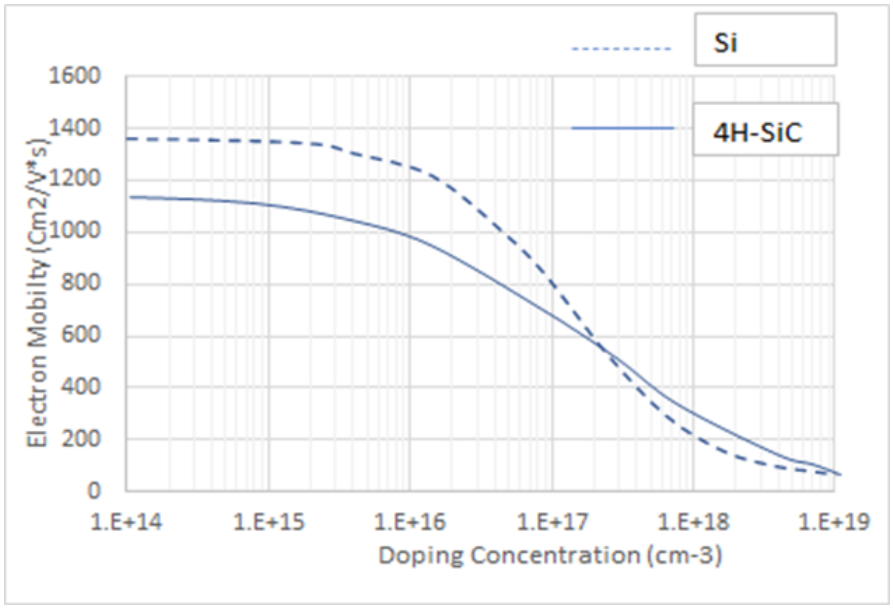

Fig. 3: Mobility of electrons as a function of the doping of the epilayer for Si and 4H-SiC [1]

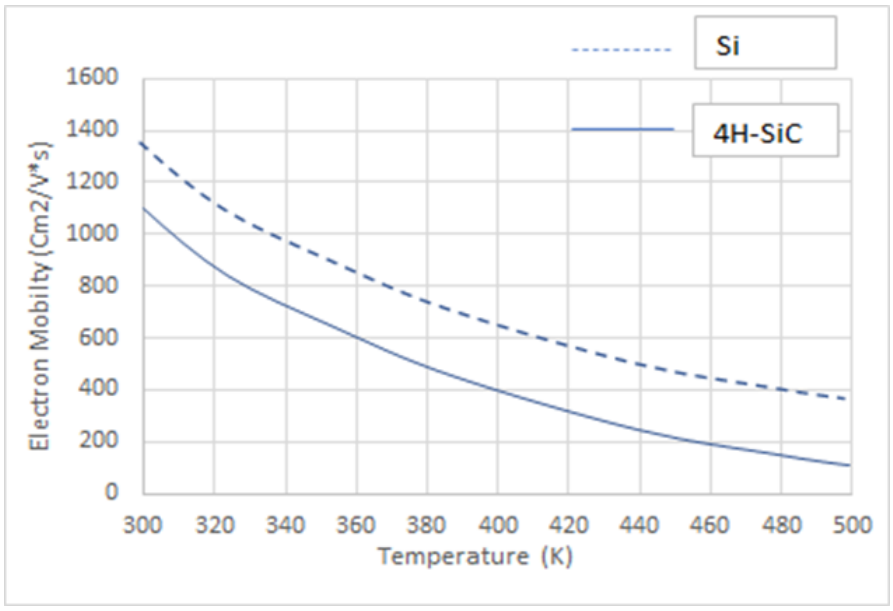

Fig. 4: Mobility of electrons as a function of temperature for Si and 4H-SiC [1]

The above graphs have been plotted up to 500 K, which is a reasonable temperature for operation since at this temperature the ohmic contacts begin to degrade [1].

Carrier saturation velocity

The possibility of using semiconductor material in high-frequency application is closely linked to the drift speed of the electrons. The higher this speed, the greater the possibility of exploiting the semiconductor to make devices with a high switching frequency, since the charge present in the depletion region of a diode can be removed more quickly. It is well known that the saturation speed of electrons in SiC polytypes 4H and 6H doubles the ones in Silicon ($1x10^7$cm / sec) [1].

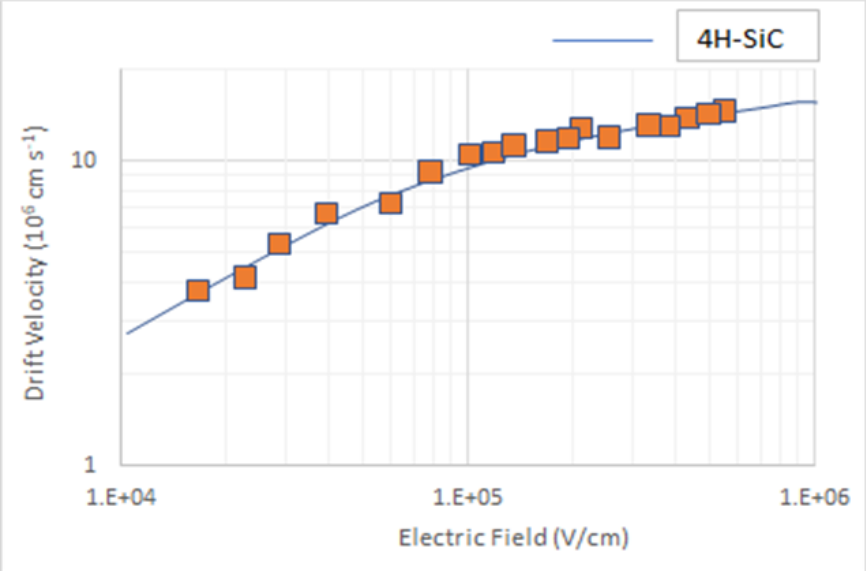

Fig. 5: Speed of drift in 4H-SiC as a function of the applied electric field. [11]

The switching frequency for power devices in Si is limited to 20 kHz for power levels of over a few tens of kW, while in SiC it is possible to reach frequencies of about 100 kHz [8].

Thermal conductivity

Silicon carbide has a high thermal conductivity, about 2-5 times that of Silicon (6H-SiC in particular has 3-5 W / cm · K). This greatly help the heat dissipation, as thermal resistance is defined as

$$R_{th-jc} = \frac{d}{\lambda A}$$

where λ is the thermal conductivity, d is the thickness of the device and A is the section. Therefore, the thermal resistance is lower than that of Silicon, and this allows greater heat transfer from the junction to the case, then towards the heat sinks, and finally towards the external environment [1]. In addition, SiC also has the highest thermal conductivity of any semiconductor at room temperature, with the effect that it is much easier to cool the device,

eliminating the need for a large cooling system. Although SiC devices will be more expensive to manufacture than Si devices, the significant savings on passive components and cooling system will make the devices very attractive for a large customer base [1].

Intrinsic concentration

One of the fundamental characteristics of SiC is the intrinsic low concentration of carriers, n_i, which is the result of the compensation of two mechanisms.

- Generation of electron-hole pairs, the faster the higher the temperature and the thermal energy supplied by the crystal to activate the process of jumping an electron from the valence band to the conduction band;
- Recombination of electron-hole pairs, the more likely the greater the number of conduction electrons and holes.

The intrinsic concentration is linked to the width of the band gap Eg through the relationship.

$$n_i = \sqrt{N_c N_v} e^{\frac{-E_g}{2kT}}$$

where k is Boltzmann's constant, T is the temperature expressed in Kelvin, while N_c and N_v are the densities of the states respectively in the conduction band and in the valence band, which are calculated with the relations [12].

$$N_c = 2\left(\frac{2\pi kTm_n^*}{\hbar^2}\right)^{3/2}$$

$$N_v = 2\left(\frac{2\pi kTm_p^*}{\hbar^2}\right)^{3/2}$$

where h is Planck's constant, m_n^* and m_p^* are the average values of the effective mass on the density of the electron and hole states, respectively. The dependence of the energy gap of a semiconductor on temperature is shown by the Varshni relation [13]

$$E_g(T) = E_g(0) - \frac{\alpha T^2}{\beta + T}$$

with E_g (0) band gap at the temperature of 0 K, α and β are parameters.

The Varshni relation is suitable for calculating the energy gap for any semiconductor up to 800 K, provided that appropriate values of E_g (0) are used for the specific structure considered. The intrinsic concentration of carriers is strongly dependent on temperature, in particular the

intrinsic concentration increases with increasing temperature. Fig. 6 shows the trend of the intrinsic concentration (cm^{-3}) vs the temperature (K) for Si, GaN, 4H-SiC and 6H-SiC [1].

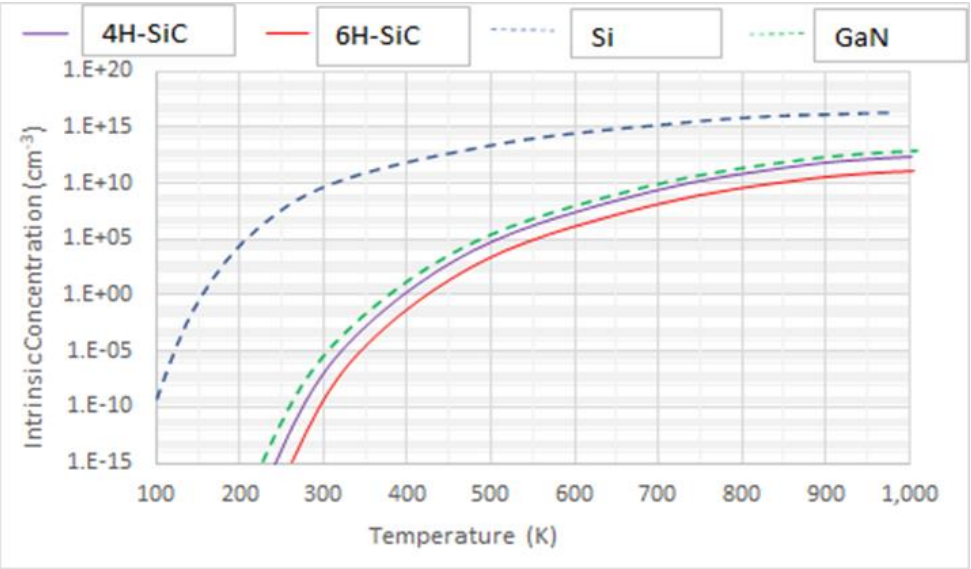

Fig. 6: Trend of intrinsic concentration with respect to temperature for Si, GaN, 4H-SiC and 6H-SiC

For Si, when the temperature increases from 25 ° C to 300 ° C, the density increases from the level of 10^{10} cm^{-3} to the level of 10^{16} cm^{-3} close to the dopant density level and most devices will not work correctly.

However, for 4H-SiC, at 300 ° C it settles to the level of only 10^{5} cm^{-3} and therefore the device can still function properly.

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CHAPTER 2

Contamination and energy states in SiC Bandgap

The Defects are crystal imperfections of different dimensions; point defects are 0-Dimensional defects, line defects, such as dislocations, disturb one dimension and planar defects, which extend over two dimensions, are caused by stacking faults. During growth, subsequent cooling and device processing, defects will be created intentionally or unintentionally in the SiC lattice [1]. Defects can be intentionally introduced by impurity doping to increase conductivity. The introduction of deep levels, which serve as trapping centers, decreases the minority charge carrier lifetime, or increases the resistivity by compensation effects.

Some common defects are explained as showed in Table 1:

Dimension	Defect Type	Examples
0	Point Defects	Vacancies Interstitial defects Substitutional Defects Frenkel Defects
1	Line Defects	Edge Dislocations Screw Dislocations
2	Planar Defects	Stacking Faults Twins Grain Boundaries Surface Defects
3	Volume Defects	Precipitates (Cluster) Voids

Table 1: Classification on defects in crystals

The purpose of this section is to show a general overview of different defects in crystal with particular attention to points defects and extended defects and their effect to parameteric and reliability failures.

2.1 Point Defect in Silicon Carbide

Point defects are point-like defective volumes, limited roughly to the size of a unit cell of the crystal structure, such as a substitional impurity, vacancy, interstitial or antisite.
An early review on point defects in SiC was given by Schneider et al [2] in 1993.

2.1.1 Description and summary

- *Substitutional impurity*: is an atom which does not belong to the crystal lattice, and it replaces another atom
- *Vacancies* are atomic lattice positions left empty in the crystal.
- *Interstitials* are atoms not placed in an ordinary lattice site but in between and they differ in:
    - *Self-Interstitials* when they are of the same kind of the crystal lattice.
    - *Impurity-Interstitials* when they are different from the crystal lattice.
- *A Frenkel Pair* is an interstitial atom together with a vacant lattice site.
- *An antisite* occurs when in a compound semiconductor, such as SiC, C is taking the Si-Lattice site, or a Si is sitting on a C-place.
- *Complexes or complex structures* are defects including two or slighty more atoms
- A *vacancy-impurity* complex is a vacancy paired with an impurity atom
- A *Split-Interstitials* occurs when two atoms take the lattice place of only one atom and thus disturbing the lattice locally. As example in SiC when two carbon interstitials are close to a carbon atom and they shift it from its original position. This is a dumbbell self intestitial complex.

In the end we can distinguish between intrinsic and extrinsic defects, in the former defective volume is composed of the same atoms as the undisturbed crystal lattice while in the latter atoms, such as doping impurities, take part in the defect.
Increasing the numbers of joining atoms, the defect can be assigned to defect clusters, such as Ci-aggregates. Finally, if whole atomic planes are shifted, the defect is no longer a point defect but belongs to the class of extended defects, which are not going to be discussed in detail in this thesis.

2.1.2 Classification

Defects in the band gap can be classified according to their energetic properties in the gap, whether they are shallow - hydrogenic impurities or deep. Deep levels can be further characterized by their interaction strength with the bands, as traps or recombination. Defects are often divided into two groups: shallow and deep levels. Depending on the size of the band gap, a level may be regarded by its energetic location as deep in Ge or Si but may be shallow in a wide-band gap semiconductor.

Defects can also be classified as shallow or deep defects based on the location of their energy levels in the bandgap of the semiconductor.

2.1.2.1 Shallow Levels

A shallow level is due to a small perturbation of the lattice potential by a coulombic (=electrostatic) potential. It is generally created by a substitutional doping atom, able to bind an electron (if created by a donor atom) or a hole (if created by an acceptor atom), the same way an electron is bound by an H+ ion, i.e. the trapped carrier sees a long-range 1/r potential. The discrete levels thus generated are hydrogen-like type and they are localized in the proximity of the purity ion. They are also characterized by a low ionization energy related to the semiconductor bandgap.

This follows the Rydberg or hydrogenic model, with binding energy = 1 Ry* (effective Rydberg) and mean distance to central atom 1 a* (effective Bohr radius). Due mainly to the high permittivity value, and sometimes the low effective mass, the 1/r potential extends over many lattice atoms and the binding energy is much lower than in the hydrogen atom: 1Ry* = m*/eps^2 x 13.6eV, and a*=eps/m* x 0.53 Å. The wavefunction of the trapped electron or hole extends over a*=100Å in GaAs, with a binding energy of 1 Ry*=5 meV, and over a*≈30Å in Si, with a binding energy in the 40-50 meV range.

One of the most common shallow levels is those impurities introduced by doping, which directly modifies the electrical properties (conductivity, carrier mobility etc.) of the semiconductors. In addition to impurities that usually take place as substitutions, the interstitial atoms that contribute to shallow levels.

Shallower levels have a large interaction with one band, which is due to the large extension of its electron wave-functions. The electrons are loosely bound to the impurity and thus move like free electrons but with a different mass. The thermal energy at room temperature is enough to ionize a large amount of the levels, meaning emission of charge carriers to the adjacent bands; thus, they are used as donor or acceptor levels. The potential of shallow levels can be

approximated by a hydrogen-like COULOMB potential screened by dielectric permeability, μ, of the host lattice and with modified effective masses, m*.

2.1.2.2 Deep Levels

As mentioned, in addition to shallow impurities, it can be present inside a semiconductor a concentration of deep-type impurities, or localized impurities. The difference with the previous case of shallow traps is that the perturbation brought by the defect to the lattice potential is now much larger in the close vicinity of the trap (close means < 1-2 interatomic distance). Thus, the wavefunction of the trapped lectron (or hole) is much more localized. What creates the perturbation may be an interstitial atom (coupled with some lattice distortion around it), or a vacancy, or an antisite (e.g. atom III in the place of an atom V or vice-versa), or a more complex defect (but still a point defect) combining several of these aspects (e.g. interstitial + vacancy). The involved energy is not only the long range coulombic potential, but contains in addition terms related to the "lattice relaxation", i.e. the energy necessary to rearrange all the lattice atoms included in the close vicinity of the trap origin. Depending on whether a carrier is trapped or not by the deep trap, each atom position rearranges, which corresponds to a part of the thermal (equilibrium) energy between the trapped and untrapped states.

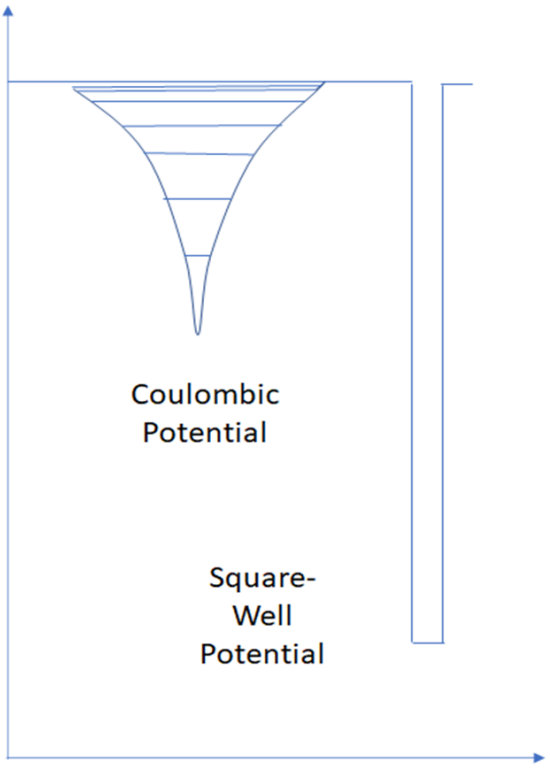

Fig. 1: One dimensional potential of shallow and deep levels

In addition, there is a barrier energy to be overcome between these two states, that for some sorts of deep traps may be much higher than either thermal energies, leading e.g to metastability at low temperature.

For deep type centers, the hydrogenic approximation is no longer valid [3], due to the fact that the carrier-impurity binding energy is much larger than for shallow impurities, so that the Bohr radius of the system is less than or comparable to the reticular pitch of the crystal: in fact, we speak in such cases of localized impurities.

For these reasons, the ground state of a deep center is located approximately in the center of the forbidden gap of the semiconductor, so for the ionization energy we have: Eion ~ Eg / 2. These states can capture electrons and / or holes (they are therefore called "traps"), with probability of different entrapment, depending mainly on the distance in energy from a band or on the other; if the probabilities of electron and hole capture are similar, the center is capable of trapping an electron and a hole in rapid succession, annihilating them and dissipating energy transition in a radiative or non-radiative way: in this case the level is said to be a center of radiative or non-radiative recombination, respectively.

In the case of radiative recombination, a corresponding peak will appear in the spectrum of issue; the energy position of the peak will be equal to the ionization energy of the center,

while the integral intensity will be proportional to their concentration in the material.

The structures that give rise to the deep levels are generally made up of defects or impurities native or introduced accidentally during processes, therefore unintentional: the presence of such structures is normally undesirable with regards to the performance of the material, due to the the fact that the deep centers act as traps for the carriers, lowering the concentration of free charges in the crystal, hence the electrical conductivity; furthermore, acting as centers of alternative intermediates recombination, lower the efficiency of band-band recombination processes, thus degrading the performance of optoelectronic devices.

The density of these centers strongly depends on the quality of the crystal, so an estimate of the purity of the material can be made by analyzing its concentration.

Fig. 2 shows a schematic of the band structure of a typical direct gap semiconductor in where shallow and deep levels are represented.

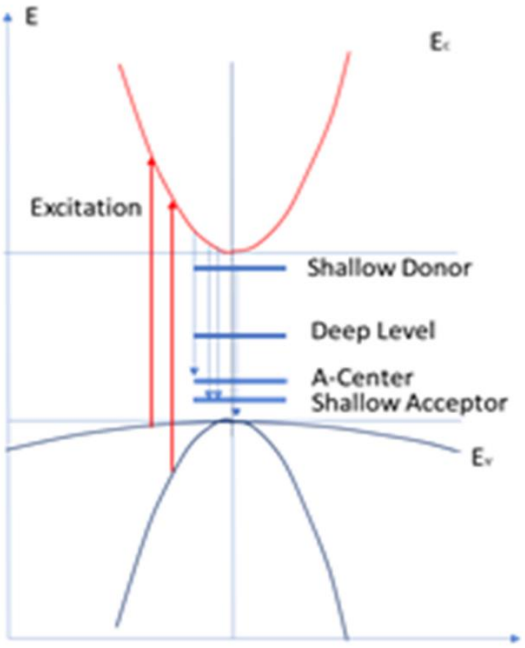

Fig. 2: Shallow and deep levels. "A" centers showed in the figure, are particular deep levels typical of some materials

Generally, the deep levels have less contribution to conduction compared with the shallow levels of dopants due to their relatively low concentration and large activation energy [4]. However, these deep levels can play an important role in the recombination process and are regarded as a significant limitation on carrier lifetime especially when the energy levels lie near the middle of the bandgap. As one of the applications, it is possible to release the carrier storage effect by limiting carrier lifetime with the help of recombination center introduced by Au impurities in silicon devices, since Au is known as a lifetime killer in silicon.

Deep levels can further be classified after their primary interaction with the bands. If the electron capture rate, cn, is much larger than the hole capture, cp (cn _ cp), then the defect is called electron trap; vice versa if the hole capture is larger than the electron capture, then the defect is acting as a hole trap (cp _ cn). If both capture rates are almost similar (cn _ cp), then the defect interacts with the same strength with both bands and is regarded as a generation-recombination center (G-R center), as shown in Fig. 3.

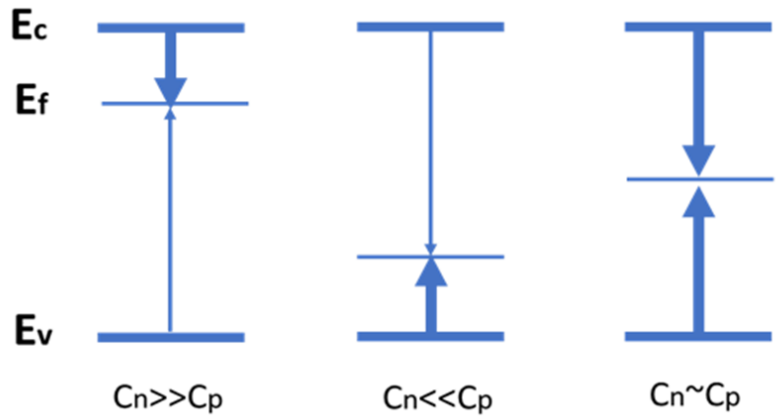

Fig. 3: Capture and emission characteristics of traps and recombination centers.

2.2 Crystal Imperfections and extended Defects in Silicon Carbide

SiC boule crystals and wafers contain a variety of crystal imperfections, both extended defects and point defects. This subsection describes the evolution and reduction of extended defects. The density of point defects in SiC boules is rather high, in the 10^{14}–10^{16} cm^{-3} range. Shows the major extended defects observed in SiC boules and wafers. The Burgers vector, which represents the magnitude and direction of the lattice distortion resulting from a dislocation in a crystal lattice, the major direction, and the typical density of the extended defects in boules (wafers) prepared using state-of-art technology (for n-type 4H-SiC) are shown with additional comments. Note that, through recent efforts, three-dimensional defects such as large carbon inclusions and voids are now eliminated.

2.2.1 Stacking Faults

Stacking faults refer to the locally changed stacking order of atom layer(s) in the structure. For example, instead of the typical stacking sequence ABCABCABC of face centered cubic (fcc) structure, the structure with stacking fault may be ABCABABCAB.

Stacking faults are common defects because of the low stacking fault energy (14 mJ m^{-2} for 4H-SiC and 2.9 mJ m^{-2} for 6H-SiC) and the occurrence of many polytypes in SiC. Typical stacking faults are 3C- or 6H-like laminar regions in 4H-SiC boules. Generation of double Shockley stacking faults observed in heavily-nitrogen-doped SiC. In Table 2, major extended defects observed in SiC boules and wafers are represented.

Through the recent progress in polytype control, inclusions of foreign polytypes and stacking faults have been greatly reduced. The typical stacking fault density along the c-axis is well

below 1 cm^{-1}. Generation of stacking faults *during SiC epitaxial growth* is one of the remaining issues.

Dislocation	Burgers Vector	Major Direction	Typical Density (cm^{-2})
Micropipe	$n < 0001 > (n > 2)$	$< 0001 >$	$0 - 0.1$
Threding Screw Dislocation (TSD)	$n < 0001 > (n = 1,2)$	$< 0001 >$	$300 - 600$
Threding Edge Dislocation (TED)	$< 11\bar{2}0 >/3$	$< 0001 >$	$2000 - 5000$
(Perfect) Basal Plane Dislocation (BPD)	$< 11\bar{2}0 >/3$	In {0001} plane (preferably $< 11\bar{2}0 >$)	$500 - 3000$

Table 2: Major extended defects observed in SiC boules and wafers. The Burgers vector, major direction, and typical density of the extended defects in boules (wafers) prepared using state-of-art technology (for n-type 4H-SiC) are shown.

2.2.2 Micropipe Defects

A micropipe defect is a hollow core associated with a *superscrew dislocation*. When the Magnitude of the Burgers vector is very large, the strain field around the dislocation core becomes extremely high (proportional to $|b|^2$, where b: Burgers vector) and a microscopic pinhole is formed by breaking bonds. Micropipe defects are indeed located at the center of a large spiral on the surface of the SiC boule, and the diameters of the pinholes range from 0.5 μm to several micrometers [5]. In SiC, the Burgers vector of an elementary threading screw dislocation (TSD) is already very large because the length of 1c corresponds to 1.0 nm for 4H-SiC and 1.5 nm for 6H-SiC, which is much larger than that for Si (~0.24 nm).

The magnitudes of the Burgers vector for micropipes have been investigated in detail, and the minimum values were determined as |3c| for 4H-SiC and |2c| for 6H-SiC both of which correspond to 3 nm. In old wafers, a large micropipe with a Burgers vector of 8–12c was also observed [5]. Fig. 8 shows an example of a micropipe in a 4H-SiC (0001) wafer, as observed by (a) optical microscopy and (b) atomic force microscopy. Near the center, a pinhole is discernible as a dark spot. When the wafer is observed in transmission mode, a dark line running along the c-axis can be traced.

Because a micropipe is a pinhole extending along the <0001> direction through the entire SiC wafer, it is not surprising that SiC devices which contain a micropipe exhibit severely degraded performance, such as excessive leakage current and premature. Micropipes also act as a source of impurity contamination in epitaxial growth and device processing. Thus, micropipes were identified as the most important killer defects, and growth technology has now been developed to eliminate micropipes.

Table 3 shows the possible causes of micropipe generation during the sublimation growth of SiC. These possible causes can be classified into fundamental and technological issues. The fundamental issues include thermodynamic mechanisms such as thermoelastic stress arising

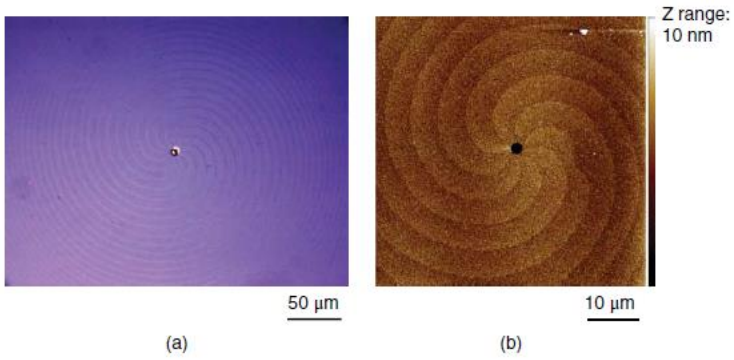

Fig. 4: Micropipe in a 4H-SiC (0001) wafer, as observed by (a) optical microscopy and (b) atomic force microscopy.

Fundametal		
Thermodinamic	**Kinetic**	
Thermal field unformity	Nucleation Processes	
Dislocation formation	Inhomogeneous Supersaturation	
Solid-State Transformation	Constitutional Supercooling	
Vapor Phase Composition	Growth Face Morphology	
Vacancy Supersaturation	Capture of gas phase Bubbles	
Technological		
Process Instabilities	Seed Preparation	Contamination

Table 3: Possible causes of micropipe generation during the sublimation growth of SiC

from non-uniform temperature distribution, and kinetic mechanisms such as an unwanted nucleation process. Technological issues such as process instabilities, imperfect surface preparation of a seed, and carbon inclusions also need to be considered. Inclusion of foreign polytypes causes severe mismatch in the stacking sequence when such an island meets the host polytype. This stacking mismatch and the associated large strains also trigger micropipe formation. When elementary screw dislocations are introduced for some reason, the spiral steps emanating from them interact with each other. Because of the strong repulsive interaction

between steps, the energetic bunching of spiral steps promotes the coalescence of adjacent screw dislocations, leading to micropipe formation. Accumulation of screw dislocations around a surface depression, and the interaction between screw dislocations and twist-type misorientation have also been suggested as mechanisms of micropipe formation.

2.2.3 TSD, TED and BPD

Threading screw dislocation (TSD) is located at the center of spiral growth during sublimation growth on a SiC {0001} surface. Fig. 5 shows a schematic illustration of an elementary TSD in SiC.

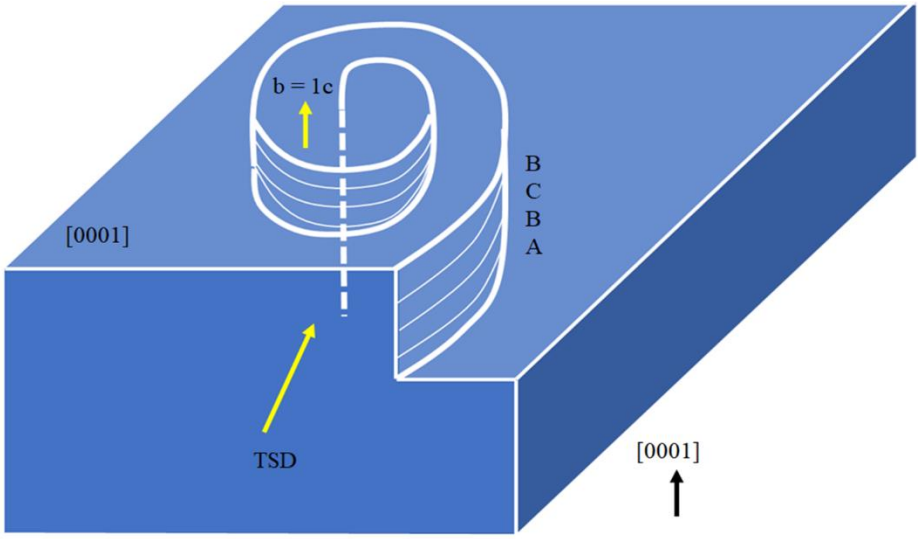

Fig. 5: Schematic illustration of an elementary threading screw dislocation in SiC.

The TSDs usually propagate almost along the <0001> direction, but occasionally they are bent toward the basal planes (and sometimes again bent back toward <0001>).

Threading screwdislocations are basically replicated from a seed crystal, as also occurs formicropipes. A major cause of threading-screw-dislocation nucleation in SiC sublimation growth is the generation of a half loop at the initial stage of bulk growth.

As shown in Fig. 6, in case an extra (or missing) half plane introduced into a boule crystal, a dislocation with a Burgers vector of [1120]/3 exists along the edge of the extra half plane. The dislocation lying in the basal plane (line AB) is defined as a “BPD” (pure edge-type), and the dislocation lying along the <0001> direction (line BC) is defined as a “TEDn”. Therefore, “BPD” and “TED” have the same basic nature; the name simply differs depending on the dislocation direction. In fact, inside the boule crystals, conversion from BPD to TED and from TED to BPD is often observed.

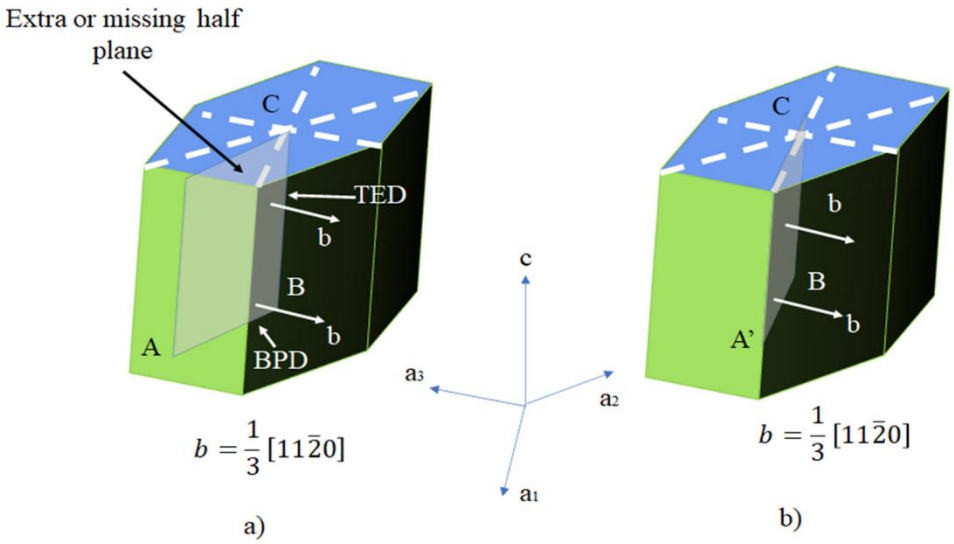

Fig. 6: (a) Schematic illustration of an extra (or missing) half plane introduced into a SiC crystal. (b) Typical configuration of threading edge and basal plane dislocations,where the basal plane dislocation lies along a <1120> direction.

2.2.4 Surface Morphological Defects

Surface defect is another significant category of defect. Generally speaking, surface defects do not refer to the specific defect type as discussed before but focus on the position where large fraction of dialing bond occur and the periodic of lattice is destroyed. As a result, the carrier lifetime, mobility etc. can be affected near the surface. In addition, similar defects can lie in the interface between semiconductor and metal/oxide and is recognized as interface states, which can be the decisive factor of Schottky barrier height under certain circumstance instead of the metal type.

Except step bunching, SiC epitaxial layers grown on off-axis {0001} substrates exhibit several types of surface defects. Fig. 7 shows the typical surface defects observed in 4H- and 6H-

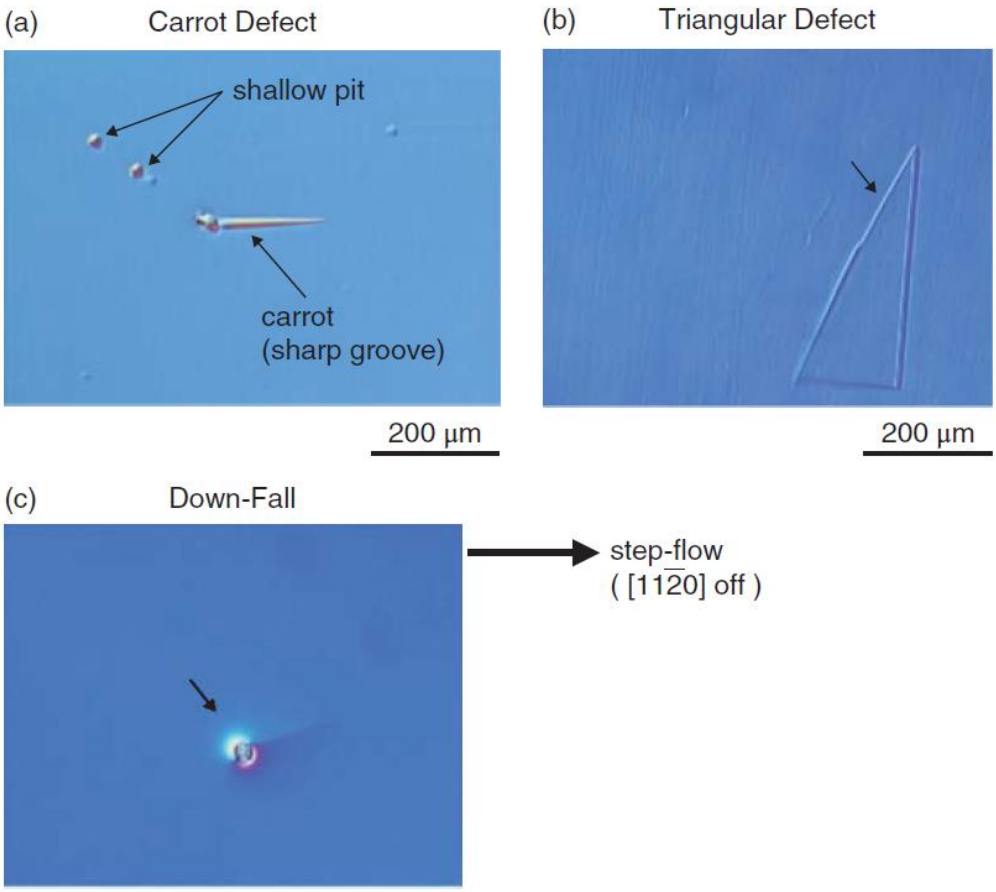

Fig. 7: Typical surface defects observed in 4H- and 6H-SiC{0001} homoepitaxial layers: (a) "carrot" defect and shallow pit, (b) triangular defect, and (c) down-fall.

SiC {0001} homoepitaxial layers, (a) "carrot" defect and shallow pit, (b) triangular defect, and (c) down-fall. Although the exact formation mechanisms of these defects are not fully understood, they are usually created by technical issues such as incomplete removal of polishing damage or non-optimized growth processes. The down-fall is generated by a SiC particle initially formed on the susceptor wall falling down. The density of these defects is mostly influenced by the surface quality of the substrates and the conditions used for the growth process. The density of these defects depends only slightly on the substrate quality.
The carrot (in some case "comet" depending on the defect shape and structure), and triangular defects are usually elongated along the down-step direction of step-flow growth, which is a sign of disturbance of step-flow growth. As schematically shown in Fig. 8.

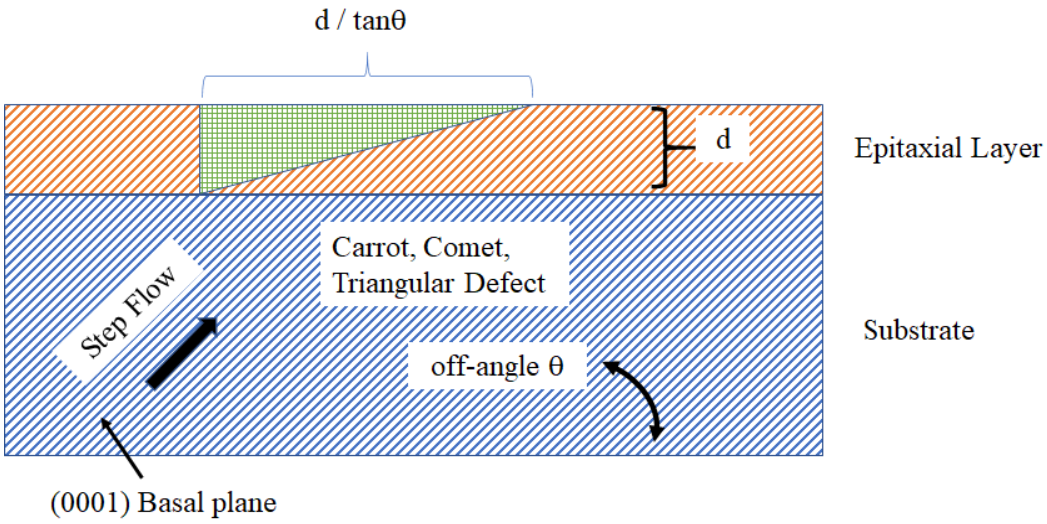

Fig. 8: Schematic illustration of an epitaxially-induced defect in SiC. The defect length along the off-direction (L) is close to the length of a basal plane in the epitaxial layer when projected onto the surface, considering the substrate off-angle (θ).

the defect length along the off-direction (L) is very close to the length of a basal plane in the epilayer when projected onto the surface, taking into account the substrate off-angle (θ):

$$L \approx depi / \tan \theta$$

where depi is the epilayer thickness. This observation has a very important implication – these defects are nucleated at the very initial stage of epitaxial growth. If these defects are observed (though they are not desirable), the epilayer thickness can be estimated from the defect length. The triangular defects also exhibit a variety of structures. In some triangular defects, the triangular region is indeed 3C-SiC, while in other triangular defects only a 3C-like laminar region with a thickness of several Si-C bilayers is extended in the basal plane. In some cases, no 3C-SiC regions are observed, and a partial dislocation runs along the two sides of the triangular shape. So far, extended defects are not always observed beneath the shallow pits (typical depth: 20–100 nm). It is of interest that higher densities of carrot (or comet) defects and triangular defects are generated when the epitaxial layers are grown under Si-rich and C-rich conditions, respectively. Under Si-rich conditions, TSDs tend to be deflected into basal planes, forming Frank-type stacking faults.

2.2.5 Dislocations

As a common example of extended defects, dislocation stands for the bending of atom planes surrounding due to the termination of the atom plane in the crystal. and can be classified as screw dislocation or edge dislocation according to different types. By studying the dislocations parallel to the Schottky contact, FIGIELS has discussed that the kinetics of electron emission from dislocation will be drastically modified due to the configuration entropy. Therefore, the Deep Level Transient Spectroscopy (DLTS) transients no longer follow the exponential law and results in the broadening of DLTS signal.

Most dislocations in 4H-SiC homoepitaxial layers originate from dislocations in 4H-SiC substrates. Therefore, the dislocation density of a SiC homoepitaxial layer depends greatly on the quality of the substrate, assuming that the epitaxial growth process is sufficiently optimized.

Major dislocations in SiC substrates include TSDs, TEDs, and basal plane dislocations (BPDs), as described in Section 2.2.3. Fig. 9 illustrates the dislocation replication and conversion typically observed in 4H-SiC epitaxial layers grown on off-axis {0001} by CVD. Almost all the TSDs in a substrate are replicated in an epilayer, but a small portion (typically <2%) of TSDs are converted to Frank-type partial dislocations. A TSD in the substrate can act as a nucleation site for a carrot defect, as described above.

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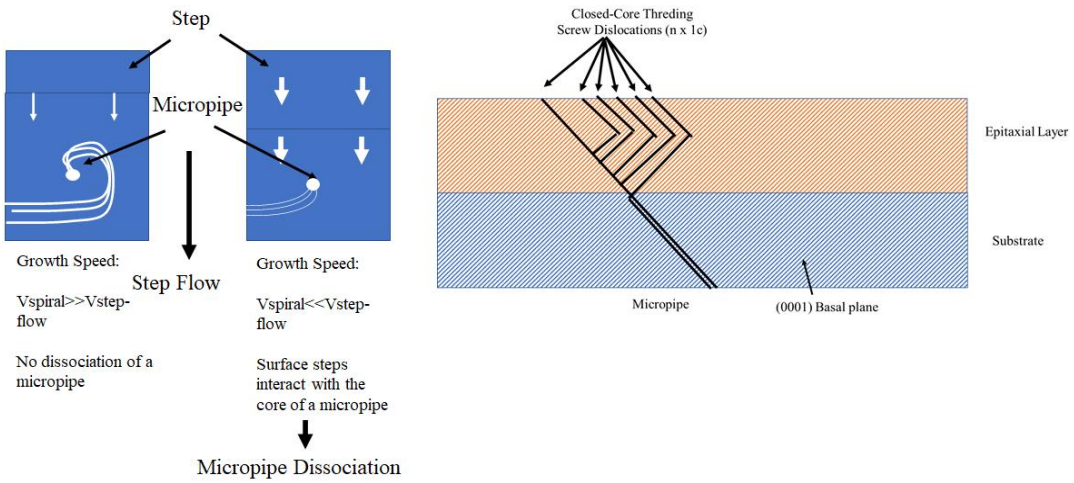

Fig. 9: Schematic illustration of micropipe closing. A micropipe in an off-axis SiC(0001) substrate can be dissociated into several elementary closed-core screw dislocations during CVD growth.

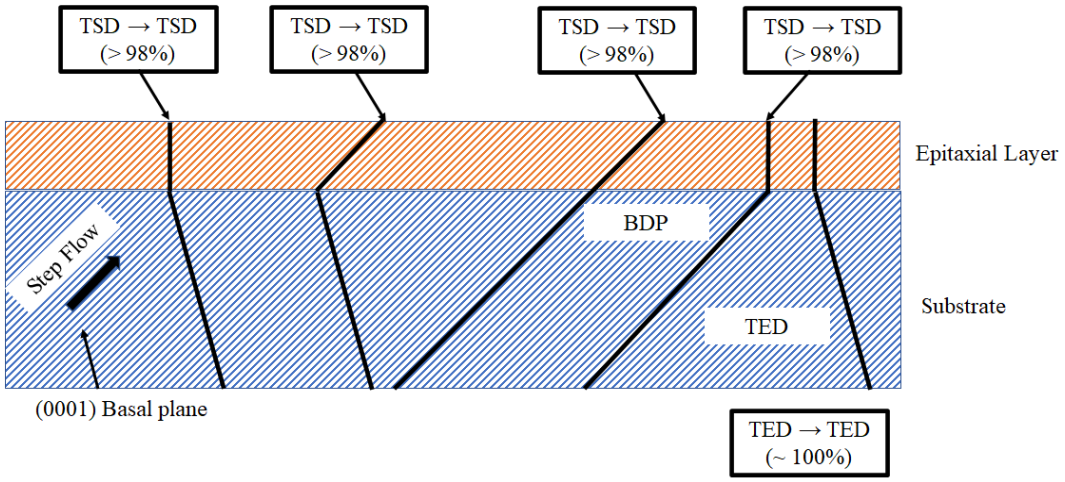

Fig. 10: Schematic illustration of dislocation replication and conversion typically observed in 4H-SiC epitaxial layers grown on off-axis {0001} by CVD.

The behavior of BPDs during epitaxial growth is much more complicated. A BPD is a detrimental defect for SiC bipolar devices because it can be the source of a Shockley-type stacking fault upon carrier injection, and such a stacking fault causes local reduction of carrier lifetimes (increase of on-resistance) and increase in leakage current This is called “bipolar degradation”.

2.2.6 Defects which impact reliability

As silicon carbide power devices enter the silicon dominated power electronics market, there is an increased interest in the reliability of SiC power devices. As presented in the work of R. E. Stahbush [6] materials defects affect SiC devices introduce leakage paths and by reducing conductivity in the device drift region. In particular the role of extended defects such as dislocations and stacking faults – as opposed to point defects has been discussed. While many of these extended defects reduce the yield of device fabrication, basal plane dislocations (BPDs) are the primary defect affecting device reliability.

As discussed by Senzaki [7] each defect degrades the manufacturing yield and reliability for SiC power devices in particular micropipes are critical and possibly lead to devices with no blocking capability, and device destructions through dislocation growth/multiplication.

However, mst of the studies included in this work are related to the gate oxide reliability which is strongly affected by SiC defectivity, most of all related to extended defects.

Early failure simulations [8] shows that the bulk defects in the gate oxide are the likely culprit for early TDDB failures through an increase in tunneling current via trap-assisted-tunneling (TAT) dominating the early failure distributions.

Recent studies have shown that the bias temperature instability (BTI) risk for such devices is diminishing due to recent advances in annealing and interface passivation [9, 10]. The intrinsic TDDB performance was also shown to be comparable, if not better than, that of similar SiO_2/Si devices [4]. The high scale production and the higher volume forces semiconductor companies to take under control at an higher level the extrinsic defects reducing at maximum the early failures which is what dictates the overall product reliability. This study greatly extends earlier efforts to identify the origin of these early failures by establishing a correlation between the extrinsic tails of measured failure distributions and user defined lucky defect profiles for arbitrarily chosen device populations.

Then the double purpose of the process improvement is to identify the cause of defectivity, reducing the related amount and to characterize the effect by several characterization techniques such as C-V, charge injection effect and reliability techniques such as TDDB test to extrapolate the gate oxide lifetime under operative voltage.

Moreover, in the characterization scenario, since 1990s, a great deal of research about deep level defects in SiC has been done with the help of DLTS or other investigation methods. The donor deep levels with almost full range of activation energy have been reported, as is shown in Fig. 11.

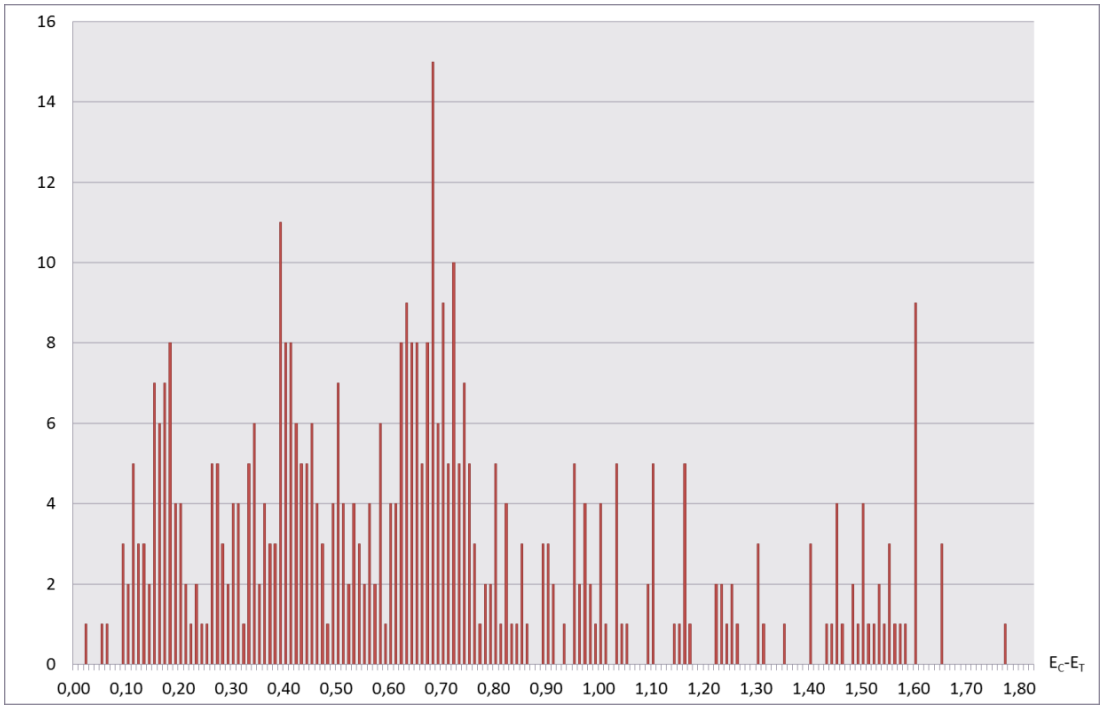

Fig. 11: Number of articles which report defects with certain activation energy in 4H-SiC.

Obviously, these deep levels focus on activation energy from 0.1 eV to 0.9 eV, including the well-known $Z_{1/2}$ defect with E_a around 0.68 eV.

Various of impurity defects have been investigated by means of doping or implantation, part of them found in 4H-SiC. Other impurity de-fects such as O and Er have been reported in 6H-SiC.

Recently, more attention has been payed on characteristic of deep level defects and its relation to device properties. Danno and Kimoto have pointed out the similarity between Z1/2 and EH6/7 (with around 1.6 eV) due to the fact that the concentration of Z1/2 and EH6/7 have the same trend regardless of As-growth, irradiation or annealing. They believe a E both centers contain the same defect such as a carbon vacancy. As the two dominant electron traps, Z1/2 and EH6/7 could both survive after high temperature annealing at 1700 ℃. However, Klein argued that Z1/2 acted alone as the lifetime limiting defect. By comparing the concentration of carbon vacancy (VC) determined by electron paramagnetic resonance with that of Z1/2 defect obtained by C-V and DLTS.

Impurities in semiconducting materials can result in poorer property such as a carrier lifetime reduction. Especially those deep level defects, which are close to midgap, can be efficient recombination centers or carrier traps. Meanwhile, charged interface traps directly affect the device performance by increasing the threshold voltage, degrading the channel mobility and

causing leakage current for MOS applications. On the other hand, trap levels can be sometimes important for carrier lifetime adjustment as well as in the application of LEDs. These deep level defects can not only be caused by irradiation or impurities such as Ti, V, Cr but also be intrinsic defects introduced by manufacturing process such as carbon vacancy (VC). Activation Energy (Ea), capture cross section (σ) and defect concentration (NT) are all significant parameters for deep level defects identification. as shown in Table 4.

On the other hand, the correlation between the observation of the two barrier height behavior in the I-V characteristics and traps measured from DLTS and Random Telegraph Signal (RTS) dates back to year 2002. It was pointed out that the I-V characteristics tended to degrade with increasing deep-level concentration and those inhomogeneous diodes tended to contain defect clusters, which can lead to a local Fermi-level pinning.

Defects	**$E_a=E_c-E_f$ (eV)**	**σ (cm^2)**	**NT (cm^{-3})**
Ti	0.13	7×10^{-15}	3.66×10^{10}
	0.17	1×10^{-15}	1.17×10^{11}
Cr	0.15	2×10^{-15}	1.4×10^{13}
	0.18	8×10^{-16}	1.3×10^{13}
	0.74	2×10^{-15}	\
V	0.80	1.79×10^{-16}	3×10^{17}
	0.89	\	$<1 \times 10^{14}$
	0.97	6×10^{-15}	\
Fe	0.39	2×10^{-15}	7.6×10^{12}
Ta	0.68	8×10^{-15}	\
Intrinsic	0.56	5×10^{-17}	
	0.62	\	1.2×10^{15}
	0.66	1.31×10^{-14}	\
	0.68	7×10^{-15}	1×10^{13}
	0.72	2×10^{-14}	9.5×10^{14}

Table 4: Activation Energy (Ea), capture cross section (σ) and defect concentration (NT) for deep level defects identification

Transition metals (TM) introduce shallow and deep levels in SiC, which are crucial for the charge carrier concentration and the minority charge carrier life-time. The most studied TMs in SiC are Titanium (Ti), Vanadium (V), Chromium (Cr) and Tungsten (W). Ti, Cr and V are dominant background impurities due to their presence in parts of SiC growth (both sublimation and epitaxial CVD) reactors. V attracts attention for its ability to compensate the residual nitrogen doping to obtain semi-insulating Si by a deep donor level in the middle of the gap (EC 1.59 eV). An additional level is detected at EC 0.97 eV is discussed having an amphoteric character, i.e. both donor and acceptor levels in the SiC band gap. Ti introduces two shallow levels (EC 0.13 eV and EC 0.17 eV) in the band gap of 4H-SiC, which accounts for the two inequivalent lattice sites.

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CHAPTER 3

Electrical Characterization of Defects in Gate Dielectrics

In this chapter we will discuss the measurement techniques to characterize the charges at the interface and in the gate oxide. Defects in gate oxides/insulators could be characterized by many electrical and physical techniques. These methods played a crucial role during the early MOS and PowerMOSFET development to determine the origin of oxide/interface charges that led to unstable devices [1]. In this section I give a brief description of the common defects (oxide, border and interface traps), on which most of yield improvement activities are dedicated on defective substrates such as Silicon Carbide and then describe many of the more common electrical characterization techniques.

3.1 Oxide defects

In this section the main defects commonly observed in insulators, some in thermally-grown [1] or deposited SiO_2, others in non SiO_2 insulators, and some generated or propagated during epitaxial growth will be described. Some aspects of oxide breakdown as it pertains to oxide defects will be also briefly touched on.

3.1.1 Fixed oxide charge

Fixed oxide charge was identified early during MOS development and was attributed to excess silicon near the SiO_2/Si interface in thermally-grown oxides [2]. The model was that as an oxide grows on a Si wafer, oxygen diffuses through the growing oxide to react at the interface forming SiO_2. This leaves some excess Si in the oxide near the interface. As the growing oxide front moves into the wafer, the excess Si moves with it and defects associated with this excess Si become positively charged during negative bias stress. The fixed oxide charge is not in electrical communication with the underlying silicon [1]. The same considerations can be made for the oxides deposited on SiC. Theoretically, the oxidation processes should eliminate carbon in the face of the growth of SiO_2 oxide on the SiC surface. However, this does not happen in trials real, since there may be carbon atoms in the interstitial regions of the oxide or vacancies of oxygen atoms that constitute defects at the SiO_2/SiC interface. It is possible to reduce oxide charges by annealing the oxidized wafer in a nitrogen or argon ambient after oxidation.

3.1.2 Mobile oxide charge

In the MOS capacitor or PowerMOSFET mobile charge in SiO_2 is due primarily to the ionic impurities [1]. Among the mobile charges present in the oxide we find: Sodium is the dominant contaminant, Lithium has been traced to oil in vacuum pumps and Potassium which can be introduced during chemical-mechanical polishing. MOSFETs were very unstable for positive gate bias but relatively stable for negative gate voltages. Sodium was the first impurity to be related to this gate bias instability.[3] By intentionally contaminating MOS capacitors (MOS-Cs) and measuring the gate voltage shift after bias temperature stress, it was shown that alkali cations could easily drift through thermal SiO_2 films [1].

Chemical analysis of etched-back oxides by neutron activation analysis and flame photometry was used to determine the Na profile [4]. The drift has been measured with the isothermal transient ionic current, the thermally stimulated ionic current, and the triangular voltage sweep methods.[5]

$$\mu = \mu_0 e^{\left(\frac{E_A}{kT}\right)} \tag{1}$$

where for Na: μ_0=3.5x10^{-4} cm^2/V·s (within a factor of 10) and E_A=0.44±0.09 eV; for Li: μ_0=4.5x10^{-4} cm^2/V·s (within a factor of 10) and E_A=0.47±0.08 eV, for K: μ_0=2.5x10^{-3} cm2/V·s (within a factor of 8) and E_A=1.04±0.1 eV, and for Cu, μ_0=4.8x10^{-7} cm^2/V·s and E_A=0.93±0.2 eV.[6] If the oxide electric field is taken as V_G/t_{ox}, neglecting the small voltage drops across the semiconductor and gate, the drift velocity of mobile ions through the oxide is $v_d=\mu V_G/t_{ox}$ and the transit time t_t is:

$$t_t = \frac{t_{ox}}{v_d} = \frac{t_{ox}^2}{\mu V_G} = \frac{t_{ox}^2}{\mu_0 V_G} e^{\left(\frac{E_A}{kT}\right)} \tag{2}$$

Equation (2) is plotted in Fig. 1 for the three alkali ions and for Cu. the oxide electric field is 10^6 V/cm, a common oxide electric field for such measurements, and the oxide thickness is 100 nm [1]. Typical measurement temperatures lie in the 200 to 300°C range and only a few milliseconds suffice for the charge to transit the oxide. Mobile charge densities in the 5x10^9-10^{10} cm^{-2} range are generally acceptable in integrated circuits.

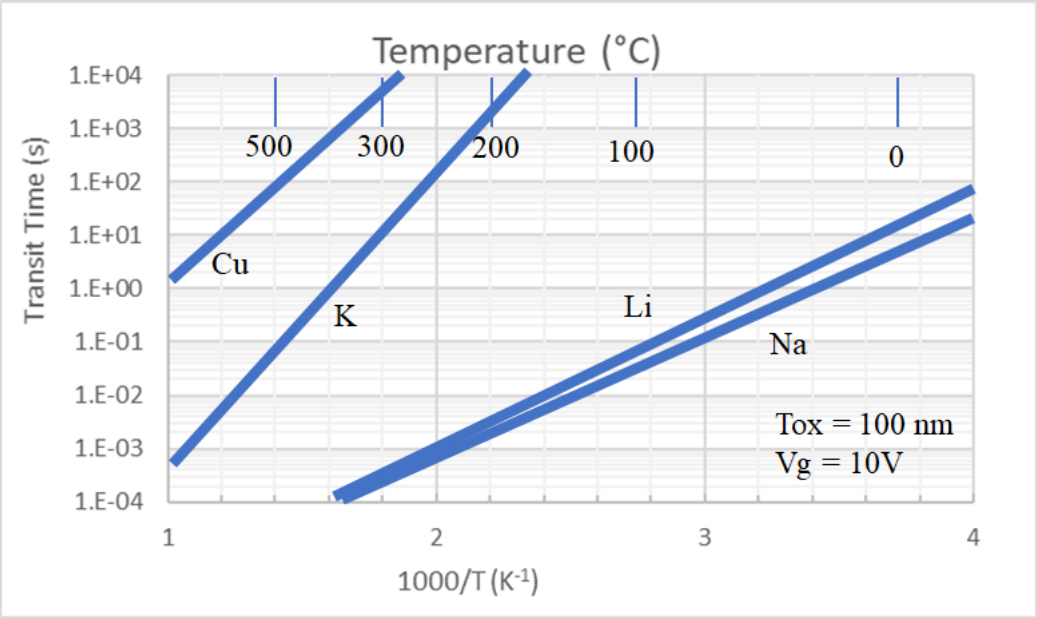

Fig. 1: Transit times for Na, Li, K, and Cu for an oxide electric field of 10^6V/cm. [Greeuw, G., and Verwey, J.F., The mobility of Na+, Li+ and K+ ions in thermally grown SiO_2 films.

3.1.3 Interface trapped charge

At the SiO_2/Si interface are present interface trapped charge, also know as interface states, interface traps, and fast surface states. One of the main causes is a structural imperfection. Silicon is tetrahedrally bonded with each Si atom bonded to four Si atoms in the wafer bulk [1]. The bonding configuration at the surface is as shown in Fig. 2(a) and 2(b) with most Si atoms bonded to oxygen at the surface after Si oxidation. Some Si atoms bond to hydrogen, but some remain unbonded. An interface trap, is an interface trivalent Si atom with an unsaturated (unpaired) valence electron usually denoted by $Si \equiv Si \bullet 3$, where the "≡" represents three complete bonds to other Si atoms (the Si3) and the "•" represents the fourth, unpaired electron in a dangling orbital (dangling bond)[1]. Interface traps, also known as Pb centers,21 are designated as D_{it} ($cm^{-2}eV^{-1}$), Q_{it} (C/cm^2), and N_{it} (cm^{-2}). The Pb ESR spectrum was first observed by Nishi [7] and later identified by Poindexter et al. as a paramagnetic dangling bond [8, 9].

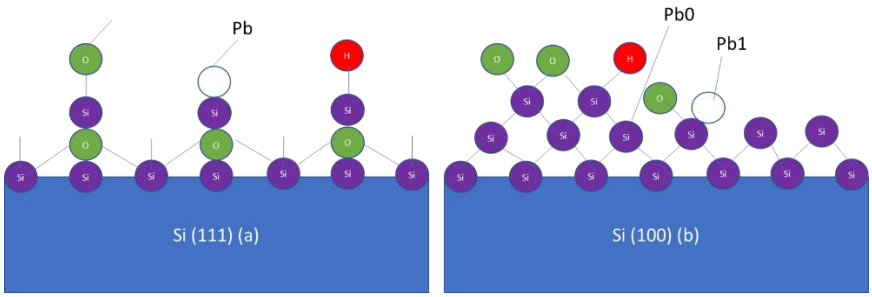

Fig. 2: Structural model of the (a): (111) Si surface and (b): (100) Si surface.

On (111)-oriented wafers, the Pb center is situated at the Si/SiO_2 interface with its unbonded central-atom orbital perpendicular to the interface and aimed into a vacancy in the oxide immediately above it, as shown in Fig. 2(a). On (100)-oriented Si, the four tetrahedral Si-Si directions intersect the interface plane at the same angle [1]. Through electron spin resonance it was possible to detect defects, named Pb1 and Pb0 and shown in Fig. 2(b) [1]. A recent calculation suggests the Pb1 center to be an asymmetrically oxidized dimer, with no first neighbor oxygen atoms.[10] By 1999, it was unambiguously established that both Pb0 and Pb1 are chemically identical to the Pb center [11]. However, there is a charge state difference between these two centers indicating Pb0 is electrically active, while some authors believe the Pb1 to be electrically inactive [12]. Interface traps are electrically active defects with an energy distribution throughout the Si band gap. They act as generation/recombination centers and contribute to leakage current, low-frequency noise, and reduced mobility, drain current, and transconductance [1]. Traps at the interface become charged when they are occupied by electrons or holes.

Interface traps at the SiO_2/Si interface are acceptor-like in the upper half and donor-like in the lower half of the band gap [13]. As shown in Fig. 3(a), at flatband, with electrons occupying states below the Fermi energy, the states in the lower half of the band gap are neutral (occupied donors designated by “0”). Those between midgap and the Fermi energy are negatively charged (occupied acceptors designated by “-“), and those above E_F are neutral (unoccupied acceptors). For an inverted p-MOSFET, shown in Fig. 3(b), the fraction of interface traps between mid gap and the Fermi level is now unoccupied donors, leading to positively charged interface traps (designated by “+”). Hence interface traps in p-channel devices in inversion are positively charged, leading to negative threshold voltage shifts [1].

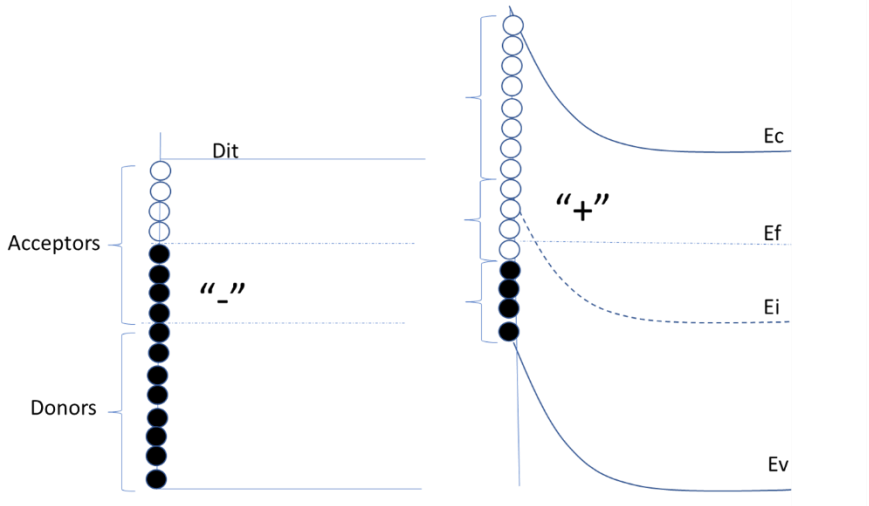

Fig. 3: Band diagrams of the Si substrate of a p-channel MOS device showing the occupancy of interface traps and the various charge polarities for a p-substrate with (a) negative interface trap charge at flatband and (b) positive interface trap charge at inversion. Interface traps are either occupied by electrons (solid circle) or holes, shown by the open circles.

3.1.4 Border traps

In 1980, a committee headed by Bruce Deal established the nomenclature for charges associated with the SiO_2/Si system, i.e., interface trapped, fixed oxide, mobile ionic and oxide trapped charge [14]. In 1992, Dan Fleetwood suggested that this list be augmented by including border traps also designated as slow states, near-interfacial oxide traps, E' centers, switching oxide traps, and others. [15, 16] He proposed border traps to be those near-interfacial oxide traps located within approximately 3 nm of the oxide/semiconductor interface. There is no distinct depth limit, however, and border traps are considered to be those traps that can communicate with the semiconductor through capture and emission of electrons and/or holes [1].

Oxide, border, and interface traps are schematically illustrated in Fig. 4(a). Defects at or near the SiO_2/Si interface are distributed in space and energy and communicate with the Si over a wide range of time scales. While for interface traps, the communication of substrate electrons/holes with interface traps is predominantly by capture/emission, for border traps it is mainly by tunneling from the semiconductor to the traps and back. Fig. 4(b) shows the flatband diagram with interface and border traps occupied by electrons to the Fermi level E_F. The border traps are shown over a wide energy range for illustrative purposes only. The band diagram in Fig. 4(c) applies immediately after VG_1 is applied, before unoccupied border and interface

traps have captured electrons. Interface traps now capture electrons from the conduction band, indicated by (ii) and inversion electrons tunnel to border traps, indicated by (i). Tunnel process (i) is followed by electron capture of lower energy border traps. In Fig. 4(d) interface and border traps up to E_F are occupied by electrons through (ii) electron capture and (iii) tunneling. For $-VG_2$ in Fig. 4(e), electrons tunnel from border traps to the conduction band (iv), interface traps (v) and the valence band (vi). The insulator electric field, shown as constant in these Fig.s, will, of course, distort as the border trap occupancy changes. I have disregarded this change here to bring out the main points.

Inversion electron tunneling is a direct tunnel process with time constant [17]

$$\tau_t \approx \tau_0 e^{\left(\frac{x}{\lambda}\right)}$$

And

$$\lambda = \frac{\hbar}{\sqrt{8m_t^*\phi_B}} \tag{3}$$

where t_0 is a characteristic time ($\approx 10^{-10}$ s), λ the attenuation length ($\approx 10^{-8}$ cm), m_t* the tunneling effective mass, and φ_B the barrier height at the semiconductor/insulator interface. τt varies from 0.01 to 1 s (100 to 1 Hz) for x varying from 1.8 to 2.3 nm. Hence border traps can be determined to a depth of approximately 2.5 nm from the SiO_2/Si interface by measurements for frequencies as low as 1 Hz [1]. Lower frequencies, of course, allow deeper traps to be characterized showing that the trap depth that can be characterized depends on the measurement frequency. Such measurements include low-frequency noise, conductance, frequency-dependent charge pumping, and others. The valence band hole tunnel times are longer than for electrons due to the higher effective mass and barrier height. Tewksbury and Lee give a more detailed discussion of tunneling [18].

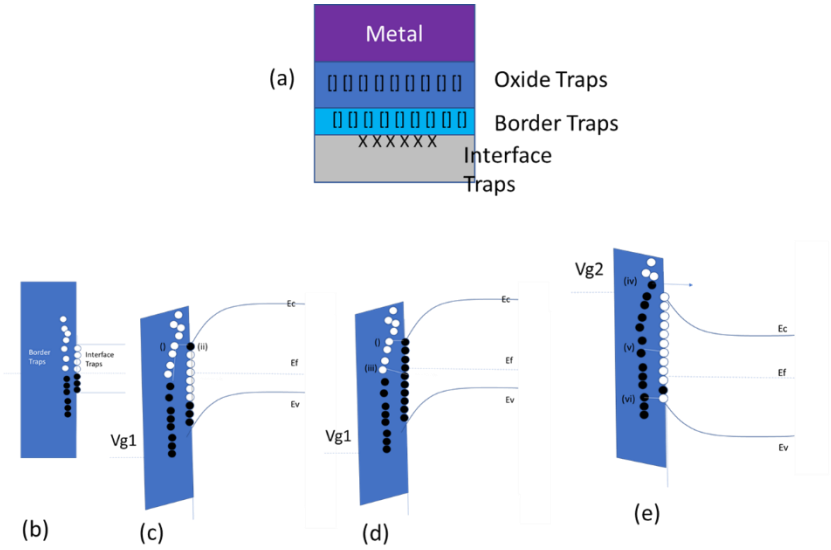

Fig.4: Schematic of oxide, border, and interface traps, (b) flatband, (c) capture of electrons by interface traps and tunneling of electrons to border traps from conduction band, (d) border and interface trap occupied by electrons (e) electron tunneling from border traps. The solid circles represent occupied and the open circles unoccupied traps.

Tunneling from the conduction band into border traps was questioned, as measurements did not support energy dissipation in the oxide [19]. Tunneling from interface traps is a two-step process: the electron must be captured from the conduction band before it can tunnel [20]. The capture time is:

$$\tau_C = \frac{1}{\sigma_n v_{th} n} \tag{4}$$

where s_n is the capture cross section, v_{th} the thermal velocity and n the inversion electron density. For strong inversion $n=10^{18}$-10^{19} cm^{-3} and using $s_n=10^{-16}$ cm^2 and $v_{th}=10^7$ cm/s, $t_c=10^{-9}$-10^{-10} s. Since the capture and tunnel processes proceed in series, to first order the time constant is:

$$\tau_{it} = \tau_C + \tau_t$$

and the tunnel time constant dominates for all but the shallowest border traps [1].

3.2 Capacitance-Voltage (C-V)

Capacitance-voltage measurements have played an important role in MOS characterization. They can be found in some of the earliest MOS-related papers. Frankl, in 1961, proposed the use of MOS capacitor CV curves to analyze such devices [21]. In 1962, Terman used C-V measurements to determinee surface state densities [22]. One of the first comprehensive papers was by the Fairchild group in 1964, the same group that played a large role in understanding and developing MOS technology [23]. Fig. 5 shows one of those early C-V curves. Barrier heights for various gate metals were characterized with C-V measurements by the same group [24]. A good early overview of the variety of material/device parameters that can be determined from C-V and C-t measurements is given by Zaininger and Heiman [25]. And, of course, the entire MOS capacitor field is very well covered in the well-known book by Nicollian and Brews [26].

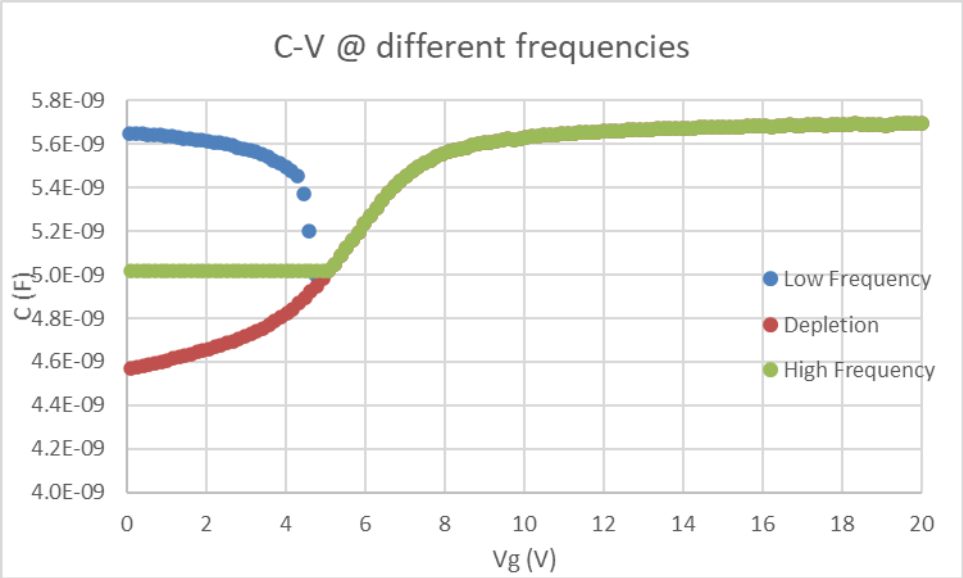

Fig. 5: Capacitance-voltage characteristics of an MOS capacitor. Lines: experiment, dots: theory. NA=1.45x1016 cm-3, tox=200 nm.

The MOS diode is affected by charges in the oxide and traps at the SiO_2-Si interface. The basic classification of these traps and charges are shown in Fig. 6 [27].

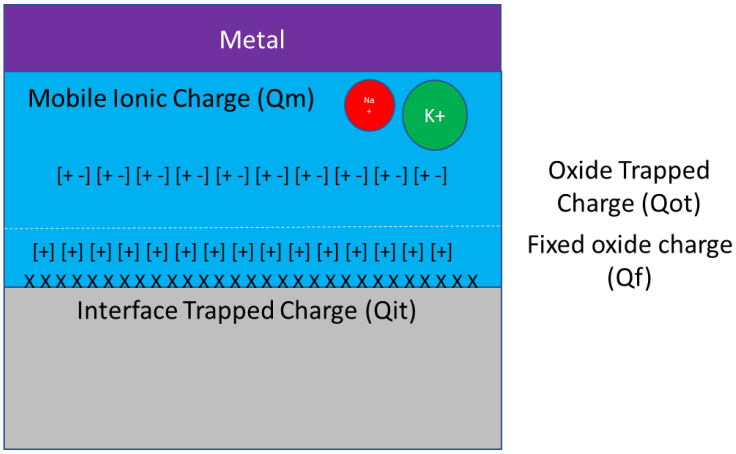

Fig. 6: Terminology for the charges associated with thermally oxidized silicon

They are the interface-trapped charge, fixed-oxide charge, oxide trapped charge, and mobile ionic. Interface-trapped charges Q_{it} are due to the SiO_2-Si interface properties and dependent on the chemicsil composition of this interface. The traps are located at the SiO_2-Si interface with energy states in the silicon forbidden bandgap. The interface trap density, i.e., number of interface traps per unit area and per eV, is orientation dependent. In ⟨100⟩ orientation, the interface trap density is about an order of magnitude smaller than that in ⟨111⟩ orientation. Present-day MOS diodes with thermally grown silicon dioxide on silicon have most of the interface-trapped charges passivated by low-temperature (450°C) hydrogen annealing. The value of $Q_{it/q}$ for ⟨100⟩-oriented silicon can be as low as 10^{10} cm^{-2}, which amounts to about one interface-trapped charge per 10^5 surface atoms. For ⟨111⟩- oriented silicon, $Q_{it/q}$ is about 10^{11} cm^{-2}.

The fixed charge Q_f is located within approximately 3 nm of the SiO_2-Si interface. This charge is fixed and cannot be charged or discharged over a wide variation of surface potential ψ_s. Generally, Q_f is positive and depends on oxidation and annealing conditions and on silicon orientation. It has been suggested that when the oxidation is stopped, some ionic silicon is left near the interface. These ions, along with uncompleted silicon bonds (e.g., Si-Si or Si-O bonds) at the surface, may result in the positive interface charge Q_f. Q_f can be regarded as a charge sheet located at the SiO_2-Si interface. Typical fxedoxide charge densities for a carefully treated $Si0_2$-Si interface system are about 10^{10} cm^{-2} for a ⟨100⟩ surface and about 5 x $10^{10}cm^{-2}$ or a ⟨111⟩ surface. Because of the lower values of Qit and Q_f, the ⟨111⟩ orientation is preferred for silicon MOSFETs. The oxide-trapped charges Q_{ot}, are associated with defects in the silicon dioxide. These charges can be created, for example, by X-ray radiation or high-energy electron bombardment. The traps are distributed inside the oxide layer. Most of process-related Q_{ot} can be removed by low-temperature annealing. The mobile ionic charges Qm such as sodium or

other alkali ions, are mobile within the oxide under raised-temperature (e.g., >100 °C) and high-electric field operations. Trace contamination by alkali metal ions may cause stability problems in semiconductor devices operated under high-bias and high-temperature conditions. Under these conditions mobile ionic charges can move back and forth through the oxide layer and cause shifts ofthe CV curves along the voltage axis. Therefore, special attention must be paid to the elimination of mobile ions in device fabrication. The charges are the effective net charges per unit area in C/cm^2. We now evaluate the influence of these charges on the flat-band voltage. Consider a positive sheet charge per unit area, Q_0 within the oxide, as shown in Fig. 7 [27].

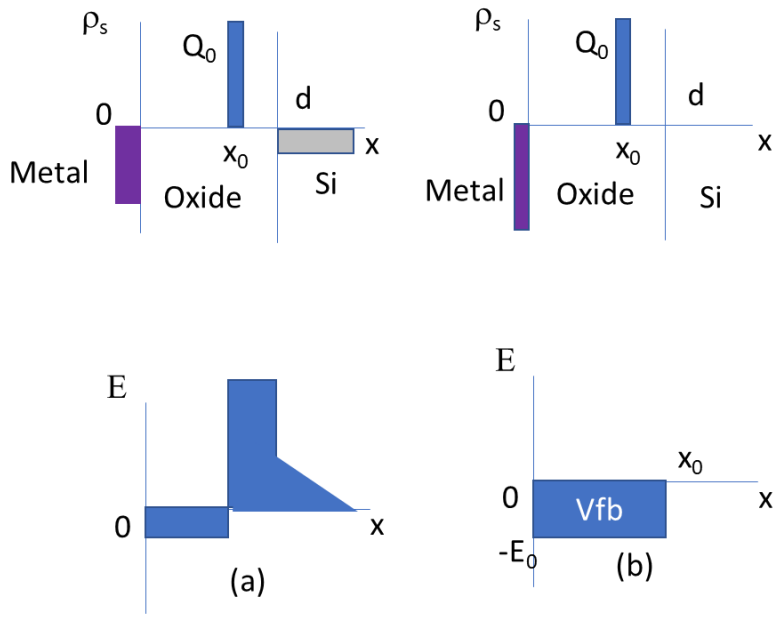

Fig. 7: Effect of a sheet charge within the oxide.2 (a) Condition for V, = 0. (b) Flat-band condition.

This positive sheet charge will induce negative charges partly in the metal and partly in the semiconductor as shown in the upper part of Fig. 7a. The resulting field distribution, obtained from integrating Poisson's equation once, is shown in the lower part of Fig. 7a where we have assumed that there is no work function difference, or $q\phi ms = 0$. To reach the flat-band condition (i.e., no charge induced in the semiconductor), we must apply a negative voltage to the metal, as shown in Fig. 7b. As the negative voltage increases, more negative charges are put on the metal and thereby the electric-field distribution shift downward until the electric field at the semiconductor surface is zero. Under this condition the area contained under the electric-field distribution corresponds to the flat-band voltage V_{FB}:

$$V_{FB} = -\mathcal{E}_o x_o = -\frac{Q_o}{C_o}\frac{x_o}{d} \tag{5}$$

The flat-band voltage is, thus, dependent on both the density of the sheet charge Q_0 and its location x_0, within the oxide. When the sheet charge is located very close to the metalthat is , if $x_0 = 0$ it will induce no charges in the silicon and therefore have no effect on the flat-band voltage. On the other hand, when Q_0 is located very close to the semiconductor-$x_0 = d$, such as the fixed-oxide charge Q_f, it will exert its maximum influence and give rise to a flat-band voltage

$$V_{FB} = -\frac{Q_o}{C_o} \tag{6}$$

For the more general case of an arbitrary space charge distribution within the oxide, the flat-band voltage is given by

$$V_{FB} = -\frac{1}{C_o}\left[\frac{1}{d}\int_0^d x\rho(x)dx\right] \tag{7}$$

where ρ(x) is the volume charge density in the oxide. Once we know ρ_{ot}(x), the volume charge density for oxide-trapped charges, and ρ_m(x), the volume charge density for mobile ionic charges, we can obtain Qot and Qm, and their corresponding contribution to the flatband voltage:

$$Q_{ot} = \frac{1}{d}\int_0^d x\rho_{ot}(x)dx \tag{8}$$

$$Q_m = \frac{1}{d}\int_0^d x\rho_m(x)dx \tag{9}$$

If the value of the work function difference qϕms, is not zero and if the value of the interface-trapped charges is negligible, the experimental capacitance-voltage curve will be shifted from the ideal theoretical curve by an amount:

$$V_{FB} = \phi_{ms} - \frac{Q_f + Q_m + Q_{ot}}{C_o} \quad (10)$$

The curve in Fig. 9a shows the C-V characteristics of an ideal MOS diode. Due to nonzero qϕms, Q_f, Q_m, or Q_{ot}, the C-V curve will be shifted by an amount given by Eq. 10. The parallel shift of the C-V curve is illustrated in Fig. 8(b). If, in addition, there are large amounts of interface-trapped charges, the charges in the interface traps will vary with the surface potential. The C-V curve will be displaced by an amount that itself changes with the surface potential. Therefore, Fig. 8 (c) is distorted as well as shifted because of interface-trapped charges [27].

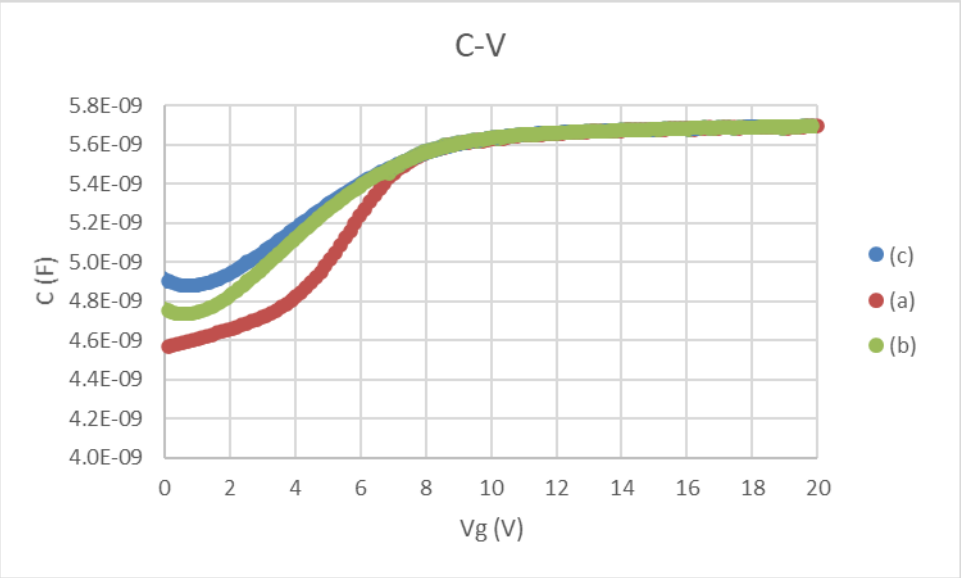

Fig. 8: Effect of a fixed oxide charge and interface traps on the C-V characteristics of an MOS diode.

3.2.1 High and Low Frequency C-V

The previous paragraph discussed the possible charges present at the interface between oxide and semiconductor and inside the oxide, called "traps" and which can be measured through C-V measurements. These interface traps can be classified as: *interface traps* and *border traps*. High and low frequency C-V measurements, as we will see in this section, are useful for determining these traps and calculating the density of the states at the interface.

a) ***Interface Traps***

MOS capacitance measurements are made at high and low frequencies. Low-frequency C-V measurements are referred to as quasi-static measurements first demonstrated in 1968-7050 to measure interface traps. The effects of interface traps on C-V_G curves to illustrate what one may expect have been calculated. Fig. 9(a) shows the assumed interface trap density as a function of surface potential for these calculations. This distribution approximates the interface trap density distribution at the SiO_2/Si interface with $D_{it,min}$ at midgap. Fig. 9(b) shows the surface potential versus gate voltage behavior without and with interface traps. The discontinuity at $\varphi_s \approx 0.4$ V is the result of the assumption of D_{it} being donors in the upper half and acceptors in the lower half of the band gap. In real devices there is a more gradual transition. The interface trap density results in a "stretch-out" of the φs-V_G characteristic because charged interface traps lead to gate voltage shifts.[1]

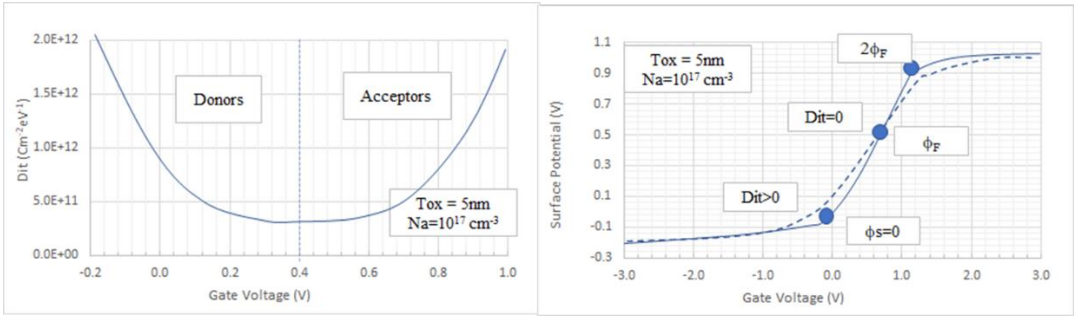

Fig. 9: (a) Interface trap distribution, (b) surface potential versus gate voltage. NA=10^{17} cm^{-3}, tox=5 nm, Dit,min=2.4x10^{-11} $cm^{-2}eV^{-1}$

Fig. 10 shows the effect of D_{it} on (a) low- and (b) high-frequency C-V_G curves. It is assumed that Q_{ox}=0 in these calculations in order to bring out the effects of interface traps. Q_{ox} would lead to a parallel shift of the curves along the V_G axis. It is assumed that at high frequencies, the interface traps do not follow the gate voltage AC and does not find it with a capacitance and the "out" is solely due to the effect of D_{it} on V_G. The acceptor states in the upper half of the band gap lead to a positive gate voltage shift in inversion whereas the donor states give the negative V_G shift in accumulation and depletion. For the low-frequency curve, on the other hand, there is both "stretch-out" and additional capacitance, as the interface traps are assumed to be able to follow the AC gate voltage. Fig. 10 (c) shows experimental data before and after gate oxide stress, with the stress generating D_{it}. Note how the curve broadens as predicted shifting to the left in region A and to the right in region B indicative of amphoteric interface traps. This curve indicates donor states over slightly more than the lower half of the band gap [1].

The basic theory, developed by Berglund, compares a low-frequency C-V curve with one free of interface traps [28]. The latter can be a theoretical curve, but is usually an hf C-V curve determined at a frequency where interface traps are assumed not to respond. "Low frequency" means that interface traps and minority carrier inversion charges must be able to respond to the measurement AC probe frequency.

The interface trap density is determined from the lf capacitance data according to:

$$D_{it} = \frac{1}{q^2}\left(\frac{C_{ox}C_{lf}}{C_{ox} - C_{lf}} - C_s\right) \tag{11}$$

where C_{it} is related to the interface trap density D_{it} by $D_{it}=C_{it}/q^2$. We should mention here that most publications use $C_{it}=qD_{it}$. With D_{it} in the usual units of $cm^{-2}eV^{-1}$ and q in Coul, the units for Cit in this expression are F/cm^2Coul, suggesting that the correct definition should be $C_{it}=q^2D_{it}$. A simplified approach, proposed by Castagné and Vapaille, uses measured lf and hf C-V curves as [29]

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{\frac{C_{lf}}{C_{ox}}}{1 - \frac{C_{lf}}{C_{ox}}} - \frac{\frac{C_{hf}}{C_{ox}}}{1 - \frac{C_{hf}}{C_{ox}}}\right) \tag{12}$$

Equation (12) gives D_{it} over only a limited range of the band gap, typically from the onset of inversion, to a surface potential towards the majority carrier band edge where the AC measurement frequency equals the inverse of the interface trap emission time constant [1].

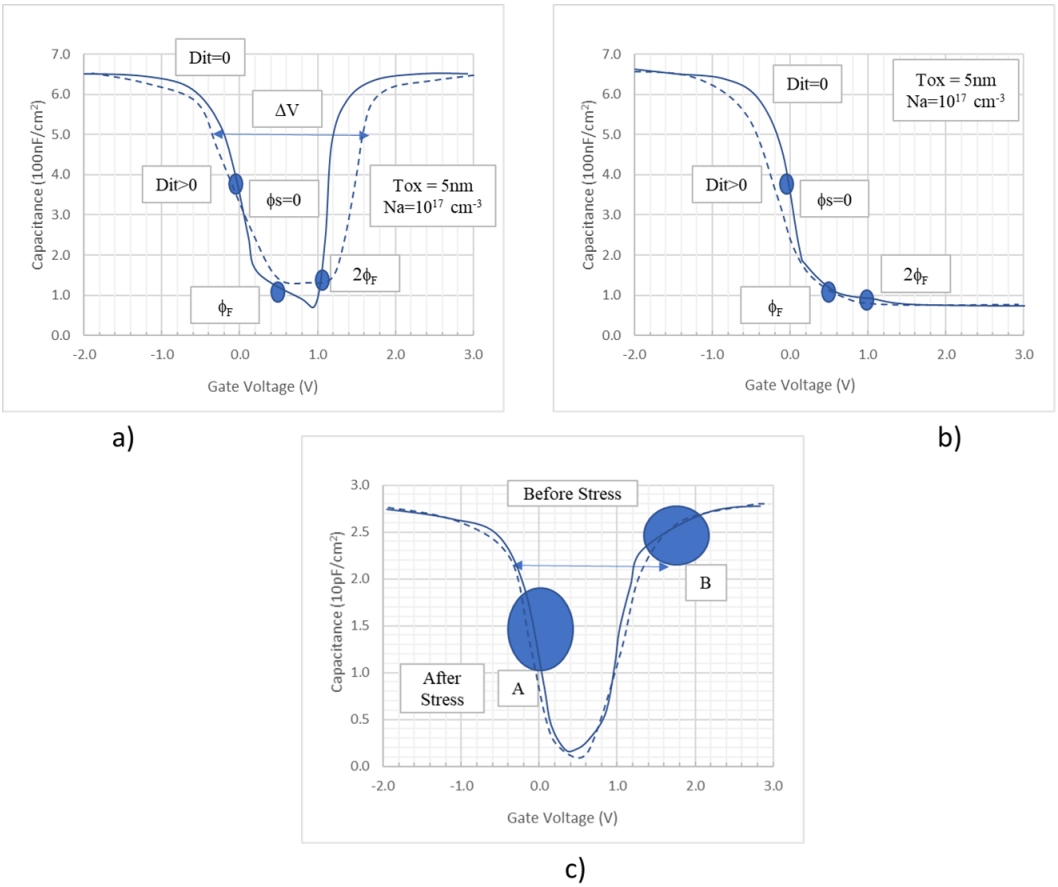

Fig.10: Theoretical (a) low-frequency, (b) high-frequency C-V_G (Dit,min=2.4x10^{11} cm^{-2}eV^{-1}), (c) experimental data. φs is the surface potential.

b) ***Border Traps***

C-V_G curves can also be used to gain information on oxide trapped charge. For example, the "hump" sometimes observed in quasi-static data, illustrated in Fig. 11, has been attributed to electron tunneling from the channel into border traps [30]. This device has an oxide/nitride/oxide gate insulator and the trap density in the nitride or at the nitride/oxide interface is increased by hot carrier stress. Traps within several kT about the trap energy participate during the AC measurement, leading to an additional capacitance. Its magnitude depends on the measurement frequency. Lower frequencies lead to higher "humps" as carriers can tunnel deeper into the insulator.

High-frequency C-V_G measurements also show a capacitance increase for accumulated nsubstrate MOS capacitors and inverted n-MOSFETs with Hf-based insulators, attributed to

tunneling from the substrate into border traps [31]. It appears that the charge carriers tunneling through the thin interfacial oxide must be electrons due to their smaller effective mass and barrier height compared to holes. The dielectric capacitance increases at low frequencies, typically 1 – 100 kHz, has been proposed as a frequency- and voltage-dependent border trap capacitance C_{bt} in parallel with the interface trap capacitance C_{it}. C_{bt} contributes to the measured capacitance only if the border trap charging/discharging

can follow the applied ac signal. The frequency/voltage dependence of C_{bt} yields the tunneling distance from the Si substrate and trap energy depth in the HfO_2. Related to C–V_G measurements are C–t measurements, commonly used to determine the generation lifetime [32]. In this technique, the MOS-C is pulsed into deep depletion and subsequently relaxes to its equilibrium state through electron-hole pair generation. The generation lifetime so determined is a measure of the substrate purity. This technique is well understood but irregularities appear when the flatband voltage changes during the recovery time. This can occur as a result of carrier injection from the semiconductor into the insulator as, for example, in H_fO_2. An initial capacitance undershoot has been attributed to electron tunneling into H_fO_2 traps and interface trap generation [33].

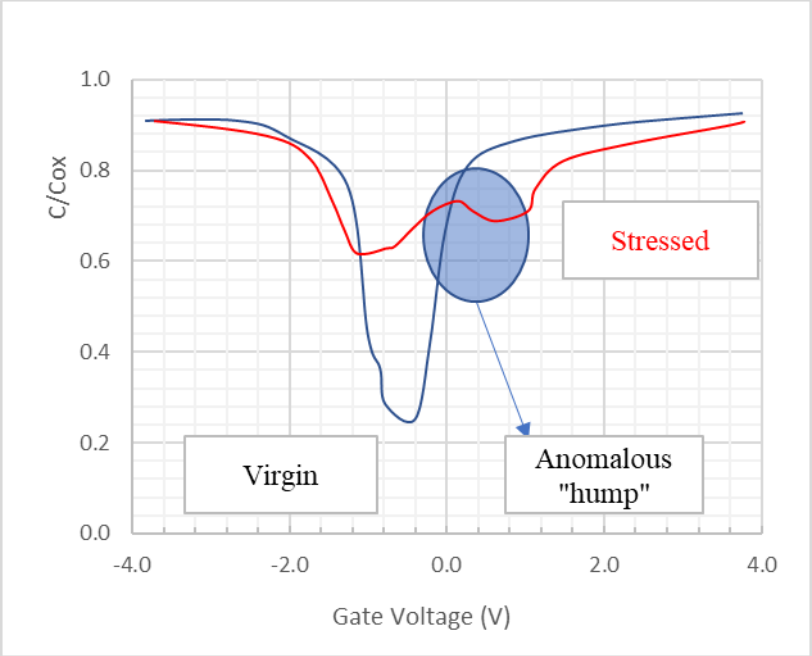

Fig.11: MOSFET normalized capacitance before and after hot carrier injection of 10^{16} electrons/cm^2.

In order to obtain a complete C-V characteristic of a MOS capacitor, a gate voltage V_G has to be swept in a staircase fashion (Fig. 12) from a sufficiently negative to a suffieciently positive bias. In this way the semiconductor moves from depletion to accumulation or reverse. V_G is swept much slower than the period of the applied AC signal, T>>2p/w [35].

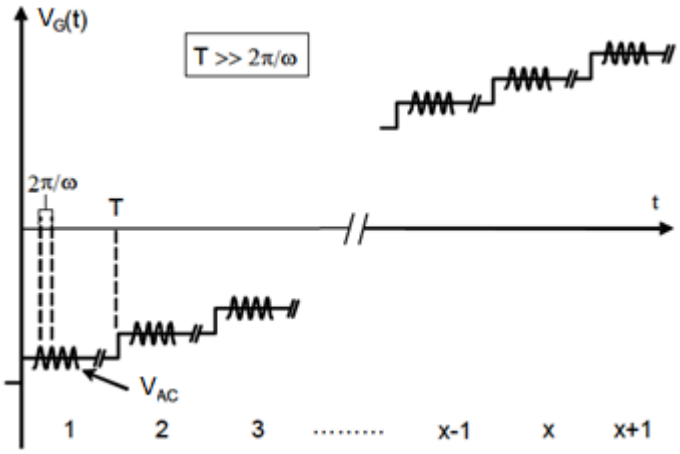

Fig.12: The time dependence of the applied gate bias. T is the integration time at one step x, and 2π/ω is the probe frequency

A schematic plot of the capacitance as a function of the gate bias for a n-type MOS capacitor is given in Fig 13.

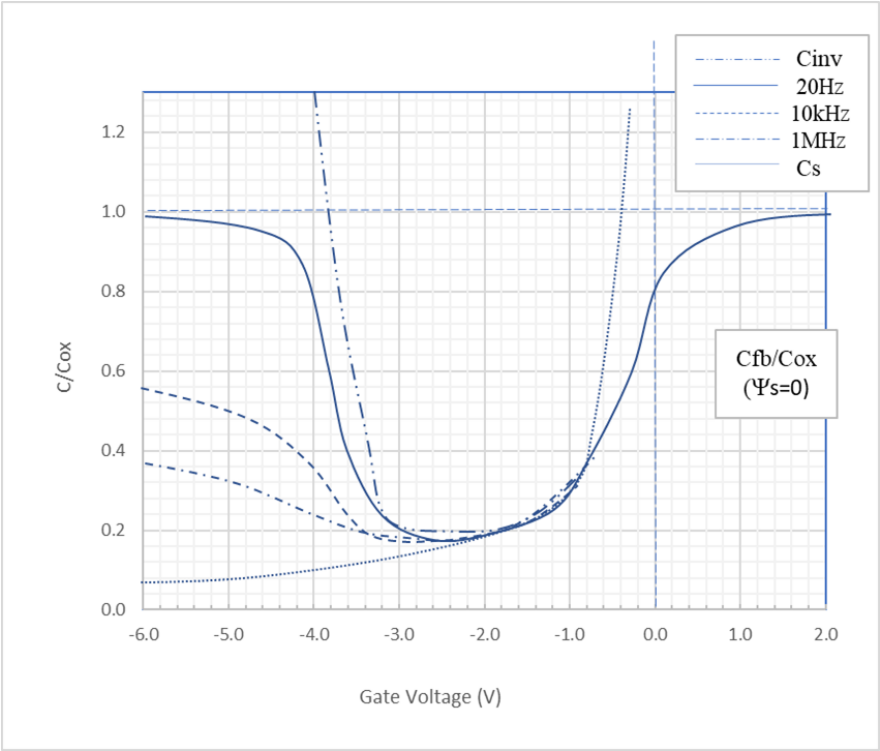

Fig.13: C-V characteristic of a n-Type 3C-SiC MOS capacitor

At low frequencies dashed and dashed-dot-dot lines correspond to the 10 kHz and 1 MHz probing signal, respectively[35].

3.2.2 High-Low frequency method

This method is based on two C-V measurements, one at a high frequency, so that the interface states cannot follow the AC signal, and the other at a sufficiently low frequency, so that interface traps response is immediate [36]. To determine the low frequency capacitance, refer to the Fig. 14(a).

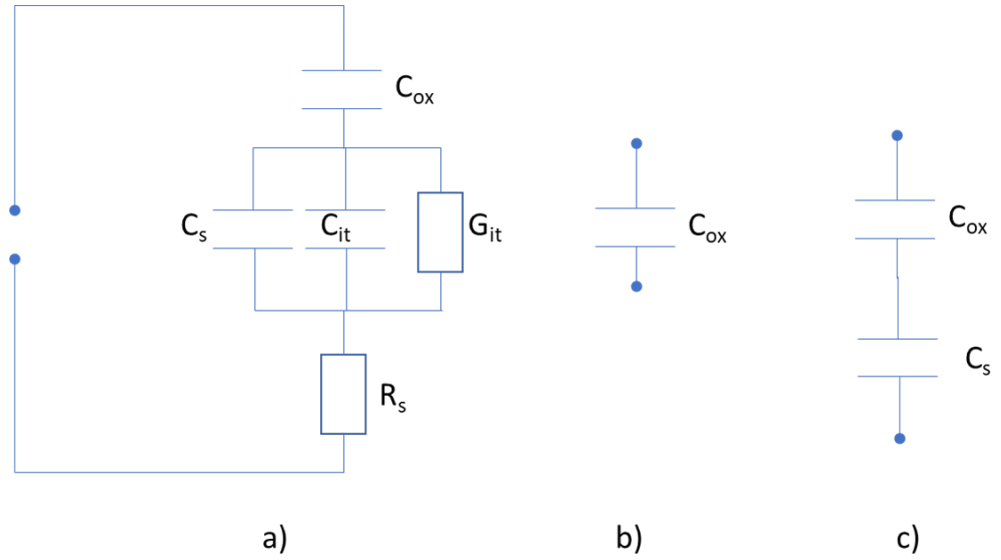

Fig.14: Equivalent circuit of the MOS capacitance for the different operating regions: (a) general equivalent circuit with all contributions; (b) accumulation/inversion at low frequency; (c) inversion at high frequency.

Since the traps are in equilibrium with the AC signal, they will contribute to the measured low frequency capacitance with an additional term C_{it}. The total capacitance of the MOS system is given by [36]:

$$\frac{1}{C_{LF}} = \frac{1}{C_{ox}} + \frac{1}{C_{it} + C_s} \tag{13}$$

The low frequency capacitance is usually obtained by “quasi-static” measurements

[37], measuring the displacement current (and not the MOS impedance), in response to a slowly varying DC gate voltage [38]. From Eq. (13) D_{it} is expressed by [36]:

$$D_{it} = \frac{1}{q}\left[\frac{1}{C_{LF}} - \frac{1}{C_{ox}}\right]^{-1} - \frac{C_s}{q} \tag{14}$$

The semiconductor capacitance C_s is obtained from the high frequency measurement, solving the relation from Terman method [citare Terman]:

$$C_{HF} = \frac{C_{ox}C_s}{C_{ox} + C_s} \tag{15}$$

Solving (15) for C_s:

$$C_s(V_G) = \left(\frac{1}{C_{HF}(V_G)} - \frac{1}{C_{ox}}\right)^{-1} \tag{16}$$

Substituing Eq. (16) in Eq. (15) yields

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox} - C_{LF}} - \frac{C_{HF}}{C_{ox} - C_{HF}}\right) \tag{17}$$

The trap position in the bandgap is obtained with the following equation from Terman method:

$$\frac{E_C - E_T(V_G)}{q} = \frac{E_g}{2q} + \psi_s(V_G) - \phi_B \tag{18}$$

knowing the VG− s relationship. A direct way to obtain this, from the low frequency capacitance only, is the calculation of the "Berglund's integral" [39]:

$$\psi_s(V_G) = \Delta + \int_{V_{G1}}^{V_G}\left[1 - \frac{C_{LF}(V_G)}{C_{ox}}\right]dV_G \tag{19}$$

where V_{G1} is an arbitrary voltage value. The determination of the integration constant is very important for the exact estimation of trap energy position and density: a wrong value can severely shift the position of the resulting D_{it} plot along the energy axis, with consequent over- or underestimation of the Dit density in the accessible portion of the bandgap [40]. The lower

integration limit of Eq. (19) can be set to a known voltage value, usually the flatband voltage V_{FB}. After integrating Eq. (19) from V_{FB} to accumulation and from V_{FB} to inversion, the resulting $V_G - \psi_s$ curve must be shifted so that $\psi_s(V_{GB}) = 0$, which is the definition of flatband voltage. The constant D corresponds to this shift along the vertical axis.

3.2.3 Determination of the Surface Potential

It is important to accurately determine the surface potential ψ_s, because it determines the energy position of the interface states and is required in all of the characterization techniques described below. The determination of the surface potential is critical for SiC because the interface state density usually exhibits a sharp increase near the band edge, especially on SiC (0001)[41]. According to a theory in MOS physics, the surface potential (ψ_s) can be calculated from the low-frequency C–V curves using [42]:

$$\psi_s(V_G) = \int \left(1 - \frac{C_{LF}}{C_{ox}}\right) dV_G + A \tag{20}$$

where C_{LF} is the low-frequency (usually quasi-static) capacitance and V_G is the gate voltage. Here, a certain ambiguity exists in the determination of the integration constant (A). For example, this constant is often determined based on the flat-band capacitance in high-frequencymeasurements, by assuming that ψ_s = 0 (flat band) when the high-frequency capacitance C_{HF} equals the ideal flat-band capacitance (C_{FB})[41].

This is correct only when the high-frequency capacitance does not include any contribution from the interface states. If the probe frequency is not high enough, the flatband capacitance contains a component

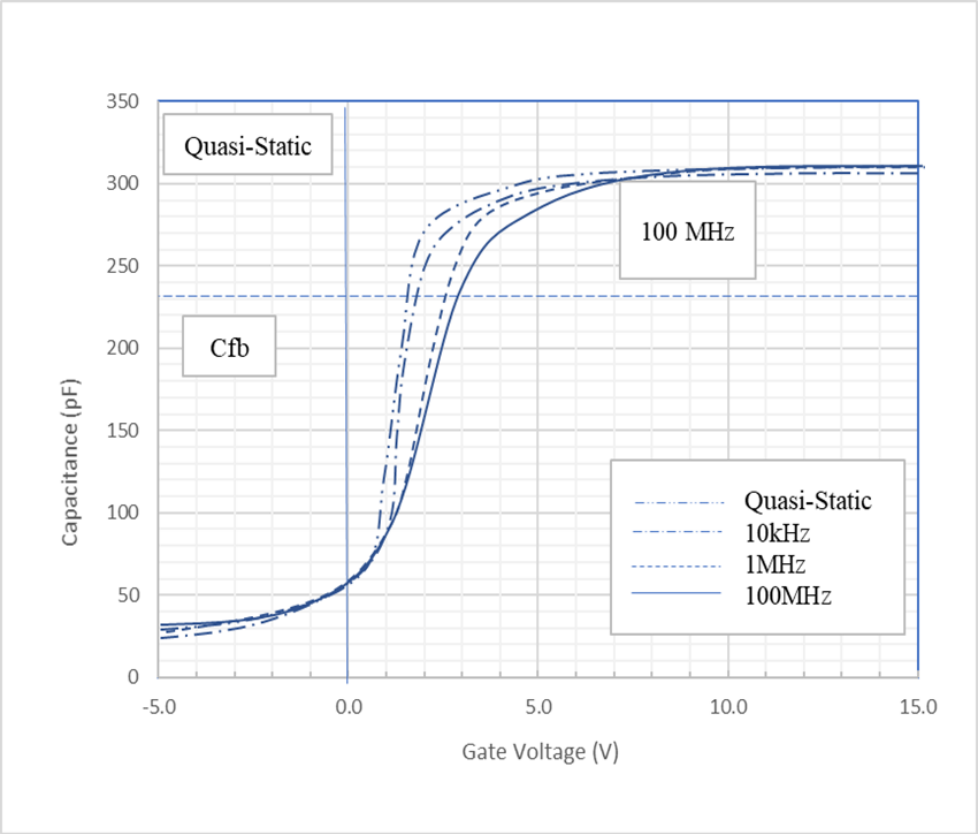

Fig.15: High-frequency C–V curves of aMOS capacitor on n-type 4H-SiC(0001) at various probe frequencies (the influence of parasitic impedance at very high frequency was calibrated).

from the fast interface states, leading to an error in the surface potential. This method results in a relatively large error of 0.06–0.15 eV when a high density of fast interface states exists, as is the case in SiC MOS structures. Some evidence for this is shown in Fig. 15, where the high-frequency C–V curves of a MOS capacitor on n-type 4H-SiC (0001) at various probe frequencies are shown (The influence of parasitic impedance at very high frequency was calibrated). There exists clear frequency dispersion in the C–V curves, and the voltage at which the ideal flat-band capacitance C_{FB} is obtained clearly depends on the probe frequency. This result suggests that some interface states respond to such high frequency, and that the interface-state capacitance is involved in the high-frequency capacitance. Taking account of the C_{ox} and Z values, $C_D + C_{IT}$ can be determined by using the equivalent circuit shown in Fig. 14 (a). On the other hand, the surface potential ψ_s (V_G) can be obtained using Equation 20, except for the integration constant A. The integration constant A can be uniquely determined, as shown in Fig. 16, where $1/(C_D + C_{IT})^2$ is plotted against ψ_s. In Fig. 16, a linear correlation is evident for sufficiently negative ψ_s (in the depletion region). At a sufficiently high frequency, and upon

depletion, the interface states do not respond and no inversion carriers are generated at the SiC MOS interface. Therefore, $C_D + C_{IT}$ can be approximated as the depletion capacitance (C_{dep}), and a linear relationship can be established between $1/(C_D + C_{IT})^2$ and ψ_s [41]:

$$\frac{1}{(C_D + C_{IT})^2} \approx \frac{1}{C_{dep}^2} = -\frac{2\psi_s}{\varepsilon_s q N_D S^2} \tag{21}$$

where ε_s is the dielectric constant of the semiconductor, N_D the donor density, and S the area of the gate electrode. Based on Equation 21, the constant A can be determined so that extrapolation of the straight line should intersect the origin of the plot, as shown in Fig. 16 [43]. The donor density is simultaneously determined from the slope of the plot.

3.2.4 C− ψ_s Method

This method is relatively new and was developed by Yoshioka et al. [44]. The determination of the integration constant D in Eq. (19) is of crucial importance for the correct determination of interface states density. This constant is usually determined from the flatband capacitance measured at high frequency, assuming that the interface states at this frequency do not contribute to V_{FB} [36]. This might be not true, especially for SiC, and an error could be introduced in the calculation of D. With the C− ψ_s method, this constant is determined from the depletion capacitance, while the concentration of interface states results from a comparison between the quasi-static and the theoretical C-V curves.

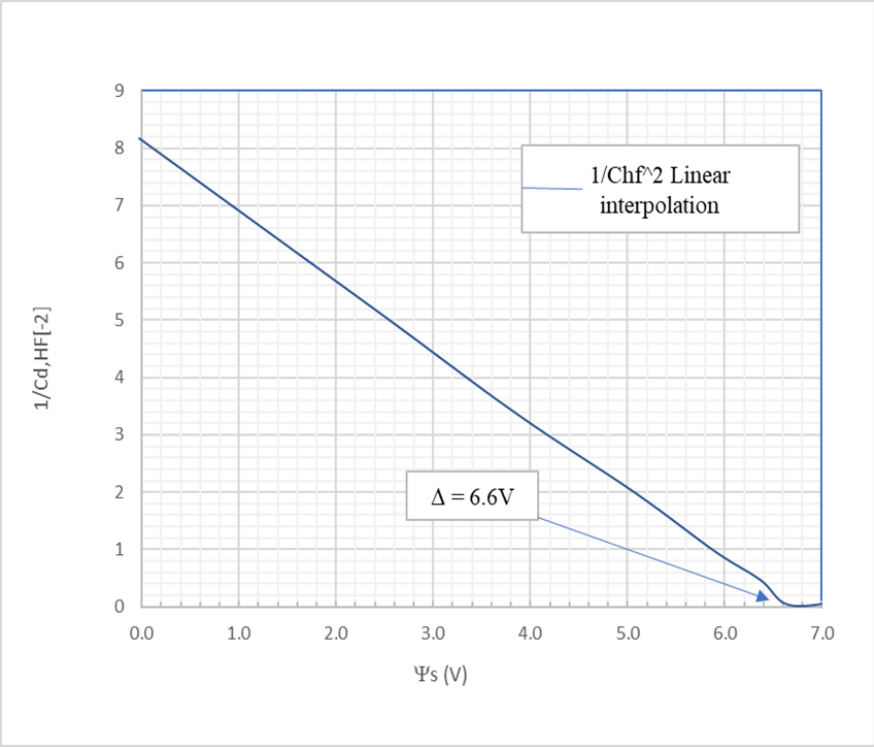

Fig. 16: Graphical explanation for the method to determine the additive constant D

When the MOS capacitor is biased in depletion and at high frequency, there is no generation of minority carriers at the SiC MOS interface and the interface states are not able to respond. Therefore the capacitance C_s + C_{it} (Fig. 14) can be approximated by the (deep) depletion capacitance C_d. We know that for sufficiently high gate voltages (in depletion) a linear relationship holds between the surface potential and the depletion capacitance [32]:

$$\frac{1}{C_d^2} \approx \frac{1}{(C_d + C_{it})^2} = -\frac{2\psi_s}{qA^2\varepsilon_{SiC}N_D} \tag{22}$$

where A is the area of the MOS capacitor. The constant D is determined so that the extrapolation of the straight line from Eq. (22) intersects the origin of the plot in Fig.16. The capacitance C_s+C_{it} must be extracted from the measured capacitance with the equivalent circuit of Fig. 14(a). The donor concentration is determined from the slope of Eq. (22) [36].
The interface states density is extracted from a comparison of the quasi-static capacitance and the calculated theoretical capacitance, in analogy to the High-Low Frequency method:

$$D_{it} = \frac{C_{ox}}{q}\left(\frac{C_{LF}}{C_{ox} - C_{LF}} - C_{D,theory}\right) \tag{23}$$

3.2.5 Conductance Method

The conductance method was firstly proposed by Nicollian and Brews [Nic-67]. It describes the relationship between measured admittance of the MOS capacitor and the interface trap properties [35]. Impedance measurements are performed as a function of voltage V_G and frequency w = 2pf in order to extract the real and imaginary components of the parallel admittance $Y_P = G_P + jwC_P$ of Fig. 4.6(b)[36]. Both contain information on the interface states concentration and can be expressed by Lehovec equations for a continuous distribution of interface states in energy throughout the semiconductor bandgap [45].

The MOS capacitor can be compared to an equivalent circuit as shown in Fig. 17 in which is represented the serial connection of the oxide dielectric C_{ox} with a parallel circuit formed by the space charge region capacitance C_{sc}, interface trap capacitance C_{it} and the conductance components G_n and G_p, which take into account the charge exchange of interface traps with the condution band (C_B) and with the valence band (V_B)[35].

With this description is possible to determinate the conductance.

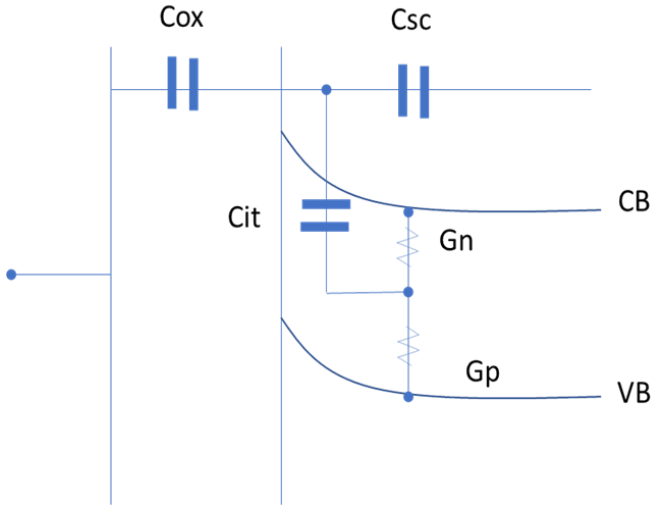

Fig.17: Equivalent circuit of a MOS capacitor. Only one energy level of the interface traps is considered

$$C_P = C_s + C_{it} = C_s + qD_{it}\frac{\arctan(\omega\tau)}{\omega\tau} \tag{24}$$

$$\frac{G_P}{\omega} = G_{it} = \frac{qD_{it}}{2}\frac{ln(1+\omega^2\tau^2)}{\omega\tau} \tag{25}$$

where $t_{it} = C_{it}/G_{it} = C_{it}R_{it}$ is the trap emission time constant. Capture and emission of carriers occur within some k_BT eV around the Fermi level position (ruled by the DC gate bias) and their frequency response depends on the trap time constant The maximum loss occurs when the trap is in resonance with the applied AC signal, that is when $\omega\tau_{it} \approx 2^2$. The value G_P/w at this maximum is [42]

$$D_{it} \approx \frac{2.5}{qA}\left(\frac{G_P}{\omega}\right)_{max} \tag{26}$$

Thus, D_{it} is determined from the maximum of the G_P/w curve, while t_{it} from the location of this peak on the w-axis. This procedure is repeated for a different gate voltage, in order to move the Fermi level to a different position in the bandgap. The energy position is calculated again with Eq. (4.6), knowing the $V_G - \psi_s$ relationship.

The method is valid in depletion-weak inversion regions of the C-V curve [42]. Eq. (24) and Eq. (25) predict narrower conductance curves with respect to the experimental ones: they do not take into account the interface trap time constant dispersion caused by surface potential fluctuations on the entire capacitor area [36]

These fluctuations can arise from non-uniformities in the oxide charge, concentration of interface traps, and doping density at the interface, or as in the case of SiC, from the larger bandgap comprising traps with a large variation of cross sections [46].

When these fluctuations are taken into account, Eq. (24) and Eq. (25) can be rewritten as [36]:

$$C_{it} = q\int_{-\infty}^{\infty} D_{it}(v_s)\frac{\arctan(\omega\tau)\,(v_s)}{\omega\tau(v_s)}P(v_s)\,dv_s \tag{27}$$

And:

$$\frac{G_{it}}{\omega} = \frac{q}{2}\int_{-\infty}^{\infty} D_{it}(v_s)\frac{ln\left(1+\omega^2\tau^2(v_s)\right)}{\omega\tau(v_s)}P(v_s)\,dv_s \tag{28}$$

where both expression are in [F/cm^2]. $P(v_s)$ is the probability that the band bending is v_s, and is given by the normal probability distribution function defined as follows:

$$P(v_s) = \frac{1}{\sqrt{2\pi\sigma_s^2}} e^{\left(\frac{(v_s-\bar{v}_s)^2}{2\sigma_s^2}\right)} \tag{29}$$

Where $\bar{v}_s = (1/k_B T)\overline{\psi_s}$ is the is the normalized mean and s_s the standard deviation of the surface potential. Substituting $\eta = v_s - \bar{v}_s$obtain the following equations describing the interface traps capacitance and conductance (for an n-type substrate, t= t_n)

$$C_{it} = \frac{qD_{it}(v_s)}{\omega\tau(v_s)} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} e^{\eta} \arctan(\omega^2\tau^2(v_s)e^{-\eta})\, e^{-\frac{\eta^2}{2\sigma_s^2}} d\eta \tag{30}$$

$$\frac{G_{it}}{\omega} = \frac{qD_{it}(v_s)}{\omega\tau(v_s)} \frac{1}{\sqrt{2\pi\sigma_s^2}} \int_{-\infty}^{\infty} e^{\eta} \ln(1+\omega^2\tau^2(v_s)e^{-2\eta})\, e^{-\frac{\eta^2}{2\sigma_s^2}} d\eta \tag{31}$$

Where the measured characteristic constant t corresponds approximately to the mean band bending $\bar{v}_s$ and is given by:

$$\tau_n = \frac{1}{\sigma_n v_{thn} N_D} e^{-(\bar{v}_s)} \tag{32}$$

$$\tau_p = \frac{1}{\sigma_n v_{thp} N_A} e^{(\bar{v}_s)} \tag{33}$$

for electrons (n) and holes (p), respectively. The term $D_{it}(v_s)$ was taken out of the integrals in Eq. (27) and Eq. (28) since it does not vary greatly with vs, at least over a range equal to s_s. For a fixed applied gate bias and thus fixed $\bar{v}_s$, equations Eq. (30) and Eq. (31) describe the relations of interface traps conductance and capacitance with three parameters D_{it}, s_s and t_n, which are functions of v_s [36].

Eq. (30) and Eq. (31) describe the behavior of capacitance and conductance in the presence of interface states with surface potential fluctuations. In order to extract trap information – density D_{it}, capture cross sections $s_{n,p}$ and surface potential fluctuations s_s – the expressions above must be fitted to experimental data [47], measured varying gate bias and frequency.

In the Fig. 18 is shown the G_p/ω curves from which have been eliminated series resistance: the information on the interface traps is contained in these curves. D_{it} data is extracted only at the gate biases for which the Gp/w curves show clear peaks. In turn this restricts the bandgap energy range over which the conductance data gives sensible results. The energy range can be

shifted closer to the band edge or deeper in the bandgap by measuring at lower or higher temperature, respectively [36]. To determine the energetic position of the extracted D_{it} values, the VG− ψ_s relationship can be found from a Quasi-Static C-V measurement via Eq. (19) and subsequently applying Eq. (18). The results of this method are presented in Fig. 19 [36].

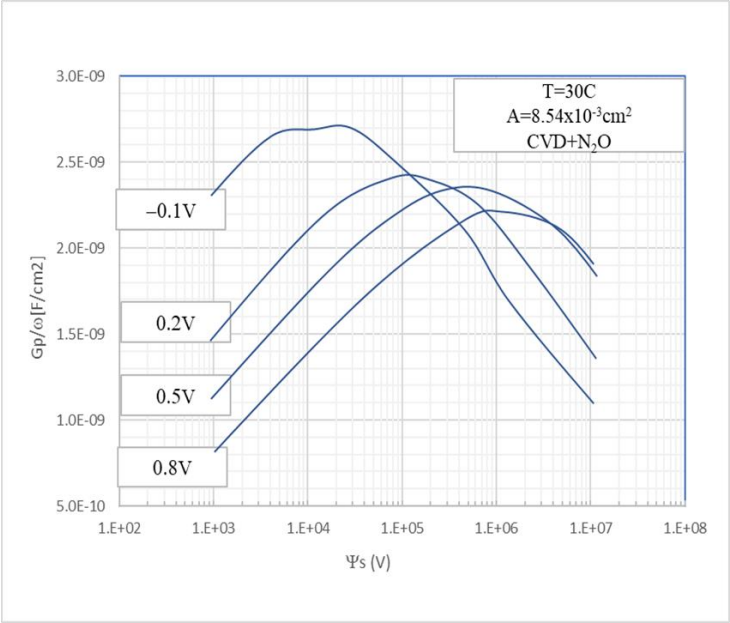

Fig.18: Conductance of interface traps (symbols) as a function of angular frequency, measured fordifferent gate voltages (only a set of these is shown for clarity). GP/w was extracted from the correctedcapacitance and conductance

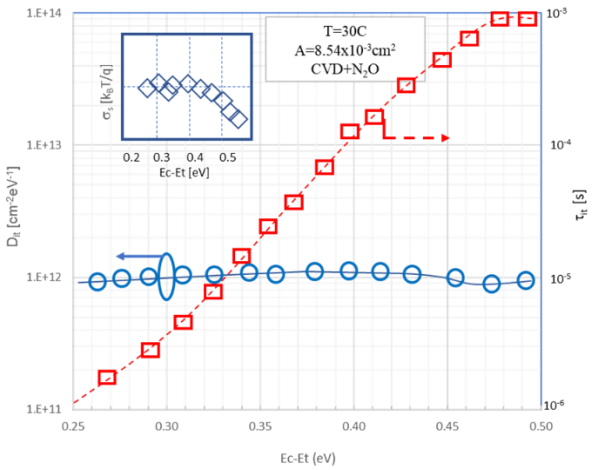

Fig.19: Interface traps parameters extracted by fitting the curves in Fig.18.

3.2.6 Bias-Temperature Stress (BTS)

In the bias-temperature stress (BTS) method the MOS device is heated to 150 to 250°C, and a gate bias to produce an oxide electric field of around 10 MV/cm is applied for 5-10 min. for any mobile oxide charge to drift to one oxide interface. The device is then cooled to room temperature under bias and a CV_G curve is measured. The procedure is then repeated with the opposite bias polarity. The mobile charge is determined from the flatband voltage shift, according to the equation [1]:

$$Q_m = -C_{ox}\Delta V_{FB} \tag{34}$$

To distinguish between oxide trapped charge and mobile charge, a BTS test is done with positive gate voltage. For oxide electric fields around 1 MV/cm mobile charge drifts, but the electric field is insufficient for appreciate charge injection. If the C-V_G curve shifts after BTS, it is due to positive mobile charge. For higher gate voltages, there is a good chance that electrons and/or holes can be injected into the oxide and mobile charge may also drift, making that measurement less definitive. For positive gate voltage, mobile charge drift leads to negative while charge injection leads to positive flatband voltage shifts [1].

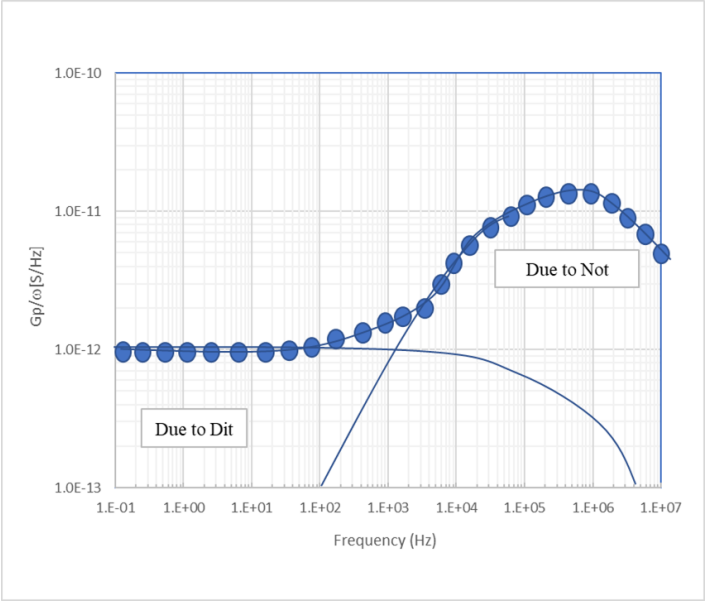

Fig.20: Gp/ω versus f for an MOS-C exhibiting a Dit peak and Nox ledge. The lines indicate the contributions from Dit=1.46x1011 cm-2eV-1 and Nox=1.3x1017 cm-3eV-1.

3.2.7 Triangular Voltage Sweep (TVS)

In the triangular voltage sweep (TVS) method the MOS device is held at an elevated, constant temperature of 200 to 300°C and the low-frequency C-V_G curve is obtained by measuring the current in response to a slowly varying ramp gate voltage.[48] TVS is based on measuring the charge flow through the oxide at an elevated temperature in response to an applied time-varying voltage. If the ramp rate is sufficiently low, the measured current is the sum of displacement and conduction current due to the mobile charge. If, at $-V_{G1}$, all mobile charges are located at the gate-oxide interface and at $+V_{G2}$ all mobile charges are located at the semiconductor-oxide interface, the mobile charge is determined by the area under the lf curve according to:

$$\int_{-V_{G1}}^{V_{G2}} \left(\frac{I}{C_{lf}} - \alpha \right) C_{ox}\, dV_G = \alpha Q_m \tag{35}$$

The hf and lf C-V curves coincide at high temperatures except for the lf "hump", due to mobile charge drifting though the oxide and illustrated in Fig.22.[49] Fig. 21(a) illustrates the effect of different mobile charge densities and 21(b) the effect of temperature. Clearly the temperature for this sample must be least 120°C for all of the mobile charge to move [1].

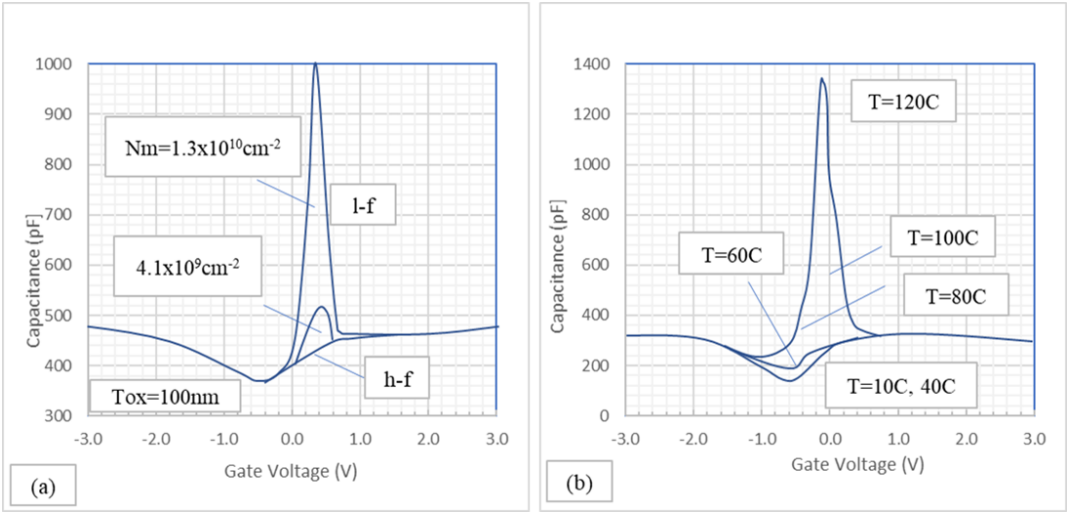

Fig.21: Clf and Chf measured at (a) T=250°C and (b) various temperatures. The mobile charge density is determined form the area between the two curves.

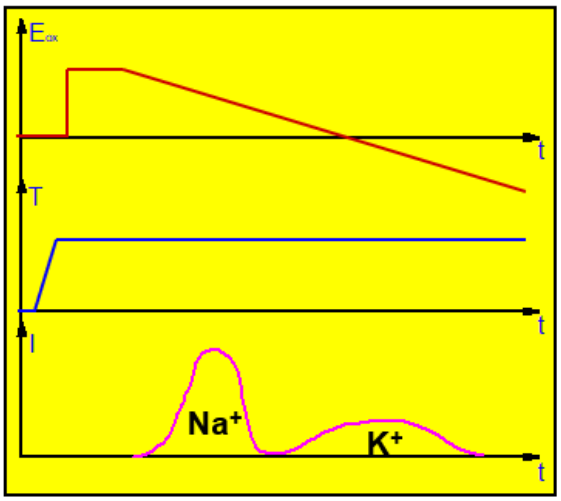

Fig.22: Ion current normalized by oxide current versus gate voltage.

Sometimes two peaks are observed in I-V_G curves at different gate voltages. These have been attributed to mobile ions with different mobilities. For an appropriate temperature and sweep rate, high mobility ions (e.g., Na+) drift at lower oxide electric fields than low-mobility ions (e.g., K+).[50] Hence, the Na peak occurs at lower gate voltages than the K peak, illustrated in Fig. 22. Such discrimination between different types of mobile impurities is not possible with the bias-temperature method. This also explains why sometimes the total number of impurities determined by the BTS and the TVS methods differ. In the BTS method one usually waits long enough for all the mobile charge to drift through the oxide [1]. If in the TVS method the temperature is too low or the gate ramp rate is too high, it is possible that only one type of

charge is detected. For example, it is conceivable that high-mobility Na+ drifts but low-mobility K+ does not. The TVS method also lends itself to mobile charge determination in interlevel dielectrics, since a current or charge is measured instead of a capacitance.

3.2.8 Deep Level Transient Spectroscopy (DLTS)

a) Bulk Traps

Deep-level transient spectroscopy (DLTS), introduced by Lang in 1972 [65] is commonly used to determine densities, energies, and capture cross sections of bulk and interface traps in semiconductors and sometimes for border traps. The device capacitance, current, or charge is measured as a function of time after pulsing the device between zero/forward and reverse bias. The traps capture electrons/holes which they subsequently emit, leading to the time-dependent capacitance [1]:

$$C(t) = C_0\left[1 - \frac{N_T}{2N_D}e^{\left(-\frac{t}{\tau_e}\right)}\right] \tag{36}$$

With the electron emission time constant t_e depending on temperature as:

$$\tau_e = \frac{e^{\left(\frac{(E_c - E_T)}{kT}\right)}}{\gamma_n \sigma_n T^2} \tag{37}$$

where γ_n is a constant for a given semiconductor. Determining the time constant at various temperatures allows the energy level E_T, density N_T, and capture cross section σn to be determined [52].

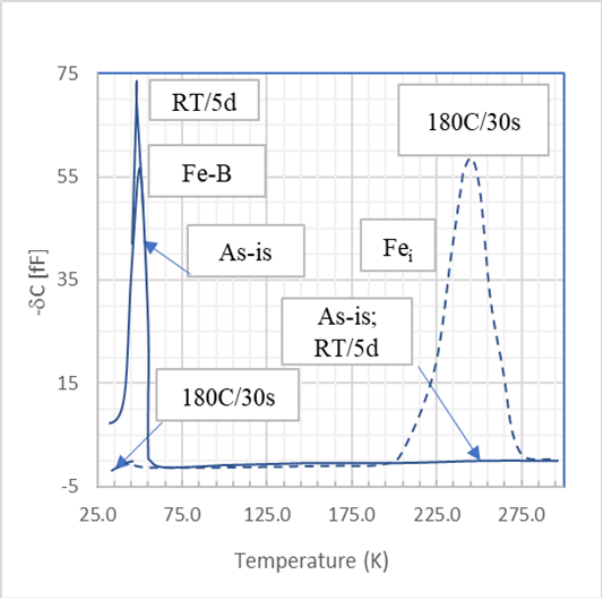

Fig.23: DLTS spectra for iron-contaminated Si wafer; "As-is", after 180°C/30 s dissociation anneal, and room temperature storage for 5 days.

Example DLTS spectra of iron-contaminated Si are shown in Fig. 24 [53]. Iron forms Fe-B pairs in boron-doped p-type Si with a DLTS peak at T≈50 K. When the sample is heated at 180-200ºC for a few minutes, the Fe-B pairs dissociate into interstitial iron Fei and substitutional boron and the DLTS peak for Fei occurs around T≈250 K. After a few days the interstitial iron again forms Fe-B pairs and the "Fe-B" peak returns while the "Fei" peak shrinks as shown in Fig. 23.

Conventional DLTS, which is applied mainly for the electrical characterization of SiC, uses the described perturbation of the equilibrium electron concentration to obtain information about deep levels in the band gap (E_T, σ_n and the defect concentration, N_T). The relaxation to thermal equilibrium conditions is measured as capacitance transient response to a voltage pulse. The principle is shown in Fig. 24 [54].

If no bias (V_r = 0 V) is applied to the SCHOTTKY diode, the depletion region is small, as explained and the deep levels located below the FERMI level are filled with electrons. In this situation, the capture rate, c_n, is larger than the emission rate, e_n. Increasing the reverse bias (Vr = -10 V), increases the band bending and results in a widened depletion region (x = 0… x_d). The deep levels will now be located above E_F and thus $e_n >> c_n$ and the electrons will be emitted to the conduction band and rapidly flow out from the depletion region due to the applied electric field. Close to the edge of the depletion region (x_0 for V_r = 0 and xd for V_r = -10 V), there exist a free charge carrier tail, which extends a distance λ into the space charge

region. In this transition region, the traps stay filled because $c_n > e_n$. The distance λ is determined by the shallow doping concentration, N_d, and the energetic position of the trap, E_T [54];

$$\lambda = \sqrt{\frac{2\varepsilon\varepsilon_0(E_F - E_T)}{q^2 N_d}} \tag{38}$$

Thus, the transition region becomes less important for high electric fields, where $x_d >> \lambda$ and for deep levels close to the band edges.

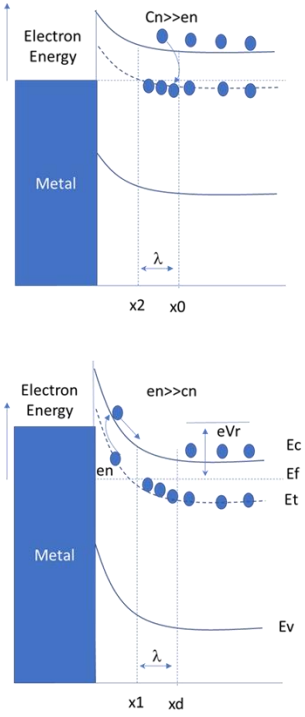

Fig.24: Band diagram of a SCHOTTKY contact on n-type material. Occupancy of one deep level under different reverse bias conditions is indicated. The shallow donor levels are not shown.

Thus, the trap concentration can be determined from the capacitance change [55]

$$\Delta C(t) = C(t) - C(\infty) = -\Delta C_0 e^{(-e_n t)} \tag{39}$$

$$\frac{\Delta C_0}{C} = \frac{1}{2}\left(\frac{x_1^2 - x_2^2}{x_d^2}\right)\frac{n_T}{N_d} \tag{40}$$

where $\Delta C_0 = C(\infty)-C(0)$, see Fig. (25), $x_1 = x_d - \lambda$ and $x_1 = x_0 - \lambda$, see Fig.(25).
If the transition region is neglected ($\lambda << x_d$), then equation (40) simplifies to:

$$\frac{\Delta C_0}{C} = \frac{1}{2}\frac{n_T}{N_d} \tag{41}$$

Capacitance transients ($C(t)=C(\infty)+\Delta C_0 \exp(-e_n t)$ are measured at different temperatures, which change the emission rate. If the capacitance change is analyzed by

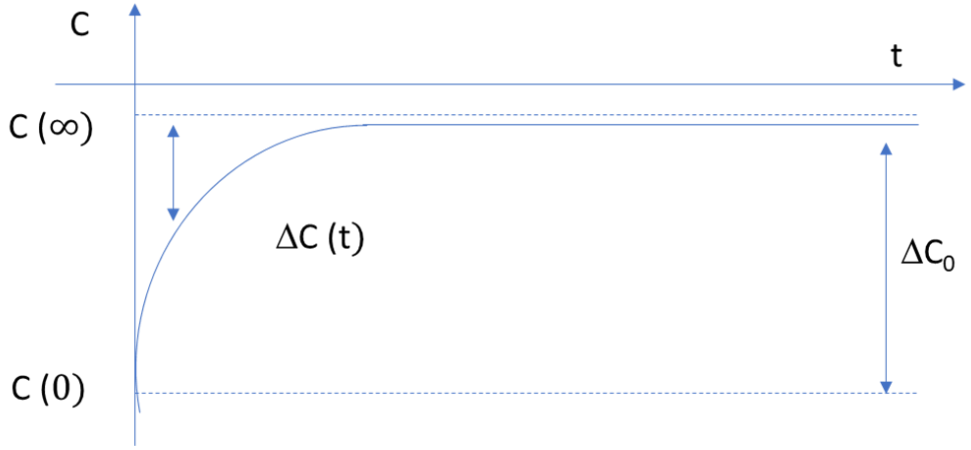

Fig.25: Diode capacitance transient ΔC(t) compared to steady state capacitance C(∞).

multiplication with a weighting function ($\int_0^{e_n(T)} w(t)dt = 0$), the emission from a defect level will be maximized for a certain rate window at a certain temperature and thus a peak will occur in the spectrum (DLTS signal versus temperature) [54]. Changing the rate window, τ_{ref}, the emission peak occurs at a different temperature. In case of a double boxcar correlation function ($\Delta C = C(t_2)-C(t_1)$)[56], the DLTS signal, S, is:

$$S \propto \left[\exp\left(-\frac{t_1}{\tau}\right) - \exp\left(-\frac{t_2}{\tau}\right)\right] \tag{42}$$

and the emission takes place at:

$$\tau(T) = \tau_{ref} = \frac{t_2 - t_1}{\ln\left(\frac{t_2}{t_1}\right)} \tag{43}$$

Deep levels, in n-type materials located above the middle of the band gap in the case

SiC, can be detected by a temperature scan from 85 to 700 K [54].

b) Interface Traps

The instrumentation for interface trapped charge DLTS is identical to that for bulk deep-level DLTS, but the data interpretation differs because interface traps are distributed in energy through the band gap. We illustrate the interface trapped charge majority carrier DLTS concept for the MOS-C in Fig. 19(a). For a positive gate voltage most interface traps are occupied by majority electrons for n-substrates (Fig. 19(b)) [1].

A negative gate voltage drives the device into deep depletion, causing electrons to be emitted from interface traps (Fig. 19(c)).

Interface trap characterization by DLTS was first implemented with MOSFETs [58]. Being three terminal devices, they have an advantage over MOS capacitors. By reverse biasing the source/drain and pulsing the gate, majority electrons are captured and emitted without interference from minority holes that are collected by the source-drain [1]. This allows interface trap majority carrier characterization in the upper half of the band gap. With the source-drain forward biased, an inversion layer forms, allowing interface traps to be filled with minority holes. Minority carrier characterization is then possible and the lower half of the band gap can be explored. This is not possible with MOS-Cs because there is no minority carrier source other than thermal generation [1].

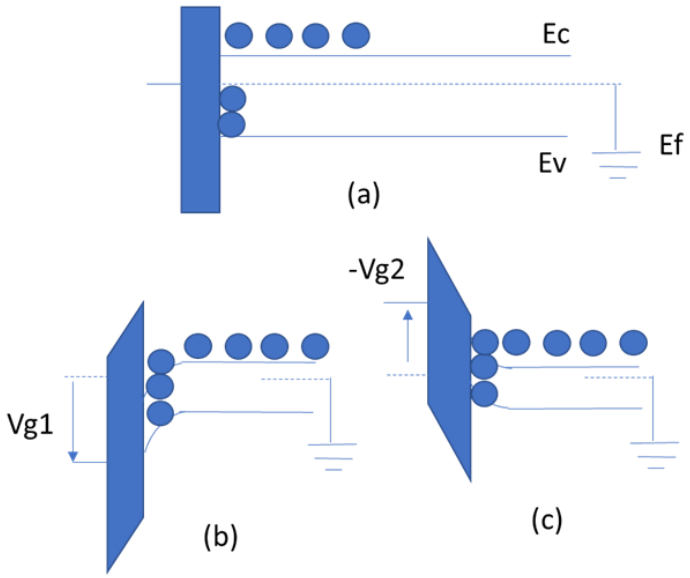

Fig.26: (a) Flatband, (b) majority carrier capture and (c) majority carrier emission frominterface traps

MOS capacitors are, nevertheless, used for interface trap characterization [55]. Unlike the conductance technique, DLTS measurements are independent of surface potential fluctuations. The derivation of the capacitance expression is more complex for MOS-Cs than it is for diodes. We quote the main results whose derivations can be found in Johnson [56] and Yamasaki et al. [57]. For $q^2D_{it}=C_{it}<<C_{ox}$ and $\delta C=C_{hf}(t_1)–C_{hf}(t_2)<<C_{hf}$

$$\delta C = \frac{C_{hf}^3}{K_s \varepsilon_0 N_D C_{ox}} \int_{-\infty}^{\infty} D_{it} \left(e^{-\frac{t_2}{\tau_e}} - e^{-\frac{t_1}{\tau_e}} \right) dE_{it} \tag{44}$$

where τ_e is the electron emission time, t_1 and t_2 the sampling times, and E_{it} the interface trap energy. If D_{it} varies slowly in the energy range of several kT around $E_{it,max}$, it can be considered reasonably constant and can be taken outside the integral of Eq. (44) leading to:

$$D_{it} = -\frac{K_s \varepsilon_0 N_D C_{ox}}{kTC_{hf}^3 ln\left(\frac{t_2}{t_1}\right)} \tag{45}$$

If the sample contains bulk as well as interface traps, it is possible to differentiate bulk traps from interface traps by the shape and the peak temperature of the DLTS plot. Interface trap densities determined by DLTS and quasi-static C-V are shown in Fig. 27.

c) Border Traps

DLTS has also been used to characterize border traps by using large amplitude filling pulses, allowing electrons not only to be captured by D_{it} but also to tunnel to border traps.[59] This effect was observed for electron tunneling, but not for holes attributed to the higher barrier for holes at the SiO_2/Si interface. The spatial and energetic border trap distribution is obtained by varying the pulse width and amplitude. In this tunnel DLTS it is possible to distinguish between interface and border traps [1].

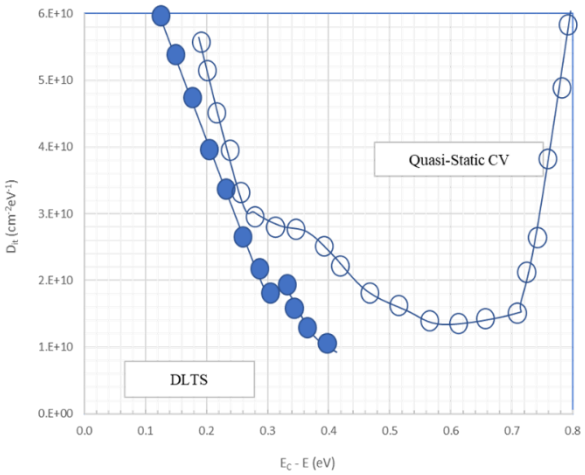

Fig.27: Interface trap density for n-Si measured by the DLTS and quasi-static methods.

3.2.9 Mosfet subthreshold slope

a) Interface Traps

The effects of D_{it} on the MOSFET subthreshold I_D-V_G characteristics are illustrated in Fig, 28. Similar to the broadening of the C-V_G curves in Fig.10, the subthreshold characteristic also broadens and only the surface potential region between about midgap ($\varphi_s=\varphi_F$) and inversion can be probed. The drain current of a MOSFET in the subthreshold regime for drain voltages higher than about 4kT/q is

$$I_D = \frac{W\mu_{eff}}{L}\left(\frac{kT}{q}\right)\sqrt{\frac{qK_s\varepsilon_0 N_A}{4\varphi_F}}\,e^{\left(\frac{q(V_{GS}-V_T)}{nKT}\right)} \qquad (46)$$

where $n=1+(C_b+C_{it})/C_{ox}$, where C_b is the bulk (substrate) capacitance

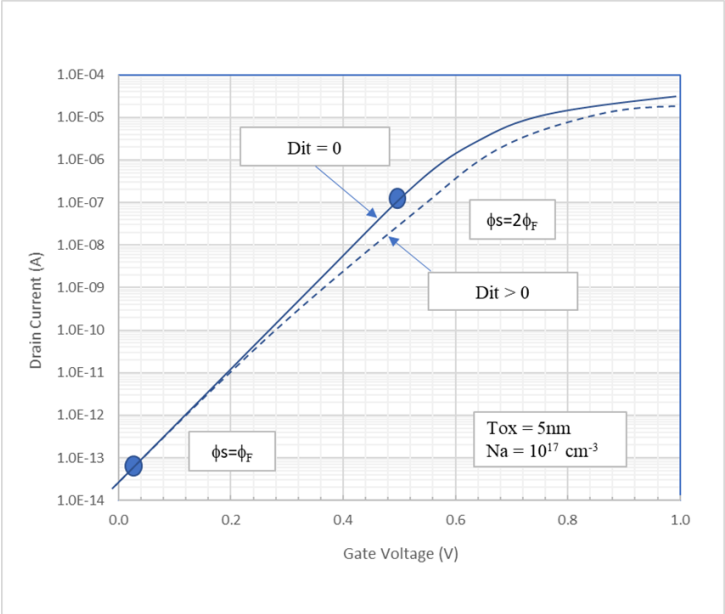

Fig.28: Theoretical I_D-V_G curves for $D_{it}=0$ and $D_{it,min}=2.7x10^{10}$ $cm^{-2}eV^{-1}$.

The usual subthreshold plot is log(I_D) versus V_G with subthreshold swing S being that gate voltage necessary to change the drain current by one decade, given by[1]:

$$S = \frac{ln(10)nkT}{q} \approx \frac{60nT}{300}\frac{mV}{decade} \tag{47}$$

with T in Kelvin. The interface trap density is:

$$D_{it} = \frac{C_{ox}}{q^2}\left(\frac{qS}{ln(10)kT} - 1\right) - \frac{C_b}{q^2} \tag{48}$$

requiring an accurate knowledge of C_{ox} and C_b[1]. The slope also depends on surface potential fluctuations. This is the reason that this method is usually used as a comparative technique in which the subthreshold swing is measured, then the device is degraded and remeasured [1]. The D_{it} change is given by:

$$\Delta D_{it} = \frac{C_{ox}}{ln(10)q^2kT}\left(S_{after} - S_{before}\right) \tag{49}$$

The subthreshold MOSFET curves are shown in Fig. 29 before and after stress, causing a threshold voltage shift and a slope change.

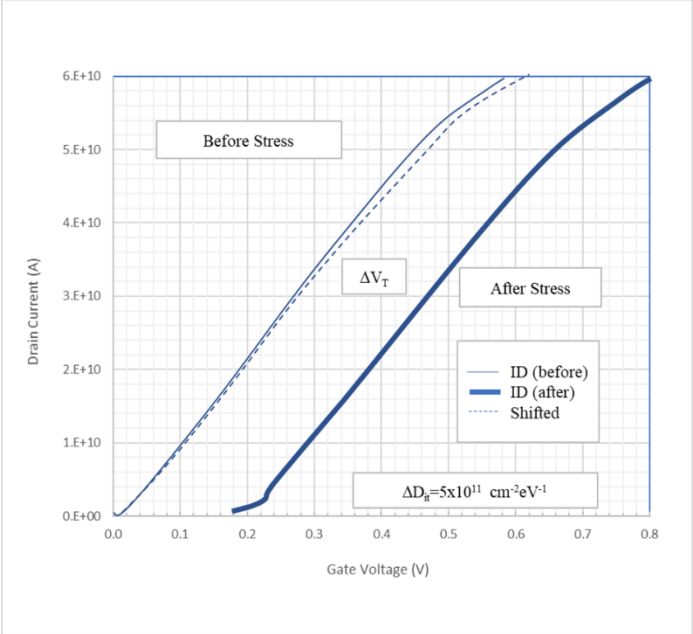

Fig. 29: MOSFET subthreshold characteristics before and after MOSFET stress. The change in slope results in a stress-generated $\Delta D_{it}=5x10^{11}$ $cm^{-2}eV^{-1}$. The dashed curve is the "After stress" curve shifted to the left to coincide with the "Before stress" curve at $I_D=10^{-13}$ A to bring out the slope change.

b) Oxide Traps

Subthreshold measurements are also made to determine oxide charge densities. When the surface potential coincides with the Fermi level, as shown in Fig. 30(a) by $\varphi_s=\varphi_F$, interface traps in the upper and lower half in the band gap are neutral, and neither contributes to a gate voltage shift. The corresponding gate voltage is V_{mg} , which is typically the gate voltage at $I_D\approx$0.1-1 pA. Increasing the gate voltage from Vmg to VT fills interface traps in the upper half of the band gap with electrons (Fig. 30(b)) [1]. ΔE usually covers the range from mid-gap to strong inversion. Since at mid-gap the interface traps do not contribute any voltage shift, a shift of Vmg must be due to oxide trapped charge according to [60]

$$\Delta V_{ot} = V_{mg2} - V_{mg1} \; and \; \Delta N_{ot} = \frac{\Delta V_{ot} C_{ox}}{q} \tag{50}$$

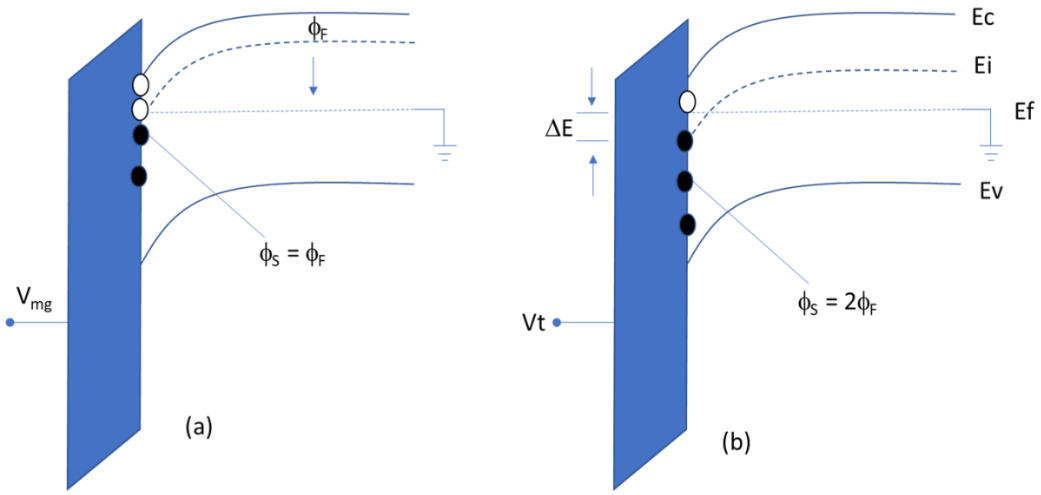

Fig.30: Band diagrams for midgap and threshold voltages.

An example of dielectric charging, related to border traps, is shown in Fig. 31, clearly illustrating the hysteresis for the transient measurements due to charge trapping/detrapping. The pulsed techniques was recently used to determine the capture cross sections.

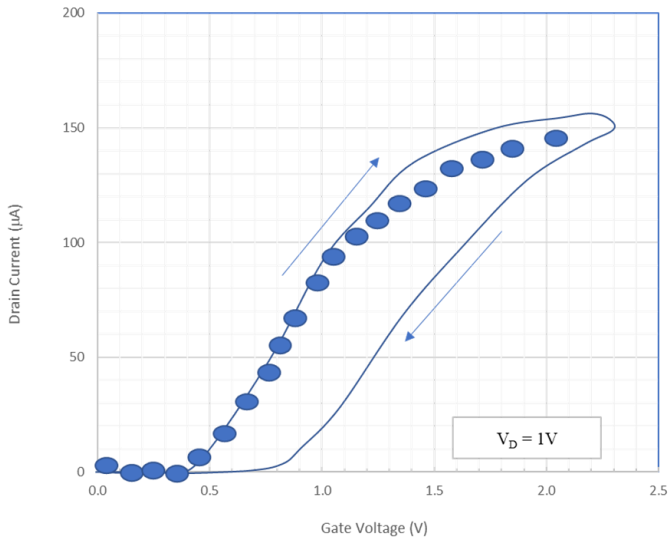

Fig.31: ID-VG dc (open circles) and transient (100 μs pulse width, rise and fall times) characteristics showing higher transient current and hysteresis due to carrier trapping/detrapping.

3.3.1 Determination of the effective trapped charge density and centroid

PST (Photon Stimulated Tunneling) is a power technique [61] for characterizing insulator defects in semiconductorinsulator structures with the energy levels outside the semiconductor band gap in particular in the upper part of the SiO_2 band gap.

Similary the DiMaria Method [62], based on the Fowler-Nordheim shift under CCS (Constant Current Stress) is able to detect traps not only at the SiC/SiO_2 interface but also inside the gate oxide bulk.

In fact charges trapped in the gate dielectric modify the electric field. Positive charges increase the cathode field whereas negative charges reduce it [63]. Accordingly, charge trapping can modify the gate current from the time-0 trap-free case.After stressing a device, the change in the gate voltage at a given current level resulting from an arbitrary charge distribution in the oxide ρ(x) is for +/- V_G respectively [62]:

$$\Delta V_G^+ = -\left(\frac{1}{C_{ox}}\right)\int \frac{x}{t_{ox}}\rho(x)dx \tag{51}$$

$$\Delta V_G^- = -\left(\frac{1}{C_{ox}}\right)\int \left(1-\frac{x}{t_{ox}}\right)\rho(x)dx \tag{52}$$

The limits of the integrals in (51) and (52) are 0 to t_{OX}, where x = t_{OX} corresponds to the Si-SiO_2 interface. The centroid of the charge distribution (integrated from 0 to t_{OX}) is:

$$\bar{x} = \frac{\int x\rho(x)dx}{\int \rho(x)dx} \tag{53}$$

$$\Delta V_G^+ = -\left(\frac{\bar{x}Q}{\varepsilon_{ox}}\right) \tag{54}$$

Q is the trapped charge in the oxide. To find the centroid of the trapped charge, we use (51) and (52) to evaluate the ratio $DV_G^+/(DV_G^+ + DV_G^-)$:

$$\frac{\Delta V_G^+}{\Delta V_G^+ + \Delta V_G^-} = \frac{\int \left(\frac{x}{t_{ox}}\right)\rho(x)dx}{\int \left(\frac{x}{t_{ox}}\right)\rho(x)dx - \int \left(1-\frac{x}{t_{ox}}\right)\rho(x)dx} \tag{55}$$

Inserting (53) into (55), we obtain [62]

$$\bar{x} = t_{ox}\left(1 + \frac{\Delta V_G^-}{\Delta V_G^+}\right)^{-1} \tag{56}$$

Equations (54) and (56) apply when the dielectric is thick enough so that there is no significant steady state current due to trap assisted tunneling[63].

3.3.2 Conduction mechanisms in dielectric layers and oxide integrity

The electrical quality of bulk dielectrics is evaluated by studying the current flowing through the insulator layer, performing I_G–V_G measurements (Fig. 32) [36]. The most important information that can be extracted from these measurements includes the identification of the conduction mechanism through the dielectric layer, the leakage current, the offset between insulator and semiconductor conduction or valence bands, and the breakdown characteristics [64]. Since the electrical resistance of SiO_2 lies in the range of 10^{15} W.cm, conduction in insulator layers is generally assumed to be negligible, especially with oxide fields below ~ 4MV/cm. In reality different phenomena can occur depending on the strength of the applied electric field and on the measurement temperature. To enable charge transport, extrinsic charge carriers must be injected from the semiconductor or gate electrode bands into the insulator bands [36]. For the MOS system, tunneling is the main current flow mechanism and depending on the electric field, it can be Fowler-Nordheim tunneling [65] direct tunneling [66]: in these cases the current is of ohmic type67]. When the carrier transport is associated with localized traps states in the insulator, the mechanism obeys Poole-Frenkel conduction [66]. Other mechanisms, such as Schottky (thermionic) emission, hopping and space-charge-limited conduction are not considered in this thesis; more details can be found in [67].

The tunnel conduction is caused by field ionization of trapped electrons (in the dielectric layer) into the conduction band, or by electrons tunneling from the metal to the semiconductor through the dielectric conduction band (or vice versa, depending on the applied polarity) [36]. In order to calculate the tunneling current, it is necessary to know the number of electrons that will travel by tunneling, their energy distribution,

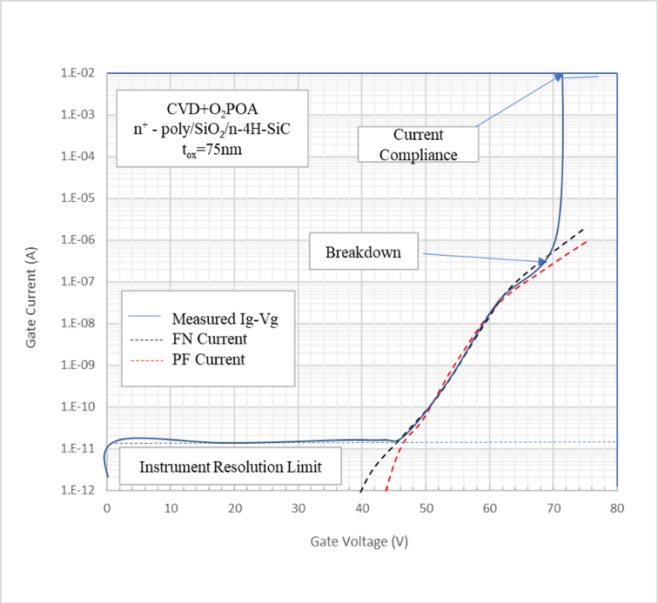

Fig.32: $I_G - V_G$ plot illustrating the conduction through the oxide, its possible mechanisms (Poole-Frenkel conduction and Fowler-Nordheim tunneling, explained later in the text) and oxide breakdown.

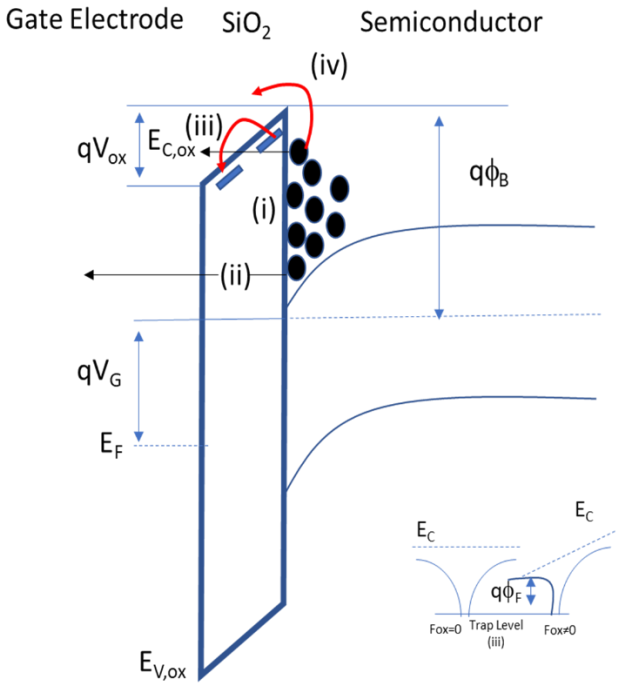

Fig.33: Different mechanisms of electronic conduction through the oxide of a MOS capacitor (in accumulation condition) fabricated on n-type substrate. i) Fowler-Nordheim tunneling; ii)

direct tunneling; iii) Poole-Frenkel conduction; iv) Schottky (or thermionic) conduction. The inset shows the mechanism of Poole-Frenkel conduction.

and the transmission or tunneling probability T(E) that an electron with energy E will cross the barrier. An approximate general equation is given by [67].

$$J = \frac{4\pi q m_0}{h^3} \int_{E_c}^{E_c + q\phi_B} T(E) k_B T ln\left(1 + e^{-\left(\frac{E - E_{Fs}}{k_B T}\right)}\right) dE \tag{57}$$

where h [J · s] is the Planck constant, ϕ_B[eV] the effective barrier height between the semiconductor and insulator bands, E_{Fs} [eV] the Fermi level in the semiconductor, and m_0 [kg] the free electron mass. When $V_{ox} < q\phi_B$, direct tunneling occurs. In this case the flow of electrons occurs through the entire oxide thickness, as illustrated in Fig.33. The tunnel emission is strongly dependent on voltage but is essentially independent from temperature and is more significant for thin oxides (< 10nm) rather than for thick ones (for the same Fox, Vox is larger for thicker oxides). For this reason this type of conducting mechanism was not considered in this work, since the oxide thicknesses of the investigated devices are in the range of 50nm to 80nm [36].

For higher oxide fields, so that Vox > $q\phi_B$ (typically larger than 5 − 6MV/cm), the carriers tunnel through a triangular barrier (Fig. 33) and the current density [A/cm^2] is given by the Fowler-Nordheim relationship [65]

$$J_{FN} = A_{FN} F_{ox}^2 e^{-\left(\frac{B_{FN}}{F_{ox}}\right)} \tag{58}$$

$$A_{FN} = \frac{q^3}{8\pi h \phi_B}\left(\frac{m_s}{m_{ox}}\right) \tag{59}$$

$$B_{FN} = \frac{8\pi\sqrt{2 m_{ox} \phi_B^2}}{3qh} \tag{60}$$

where $F_{ox} = V_{ox}/t_{ox}$ [V/cm] is the field across the oxide, m_s and $m_{ox} = 0.42m_0$ the effective electron masses for conduction [kg] in the semiconductor [68] and in SiO_2 [69], respectively [36]. This FN equation is derived under the assumptions that the electrons in the emitting electrode can be described by a free Fermi gas, with an effective mass mox, and that the

tunneling probability can be derived by taking into account the component of the electron momentum normal to the interface only [65]. The barrier height Φ_B depends essentially on the relative position of the band edges of the semiconductor and the oxide (Fig. 34). Due to the larger bandgap of 4H-SiC with respect to Si and to their band alignment, the barrier heights for electrons and holes from 4H-SiC to oxide are smaller than those of Si: tunneling conduction at lower fields with respect to the Si/SiO_2 system is indeed an issue for the reliability of oxides on SiC [70].

The Poole-Frenkel emission is a different conduction mechanism: it is not of ohmic nature, like tunneling, but involves localized trapping states in the insulator layer. Electrons are generally trapped in localized states – they are bound to a single atom – and not free to move in the dielectric material [36]. Random thermal fluctuations can occasionally have enough energy to promote some electrons to the insulator conduction band, where they can move for a short time, before relaxing into another localized state. In the presence of large electric fields, the electrons do not need much thermal energy for this process, since this is given by the field itself. As a result, these movements will be easier and more frequent, giving rise to a current, whose expression is given by [71]

$$J_{PF} = A_{PF} F_{ox} e^{\left(B_{PF}\sqrt{F_{ox}}\right)} \tag{61}$$

With:

$$A_{PF} = qN_C\mu_e e^{\left(-\frac{q\phi_{PF}}{k_B T}\right)} \tag{62}$$

$$B_{PF} = \frac{q}{k_B T}\sqrt{\frac{q}{\pi\varepsilon_0\varepsilon_{ox}^{HF}}} \tag{63}$$

where N_C is the density of states in the oxide conduction band, μ_e the mobility of electrons in the oxide and e^{HF}_{ox} the high frequency dielectric constant of the dielectric, the square of the refractive index n of the dielectric for ordinary light [72]. In this case ϕ_{PF} is the local energy barrier of a localized state, that the electron has to overcome to get into the conduction band of the insulator [73].

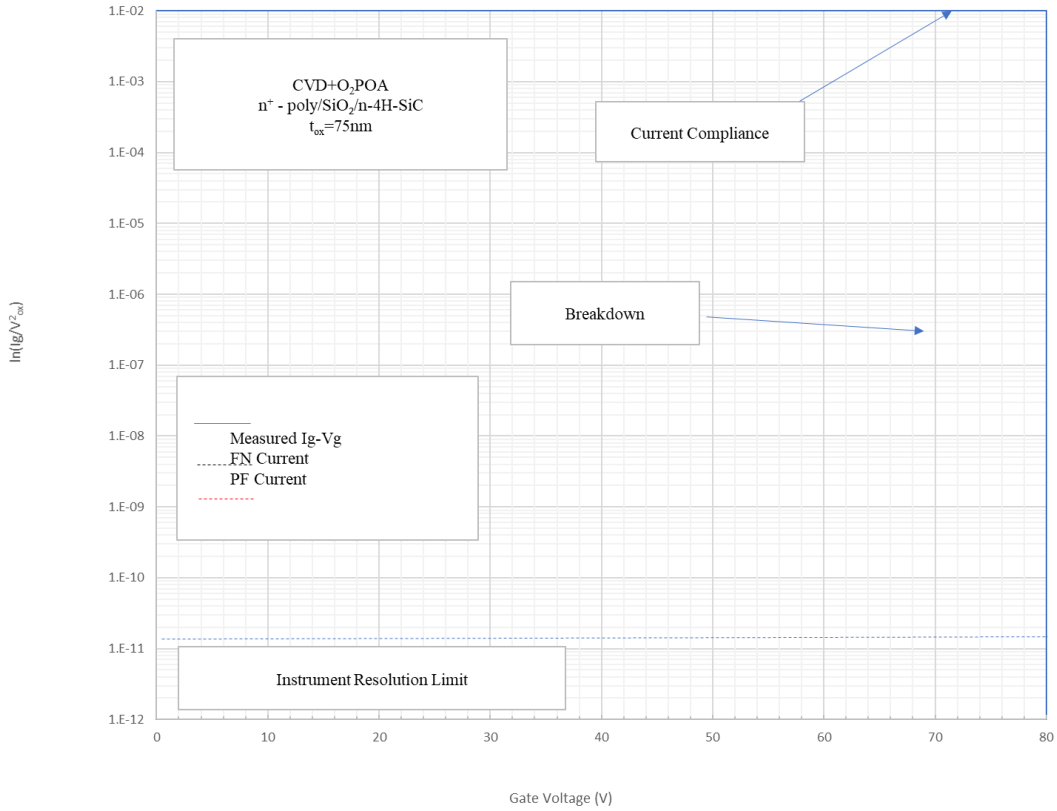

Fig.34: Band alignment between SiO_2, Si, 4H-SiC and 6H-SiC, after [36]. Values are in [eV].

Generally, in order to evaluate the current conduction mechanisms of insulator layers, the current-voltage measurement are plotted as a function of the oxide electric field F_{ox} (or of the voltage drop across the oxide J_G) versus the natural logarithm of the current density (or current I_G) [36]. Once one of these plots shows a linear behavior over a large current range, the corresponding conduction mechanism is found to occur in the examined device. These plots – the Fowler-Nordheim (FN) and Poole–Frenkel (PF) plots (Fig. 35), are obtained by rearranging Eq. (58), and Eq. (61), respectively. Taking the natural logarithm of both we obtain linear expressions:

$$ln\left(\frac{J_{FN}}{F_{ox}^2}\right) = ln(A_{FN}) - \frac{B_{FN}}{F_{ox}} \tag{64}$$

$$ln\left(\frac{J_{PN}}{F_{ox}}\right) = ln(A_{PF}) - B_{FN}\sqrt{F_{ox}} \quad (65)$$

From a plot of $\ln(J_{FN}/F^2_{ox})$ versus F^{-1}_{ox} or $\ln(J_{PF}/F_{ox})$ versus $\sqrt{F_{ox}}$ it is possible to identify the conduction mechanism and determine the constants A and B. From these, the values of the Fowler-Nordheim barrier ϕ_B and the high frequency dielectric constant e^{HF}_{ox} can be extracted from the FN and PF plot, respectively. A comparison with the ideal values, ϕ_B^{id} = 2.7 [eV] (Fig. 34) for the SiO_2/4H-SiC system and ε_{ox}^{HF} = 2.13 for SiO_2, is a good indication of which conduction mechanism prevails in the examined sample [72].

To correctly carry out the presented analyses, it is very important to know the real voltage drop across the oxide, V_{ox}, and not to use the applied gate voltage V_G, which is divided in the MOS structure between the oxide and the surface potential. The voltage drops across the oxide in a MOS capacitor (where no inversion layer is present) can be calculated with the following expression:

$$V_{ox} = V_G - V_{FB} - \psi_s = V_G - \left(\phi_{ms} - \frac{Q_{tot}}{C_{ox}}\right) - \psi_s \quad (66)$$

where Q_{tot} is the charge in the oxide (fixed, trapped or mobile), that can be positive or negative, influencing the band bending in the oxide. Interface states do not play a role in this case: a rigorous explanation of this effect can be found in [74].

The band bending ψ_s in general depends on the applied voltage. However, in good approximation it remains constant in accumulation (or inversion) regime, where tunneling dominates. For the analysis carried out in this thesis, since the structures are nMOS operated only in accumulation for this purpose, ψ_s = 0.2 V, equal to its saturating value in accumulation.

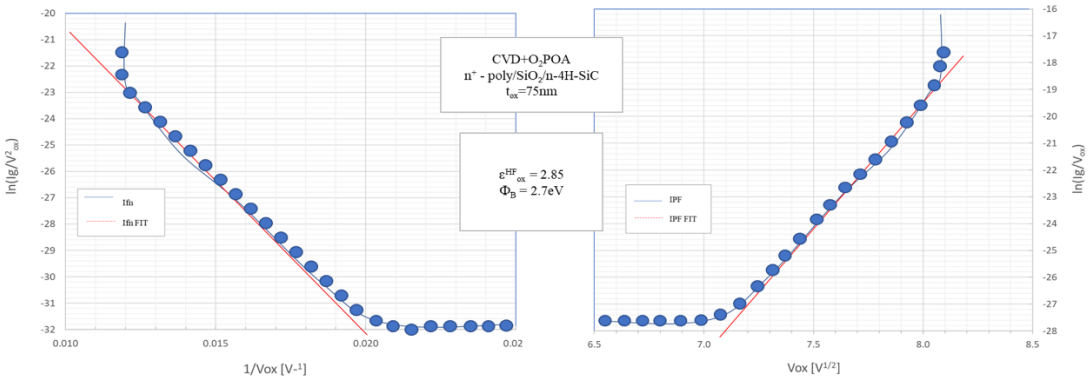

Fig. 35:(a) Fowler-Nordheim (FN) and (b) Poole–Frenkel (PF) plots of current versus oxide voltage, obtained from the data in Fig. 4.18. Both plots show linear behavior over a large voltage range but the extracted parameters show that the dominating mechanism is FN tunneling, since the extracted value of HF ox = 2.85 is too different from the ideal value, while B = 2.75 [eV], very close to the expected value.

3.3.3 Weibull statistics

The breakdown of SiO_2 films or insulator layers in general is studied by means of $I_G - V_G$ measurements on MOS capacitor structures, as done for the identification of the conduction mechanism explained in the previous section. Oxide integrity is determined by time-zero (TZBD) and time-dependent (TDDB) breakdown measurements. The time-zero method consists of recording an I_G–V_G curve with increasing gate voltage until the insulator breaks down (Fig. 32). This happens when the field across the oxide or insulator exceeds its electric strength, which is around 10 MV/cm for SiO_2 [73]. The mechanism of oxide breakdown is still a topic of intense research. The percolation model explains that a breakdown occurs through the sequential formation of a chain of defects, randomly generated in the thickness of the insulating layer, that form a percolation path leading to the rupture [75]. The time-dependent measuements are the constant gate voltage (CVS) and the constant gate current (CCS) stress methods. In these methods either a gate voltage near the breakdown voltage is applied and the gate current is measured over time (CVS), or a gate current is forced through the insulator layer and the gate voltage monitored over time (CCS) [36]. For (CCS), the oxide voltage changes during the measurement and defect generation rate and critical defect density required for breakdown change. This makes the (CVS) technique the more appropriate method for GOI determination [1].

When the oxide breaks down, the most important parameter for the quality of the oxide are the charge-to-breakdown, Q_{BD}, or the time-to-breakdown, t_{BD}. Since these two methods have not been used in this work, the reader can find more references in [73].

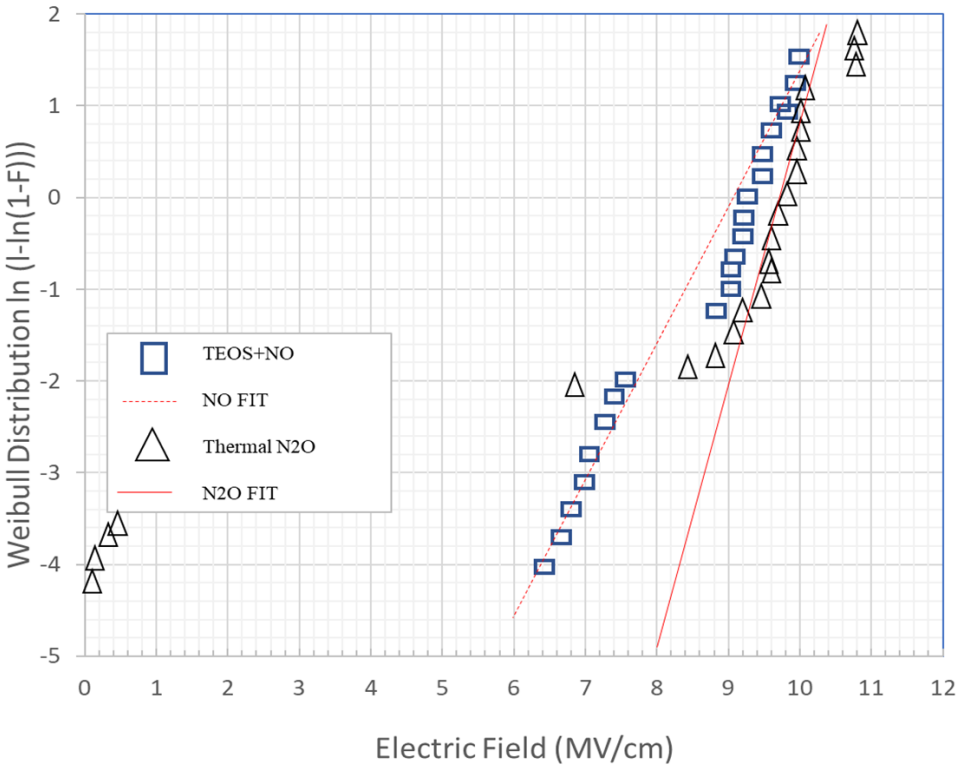

Fig.36: Weibull plot of TZDB measurements recorded for 100 MOS capacitors on n-type 4H-SiC, for two different oxides. _ values are extracted only for the intrinsic distribution of defects. The thermal N_2O oxide has a larger _ than the post-oxidized CVD oxide in NO: thermally grown oxides are of better quality than deposited ones

Oxide breakdown data – namely E_{BD}, Q_{BD} and t_{BD}, are often plotted as cumulative distributions. For the TZDB methodthe cumulative number of structures that have broken down at a certain field strength is plotted against the insulator electric field, as shown in Fig. 36. When a large number of such measurements are performed, e.g. on many devices on a wafer, the distribution function that best describes the observations, F(x), has been found to

be a Weibull distribution function [76]. If a set of N MOS capacitors is measured, each of which failing at an electric field $E_{BD,i}$, the cumulative failure is

$$F(x) = 1 - e^{-\left(\frac{x}{\alpha}\right)^{\beta}} \tag{67}$$

where x is the breakdown parameter of interest, α the characteristic life, corresponding to the percentile 63.2, and β the Weibull slope. Eq. (67) can be also written as

$$ln\big(-ln(1-F)\big) = \beta ln(x) - \beta ln(\alpha) \tag{68}$$

A plot of ln (−ln (1 − F)) versus ln(x) gives a straight line, as shown in Fig. 36 with slope b and intercept b ln(a), from which it is possible to obtain the distribution formula. For b < 1, the breakdown occurs due to extrinsic defects (impurities, crystal defects) at relatively low fields, while for b > 1 the breakdown is caused by intrinsic defects or wear-out of the oxide (Fig. 36).

The distribution function F(x) appearing in the equations above, must be obtained from the data itself: in order to do so it is necessary to calculate the empirical *distribution function* $\hat{F}$

$$\hat{F} = \frac{n.samples\ for\ which\ x < x_i}{N}$$

which can be automatically done with a statistical analysis tool, or can be approximated with the following expression (Bernard's median ranks) [77]:

$$\hat{F} = \frac{x_i - 0.3}{N + 0.4}$$

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CHAPTER 4

Results

4.1 Introduction and sample prearation of most of the samples

The device structures are realized by epitaxial growth on 4H-SiC substrates, so high-quality epitaxial wafers are essential for the development of high-performance power electronic devices such as faster switching speeds, lower losses, and higher blocking voltages, which are superior to standard silicon-based devices.

In the past 10 years, the growth process of the 4H-SiC homoepitaxial layer has been significantly improved and the current epitaxial technology enables more controllable and less defective large area substrate growth for the hexagonal polymorph of SiC (4H-SiC) with respect to the cubic counterpart (3C-SiC).

The drift layer, as an important part of power electronic devices, directly influences the performance of devices. Thus, it is very important that a high-quality drift layer can be obtained for the development of high-performance power electronic devices. Currently, the quality of the epitaxial layer is evaluated by two parameters [1]: uniformity and defect density of the epitaxial layer. The distribution of the breakdown voltage of devices in wafer depends on the uniformity of the epitaxial wafer with thickness and doping concentration, and the typical values of uniformity for the thickness and doping concentration are not more than 1.5% and 6.0%, respectively.

Although a high-quality homoepitaxial layer of 4H-silicon carbide (4H-SiC) can be obtained on a 4° off-axis substrate using chemical vapor deposition, the reduction of defects is still a focus of research.

In this study, several kinds of surface defects, either extended/ extrinsic or point/intrinsic, in the 4H-SiC homoepitaxial layer are systemically investigated.

In particular the aim of this thesis is to approach the defect characterization form several points of interest such as:

- Failure analysis method to identify the extended/extrinsic defect
- The effect of the contamination on a 4H-SiC performances and reliability and a new method of contamination detection
- Application of DLTS for point defect detection on a drift SiC Layer
- To investigate an example of process improvement by the POA (Post Oxidation Annealing) in NO and N_2O environment to reduce the NIOTs and SiC/SiO_2 interface and improve the channel mobility and also the gate oxide robustness and reliability. States, related to defects in the near-interfacial oxide layer, trap a considerable density of electrons from the SiC, and are likely responsible for the severe degradation of the electron mobility observed in the surface

channel of 4H–SiC/SiO_2 devices [2]. Most of the samples under analysis are Power MOSFET transistors at the end of the process and still at wafer level.

As mentioned above the substrate and the drift layer are the processes mainly suspected as the cause of defectivity. The first one is an n-type (0001) 4H-SiC 180μm thick substrate doped 4-5E18 cm^{-3} and resistivity of 0.012-0.025 Ω*cm.

On top an n-epitaxy layer is 12μm thick and doped 8E15 cm-3 is grown.

The gate oxide process is made under a 50-nm-thick oxide deposition on the Epitaxy layer, through a Low-Pressure Chemical Vapor Deposition (LPCVD DCS) in High Temperature Oxidation (HTO) furnace under dichlorosilane (SiH_2Cl_2) ambient.

The successive Post Oxidation Annealing (POA) using NO or N_2O as gaseous precursor is the process under investigation in this thesis work.

The process has been completed with an undoped TEOS layer 7000 Å thick, deposited by CVD technique, as intermediate dielectric followed by a 1700 Å thick TiTiNTi barrier sputtered through an Endura Sputtering tool and a AlSiCu metallization in the same chamber. This process is also under study and in particular the contamination induced by the sputtering chamber effect on the transistor performances and reliability

4.2 Extended defects electrical characterization and failure

It is well known that SiC occurs in many polytypes in nature, with different bandgaps, carrier mobilities, and crystal structures.

As mentioned in chapter one of the most common origin of defects in SiC epitaxial layers depend on the methods and reactors used to grow the layers which lead to epitaxial defects like growth pits (1–100 cm^{-2}), triangular inclusions of different polytype (e.g. 3C in 4H), carrot (0.1–10 cm^{-2}) and comet tail defects. Growth pits and carrot defects result from wafer defects that create adverse conditions for the realization of a perfect crystal structure during epitaxial growth. Temperature non-uniformities during epitaxial growth cause the appearance of triangle inclusions of different polytypes. Poor management of impurities or premature nucleations of SiC particulates cause the formation of comet tails and other defects.

But the most prominent defect in SiC is for sure the micropipe, and many commercial wafers are graded according to this specification. A micropipe is a thermodynamically stable hollow core screw dislocation, which shows as a hole through a wafer within a ±15° off the c-axis of the wafer and is close to 1 μm diameter in size. It has been shown that a SiC device with a micropipe in its active area cannot support significant electric field often leading to Drain Source leakage also in off condition [3].

The purpose of this section is to provide an example on the methodology of approaching a failure analysis flow starting, as shown in Fig.1, from an electric evidence of failure on devices suspected to be defect free by the inline inspection.

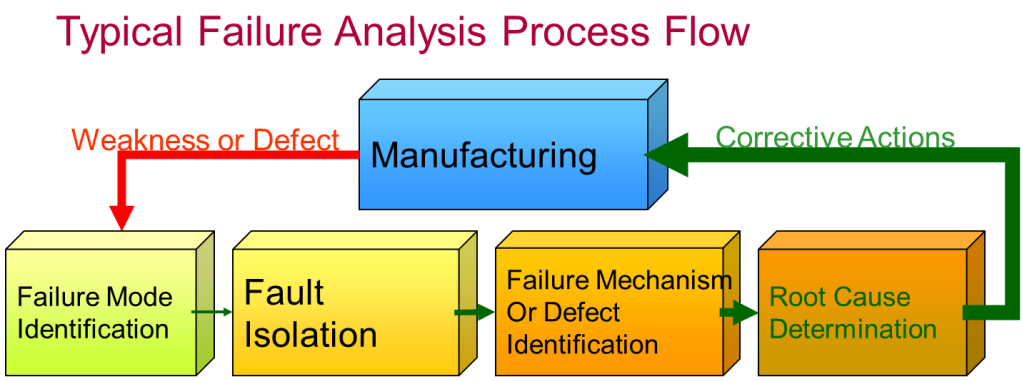

Fig.1: Failure analysis process flow example

A 4H-SiC based wafer, showed in Fig. 2, with a high level of failures (128 pink/fail devices vs. the yellow/good ones) related to Idss leakage (Vgs = 0, Vds = 50V) a high level of defectiveness was taken from the production.

At the beginning a superposition of the EWS binning and defectivity map has been performed to separate the devices for which the cause of failure was evident since the defectivity inspection, and the others (49 devices) not yet explained.

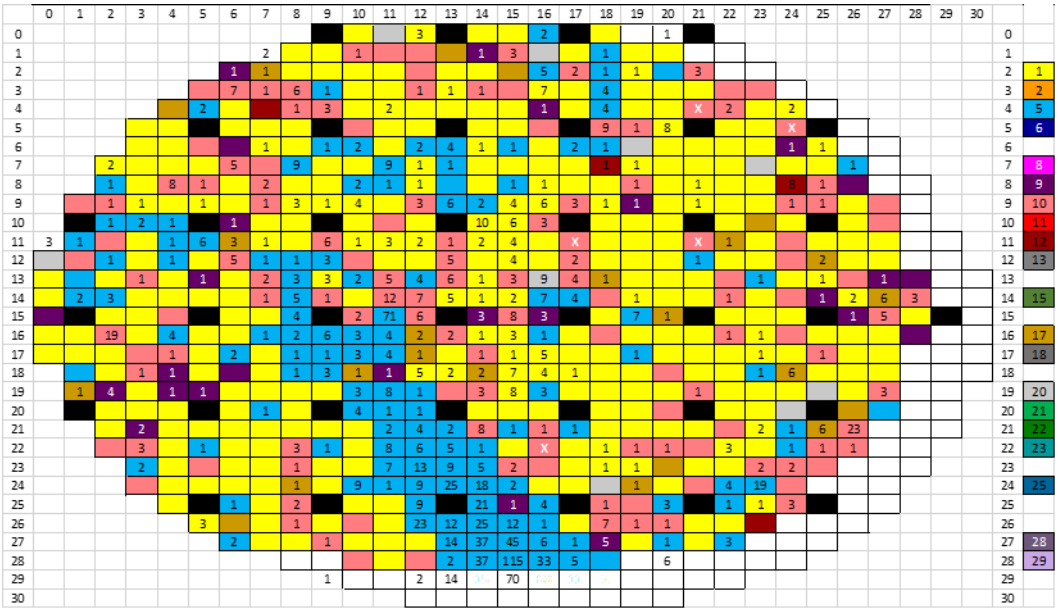

Fig. 2: Superposition of EWS binning (Binning scale at the right) and number of defects optically detected on each device

In this case the failed devices without any defectivity evidence were put under interest (see Fig. 2, pink devices, with no defects), but, in order to further differentiate the remaining devices the current separation technique to collect source and gate current was selecting just devices without gate oxide and SiC/SiO_2 interface degradation which compromises the next physical analysis. The devices in question were only 5 (as indicated by white X on Fig. 2) out of the initial 128, and the related current has been reported in Fig 3.

Bin10 @ EWS1	# dice	Current value @EWS1 [A]	Vth value @EWS1 [Volt]	IDSS@50V Bench [A]	IG@50V Bench [A]
IDSS@50V	A	5E-4	0.7	7.5E-3	-9.8E-9
	C	5E-4	2.6	2.6E-4	-8.5E-10
	E	5E-4	2.6	1.9E-2	1E-10
	B	1.3E-5	2.6	3.9E-6	-3.6E-10
	D	2E-6	2.7	4.1E-9	1.4E-11

Fig. 3: Current separation at breakdown on gate and source terminal.

On the other hand, other devices having high Igss leakage (at Vds = 50V) and namely "defect free" at optical inspection where also investigated. The majority of those devices show surface "burn" or cracks because of the large induced damage at the gate oxide interface as shown in Fig 4, making the related physical analysis ineffective.

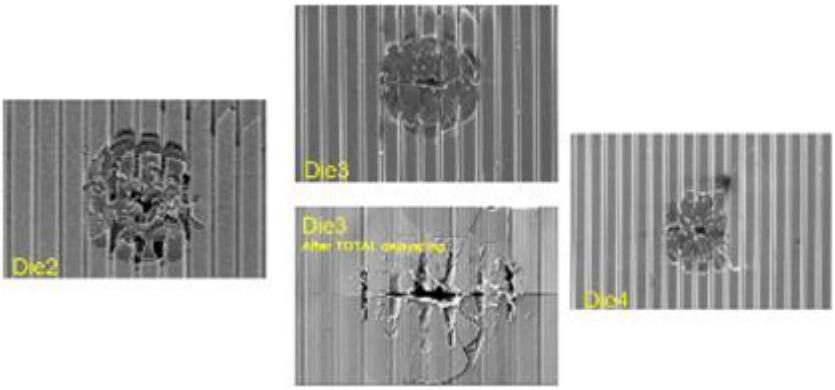

Fig. 4: Devices which exhibit high Igss (oxide degradation) have been selected for failure analysis

Then, the characterization of devices selected in Fig. 3, made possible to classify with specific fingerprints, in terms of electrical response and defectivity detection, a very limited sample size of the initial one. On all the samples a physical analysis with a 100% success rate, has been performed, confirming the failure mechanism related to defectivity.
It also provided crucial information to hypothesize a physical model, shown in Fig. 5 related to the presence of micropipe in body region, later confirmed by the TEM analysis.

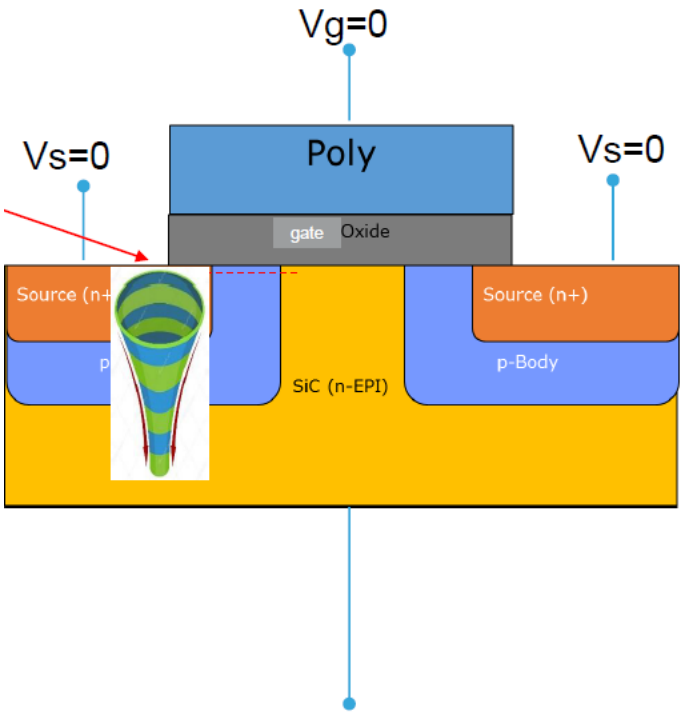

Fig.5: Failure mechanism related to Idss failure and high gate leakage at D-S junction breakdown

The fault isolation has been carrier out on the selected devices and then a physical analysis in front view (see Obirch spot and SEM image on Fig. 6).

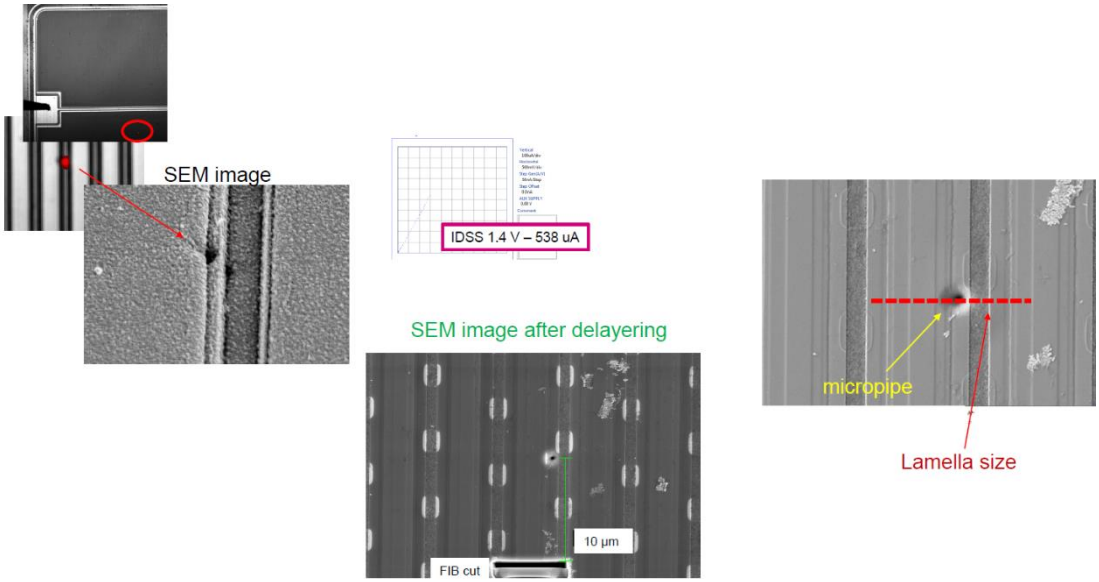

Fig.6: Fault Isolation and Front View SEM image and lamella area selection

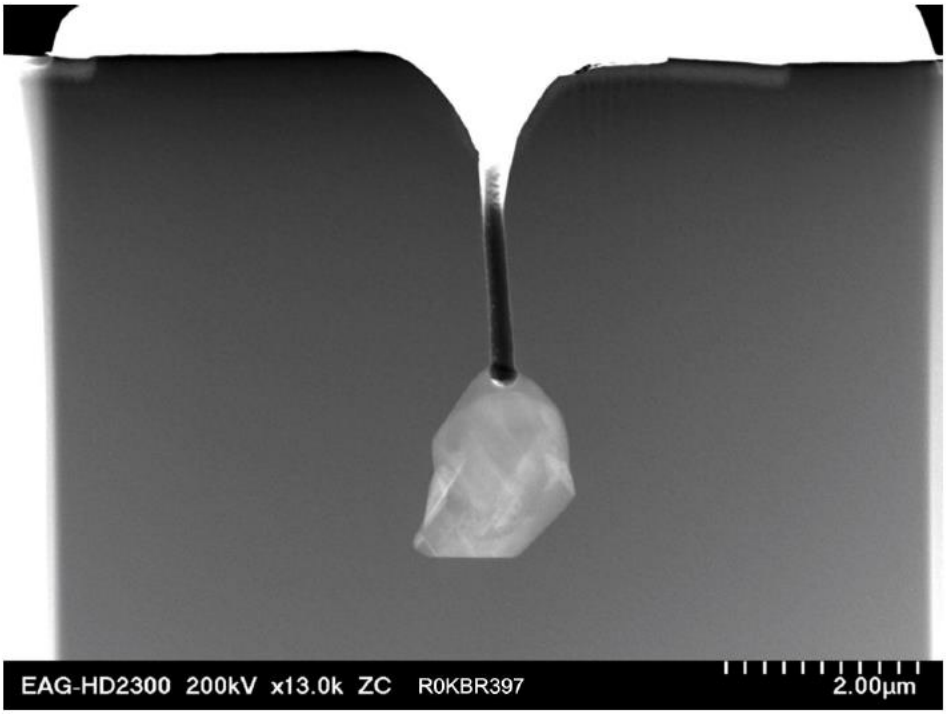

Fig. 7: Micropipe showed after TEM analysis

As hypothesized a micropipe, see Fig.7, has been found and it likely extend inside the drain epitaxy, crossing body implant.

4.3 Contamination in 4H-SiC PowerMOSFET

The purpose of processes is mainly dedicated to increase efficiency in order to improve the inversion channel mobility [4,5], gate oxide and in general transistor stability in order to reduce the on-resistance and increase transistor reliability and lifetime. Furthermore, most of the efforts in a production line are focused on process control and stability which are endangered by the several sources of contamination in the process flow or a cross contamination induced by the sharing of the same equipment for different technology. In this work, we have investigated the cause of this contamination at metal sputtering level, its specific failure mode and a way to reproduce it through the techniques mentioned above.

4.3.1 Evidence of failure

In Fig. 8, we report an example of wafer taken from a failed production due to a low threshold on all the map, with an evident worsening with center-edge symmetry.

The analysis on the process flow, steps and what is in common between several wafers suggest a possible root cause related to metallic contamination incorporated in the intermediate dielectric between polysilicon and metallization, which comes from other technologies, with a $NiSi_2$ metallization on the wafer backside, which shares the same process chamber. In particular, $NiSi_2$ at the backside in the high temperature metal sputtering chamber could degas and contamination could come out in the chamber being deposited on the top of the processed wafer.

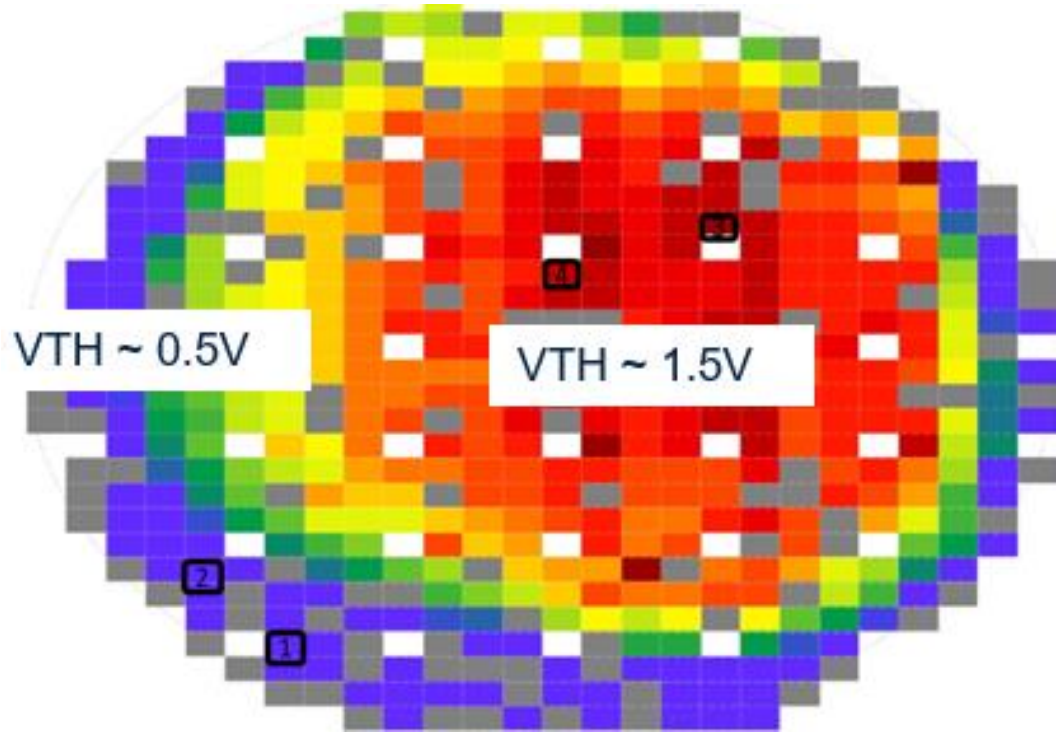

Fig. 8: Wafer failed with low Threshold

4.3.2 Sample preparation

The Power MOSFET transistors that we characterized in this work are built on 6" wafers on n-type (0001) 4H-SiC 180µm thick substrate doped 4-5E18 cm-3 and resistivity of 0.012-0.025Ω*cm. The n-epitaxy layer is 12µm thick and doped 8E15 cm-3. Over the Epi Layer a 50-nm-thick oxide has been deposited, through a Low-Pressure Chemical Vapor Deposition (LPCVD DCS) in High Temperature Oxidation (HTO) furnace under dichlorosilane (SiH_2Cl_2) ambient and a Post Oxidation Annealing (POA) using NO as gaseous precursor. The process has been completed with an undoped TEOS layer 7000 Å thick, deposited by CVD technique, as intermediate dielectric followed by a 1700 Å thick TiTiNTi barrier sputtered through an Endura Sputtering tool and a AlSiCu metallization in the same chamber.

The purpose of this work is the investigation of the physical mechanism associated with the 4H-SiC Power MOSFET transistor threshold reduction in a production line and its correlation to the metallic cross contamination chuck to wafer induced by the metal sputtering process chamber on the intermediate dielectric layer and the effect of Power MOSFET reliability, as it happened in the previous batches.

To verify the hypothesis of process cross contamination previously described a preliminary study on SiC bare test wafers has been done. Test wafers were intentionally contaminated by spin coating method [6], shown in Fig. 9: several Isopropyl alcohol (IPA) matrix solution samples were prepared by adding diluted Nickel NIST standard. Solutions concentration was by Perkin Elmer Elan DRC II Inductively Coupled Plasm Mass Spectroscopy (ICP-MS).

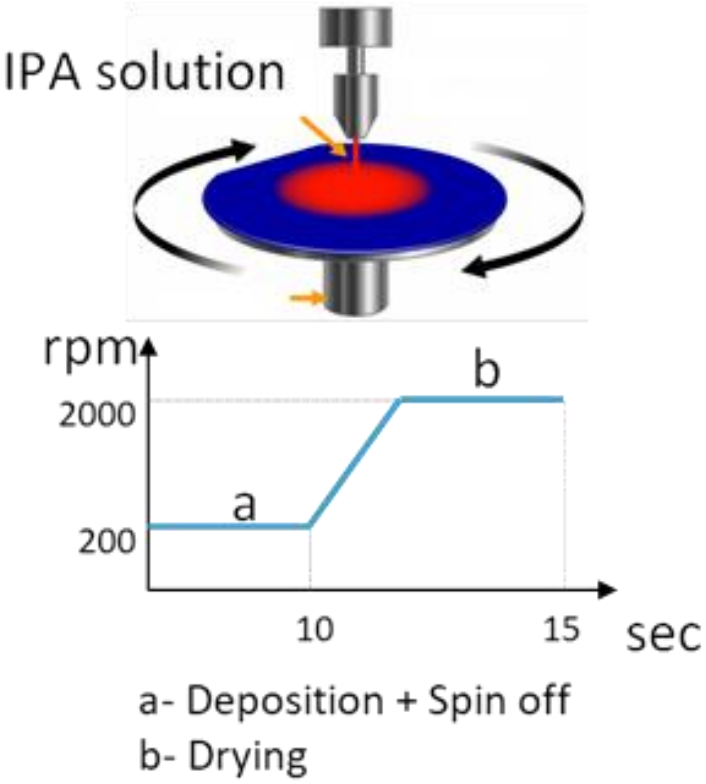

Fig. 9: Spin Coating method

A note amount of these solutions was dispensed on wafers surface to simulate a metallic contamination level range between 1E10÷1E13 at/cm^2. The contaminated wafers were analyzed by a Rigaku TXRF 3760 (Total X-Ray Fluorescence Spectroscopy) to clarify the relationship between Nickel ion concentration in IPA solution and the concentration on wafer surface. The TXRF, which is applicable only on flat wafers, allows to carry out 133 points with a spot size of about 1 cm^2 and depth of analysis of around 70 Å.

TXRF maps (see Fig. 10 and Table 1) suggest a clustering of contamination which is not uniformly dissolved in solution and then on the wafer. Despite this, an accurate linear correlation among the average contamination detected by TXRF analysis and the Nickel concentration in IPA solution has been found (see Fig. 11).

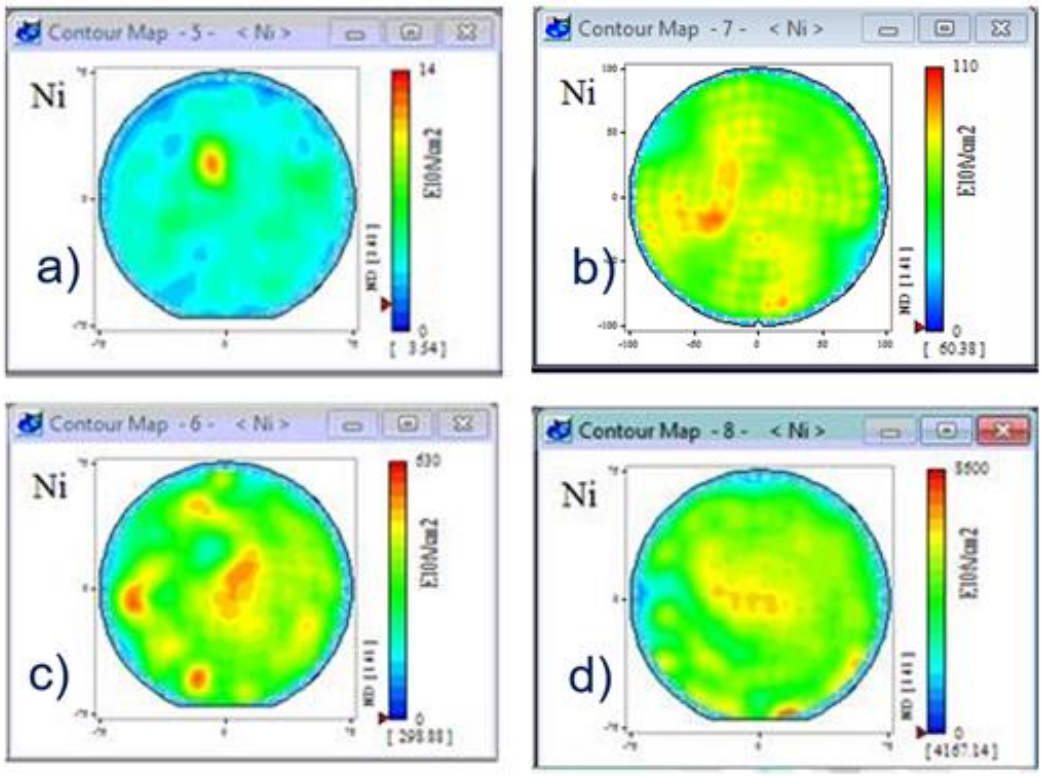

Fig. 50: TXRF Ni concentration maps: a) E10 at/cm^2, b) E11 at/cm2, c) E12 at/cm^2, d) E13 at/cm^2

	Atomic concentration (E10 at/cm2)			
	Sample a)	Sample b)	Sample c)	Sample d)
Average	3.57	14.23	298.92	4167.09
Max	12.33	21.04	571.43	7859.67
Min	0.00	1.4	40.87	643.82
Sigma	1.33	21.10	100.76	1282.49

Table 1: Values of Nickel concentration for sample a), b), c) and d)

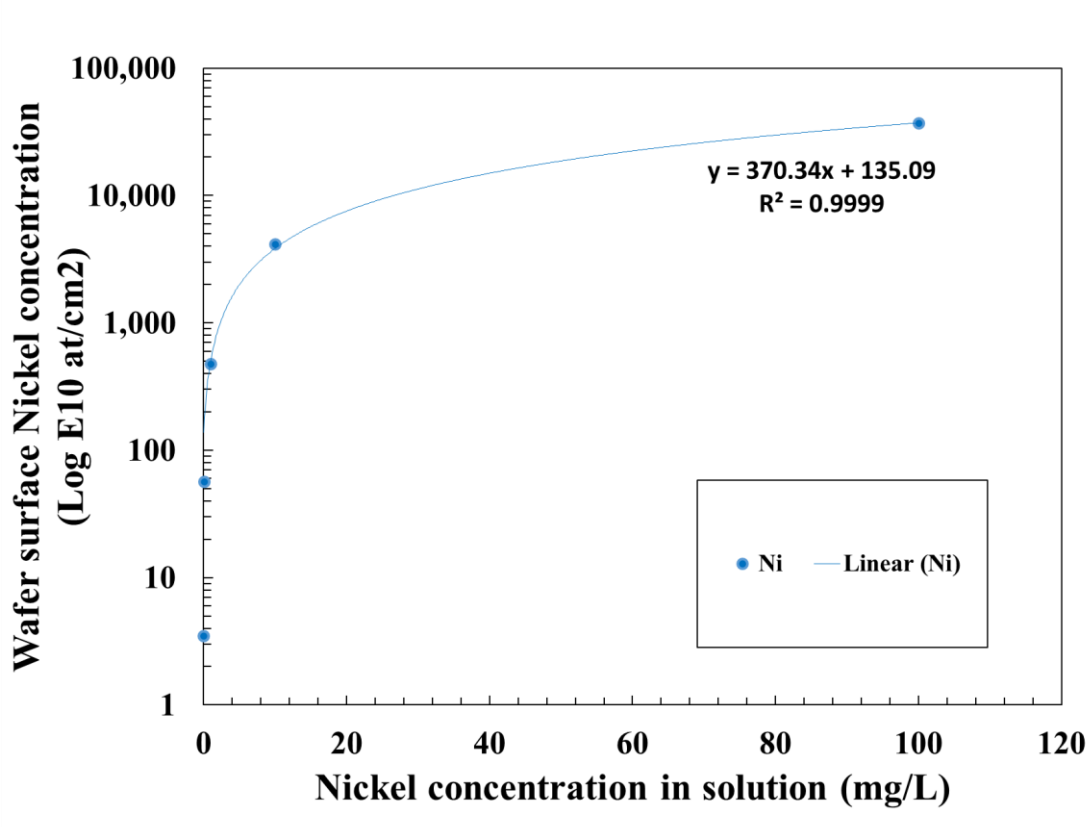

Fig.11: Nickel TXRF surface concentration vs. Nickel concentration in IPA solution

After this preliminary work, the same method was applied to intentionally contaminate the production wafer at intermetal dielectric step to simulate the model of voltage threshold degradation of the device with an average concentration of E14 at/cm^2. As shown in Fig. 10, the induced contamination is not uniform, and it is not localized at the edges of the wafer like the one contaminated by the process (Fig. 8).

4.3.3 DUTs (Devices under test) Classification

At the end of the whole process flow, the contaminated wafers have been tested at full map with a standard EWS (electrical wafer sorting), threshold voltage test performed shorting and sweeping from 0 to 10V drain and gate terminals and grounding the source one. The threshold voltage has been detected for Ids = 2.5µA, under the same testing conditions applied on failed processed wafer under standard conditions shown in Fig. 8.

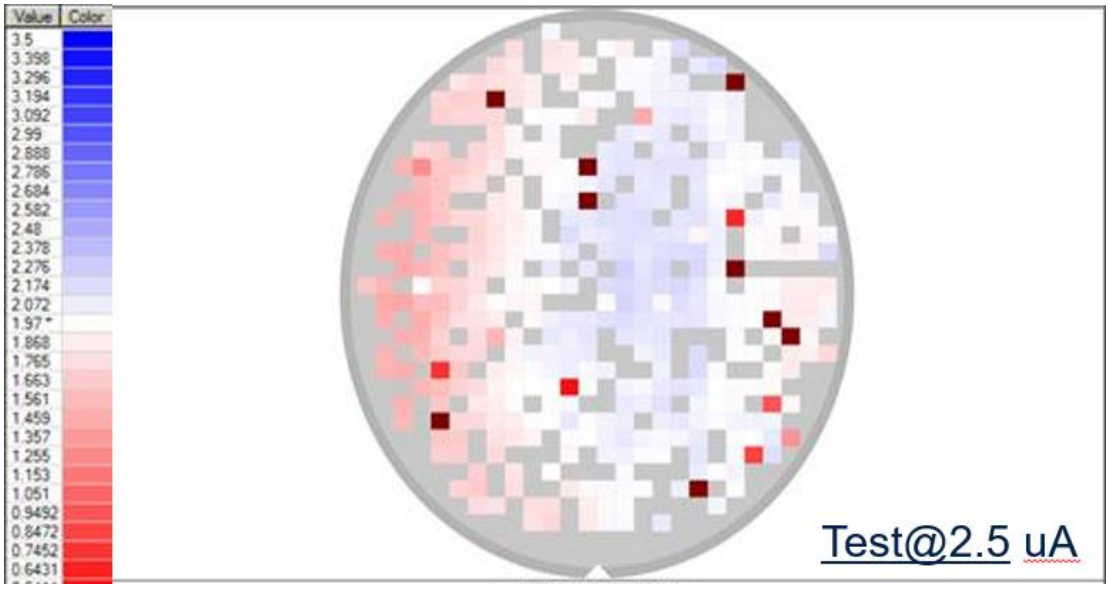

Fig.12: Wafermap of threshold at Ids=2.5 µA

Comparing Fig. 8 and Fig. 12 the wafer map related to intentionally contaminated wafer shows devices with low threshold values in a non-homogeneous way according to what hypothesized in the preliminary characterization shown in Fig 10. Devices in red region have low threshold values, on the other hand the blue ones have high threshold values. Furthermore, anomalous devices marked, respectively, dark red (Vth lower than 0.2V) and light red (Vth between 0.5V and 1V) subsequently named as Hard Low Vth and Soft Low Vth devices, as shown in Fig. 13, were analyzed to verify the impact of contamination in detail.

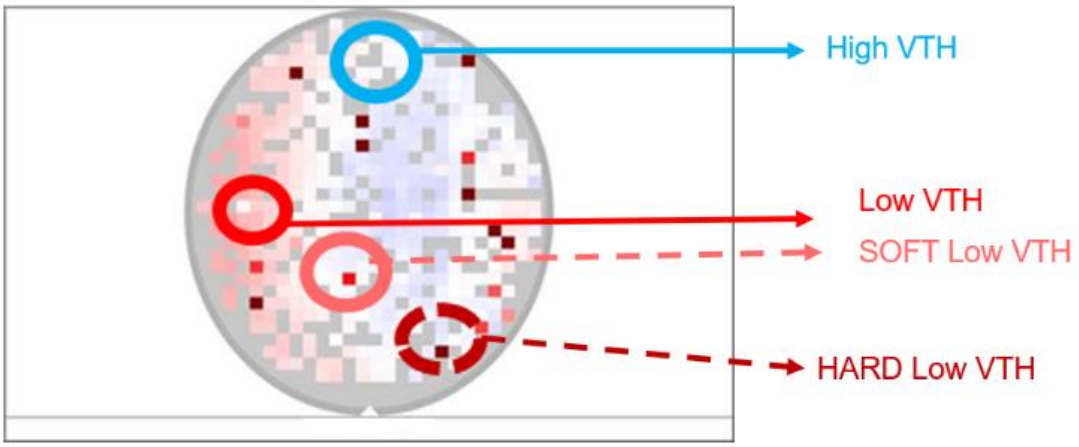

Fig.13: The samples used for the present work are devices with high Vth in blue, low Vth in red and the marked ones corresponding to (HARD Low Vth and SOFT Low Vth)

in red and the marked ones corresponding to (HARD Low Vth and SOFT Low Vth) The electrical characterization purpose is to understand if there is a commonality between the

anomalous devices in contaminated wafers and the ones with low threshold on the edge of the failed wafer taken by the production line.

Electrical Characterization for a specific failure mechanism identification. Usually, several failure mechanisms are associated to transistor threshold reduction or degradation under operative conditions. The commons are related to dangling bonds and states at SiC/ SiO_2 interface, poor oxide quality due to defectivity or contamination, plasma damage or charges induced by metallization processes. The charge-sensing method, inducing a Constant Current Stress, allows to isolate a Power MOSFET critical process or layer by the typical electrical fingerprint related to different techniques of analysis such as:

The Capacitance-Voltage (C-V) measurements which are designed to observe possible states at the interface, but in this case it allows to identify possible contamination in the gate oxide and at the interface [7], observing the C-V characteristics before and after stress. Any contamination (charge in the oxide or at the interface) manifests itself with a shift in the flatband voltage or even simply with a distorted and shifted C-V characteristic after stress [8]. It is also possible to have an indication of possible energetic states at the interface. The frequency triggers different energy levels in the band gap, as lower is the frequency as deeper is the level.

Vth and Fowler Nordheim drift under positive and negative Constant Current Stress (CCS) test allows to determinate:

A plasma damage or a contamination, impacting the intermediate dielectric, would introduce charges which could be moved under current stress varying the threshold in current over cumulated time stress. This method would be able to discriminate devices where the low threshold signal is accompanied by the recovery of the threshold under negative current stress and worsening of the same in the case of positive current stress, as in the previous batches.

a variation of the Fowler-Nordheim voltage under cumulated stress allows to estimate the position of the centroid of the maximum trapped charge and the trapped charge in the gateoxide following the method shown by DiMaria and Stasiak [9].

4.3.4 Results on Wafer contaminated by process

High and low threshold devices belonging to the wafer showed in Fig. 1 have been tested reading the threshold in current (VTC) intercepted at 5 µA, Capacitance-Voltage (C-V) and Fowler Nordheim tunneling (FN). Each device underwent a cumulative stress of about 1 hour: one part with positive stress and the other with negative stress under a Constant Current Stress (CCS) of Ig = +/- 1µA. At the end of each readout, the drift of VTC and FN have been evaluated and reported.

As shown in the Fig. 14, the VTC normalized to its initial value of low Vth device under negative stress current decreases, while the device with High Vth remains constant.

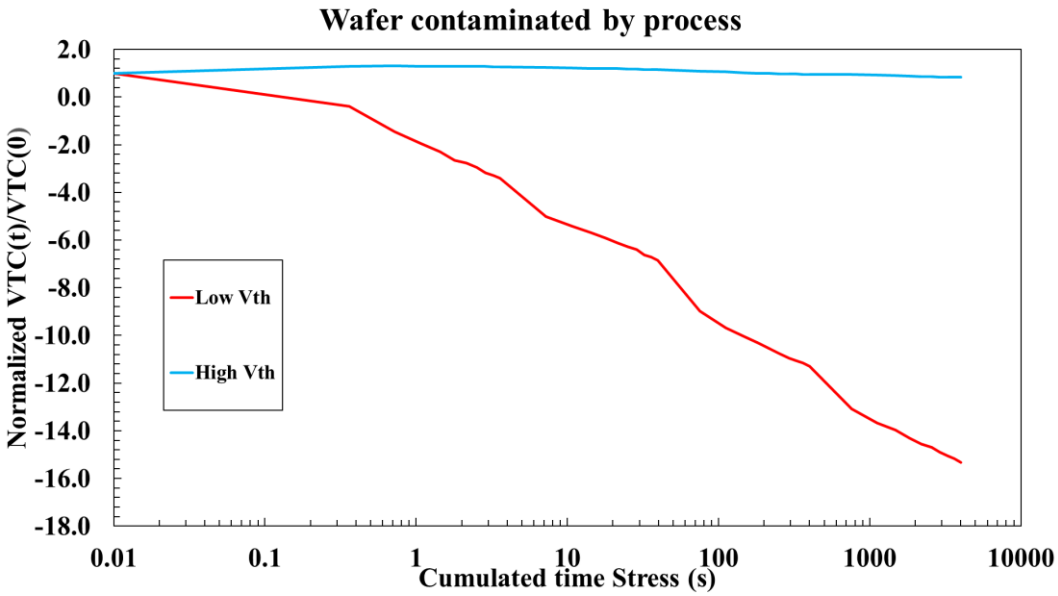

Fig. 14: VTC @ Ids=1uA normalized to the initial value under positive Constant Current

In Fig. 15, the VTC normalized to the initial value of Low Vth device under negative stress current decreases and then increases after 100 s of stress, while the device with high Vth remains constant.

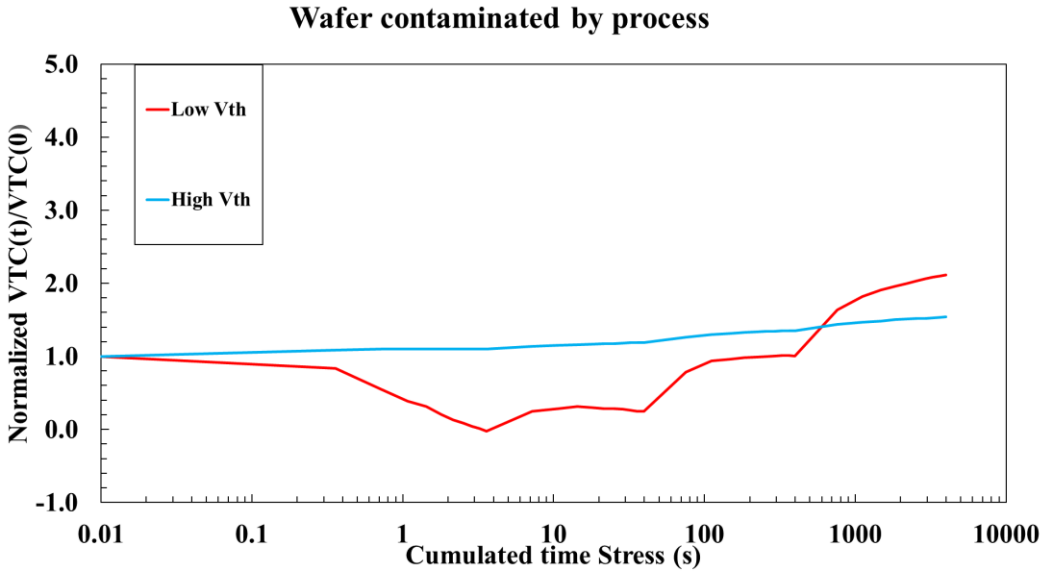

Fig. 15: VTC@ Ids=1uA normalized to the initial value under negative Constant Current stress Ig = -1uA

It is necessary to verify where this contamination comes from, which causes a lowering of the threshold. C-V measurements at high and low frequency are useful to understand if contamination is present at the SiO_2/SiC interface and states in the SiC bandgap. As shown in Fig. 16 and 17, C-V curves at 20 Hz and 100 kHz, for the samples mentioned above, are aligned the one with the other, they are not shifted or distorted and then, it seems to not be contamination at the interface. This confirms the positive effect of NO nitridation on [10, 11] on traps at SiC/ SiO_2 interface due to metallic contamination. Moreover, as previously demonstrated [12], it proves also the nitrogen benefit in decreasing the amount of carbonaceous compounds in the dielectric/SiC interface region on both the samples with high and low Vth.

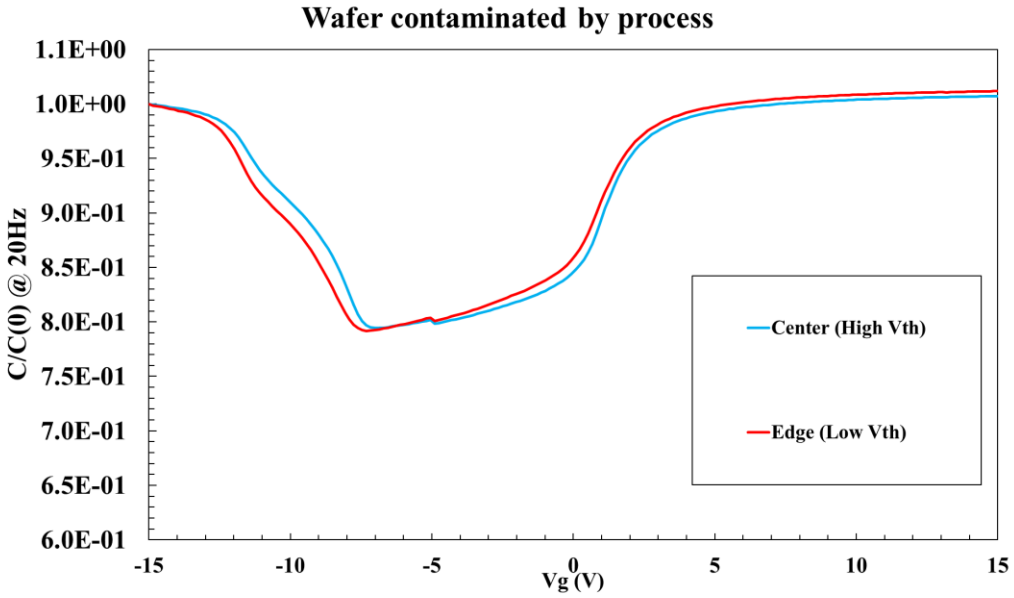

Fig. 16: C-V measurement at 20 Hz

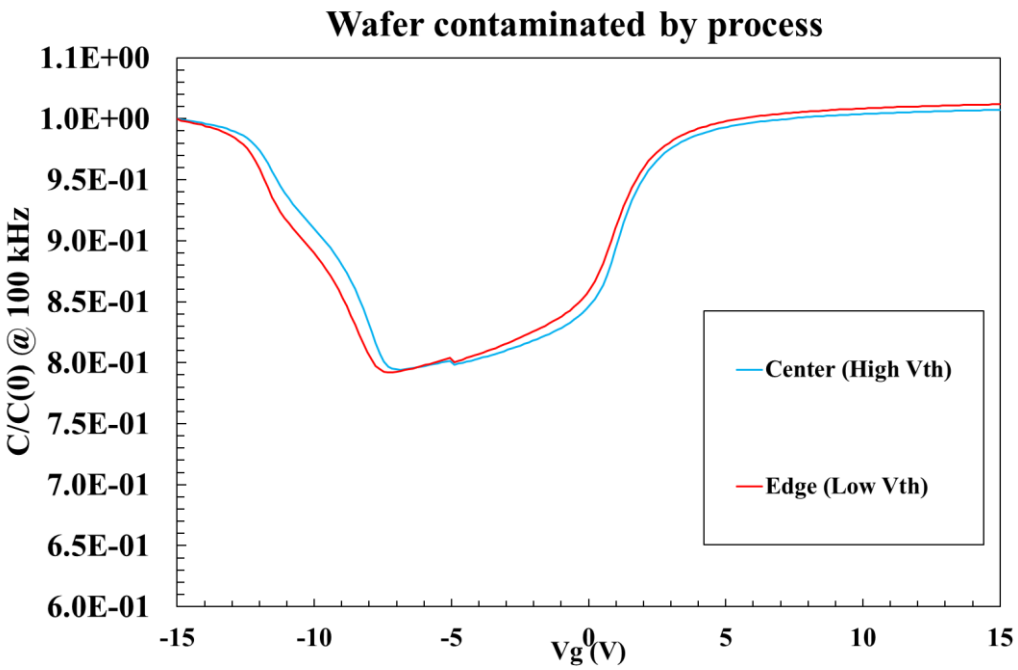

Fig.17: C-V measurement at 100 kHz

To make sure there is no contamination inside the gate oxide, we performed a Fowler-Nordheim tunneling measurement. From the Fowler Nordheim analysis of the contaminated wafer by process the two samples (Low Vth and High Vth) vary in the same way both for both positive and negative Fowler-Nordheim tunneling, i.e., there is no charge inside the gate oxide, as shown in Fig. 18 and Fig. 19 where we report the effect of negative stress as example.

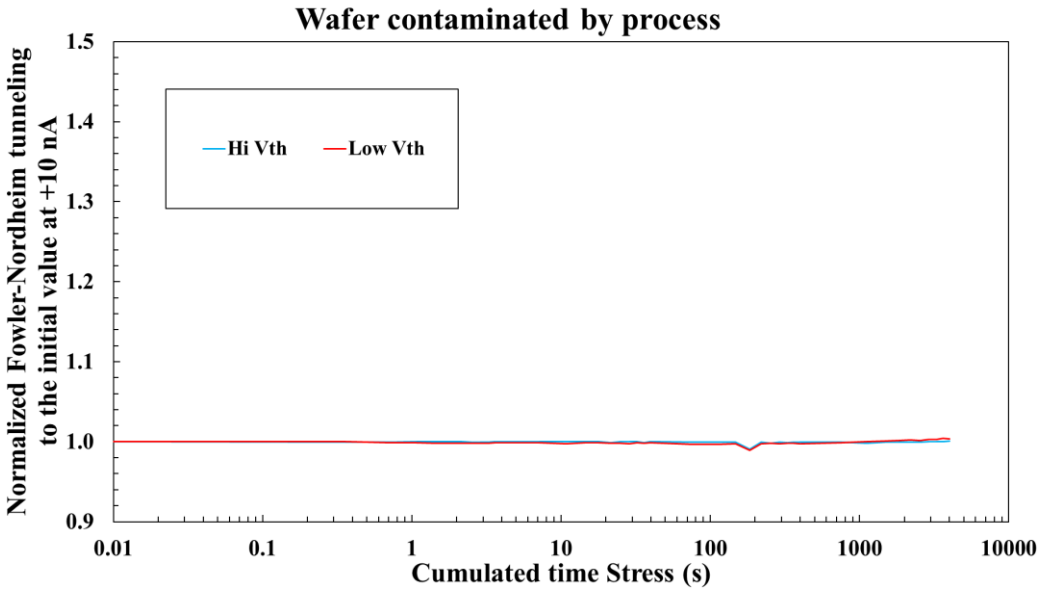

Fig. 18: Normalized Fowler-Nordheim tunneling to the initial value at +10 nA over cumulated time stress. No FN drift on both samples

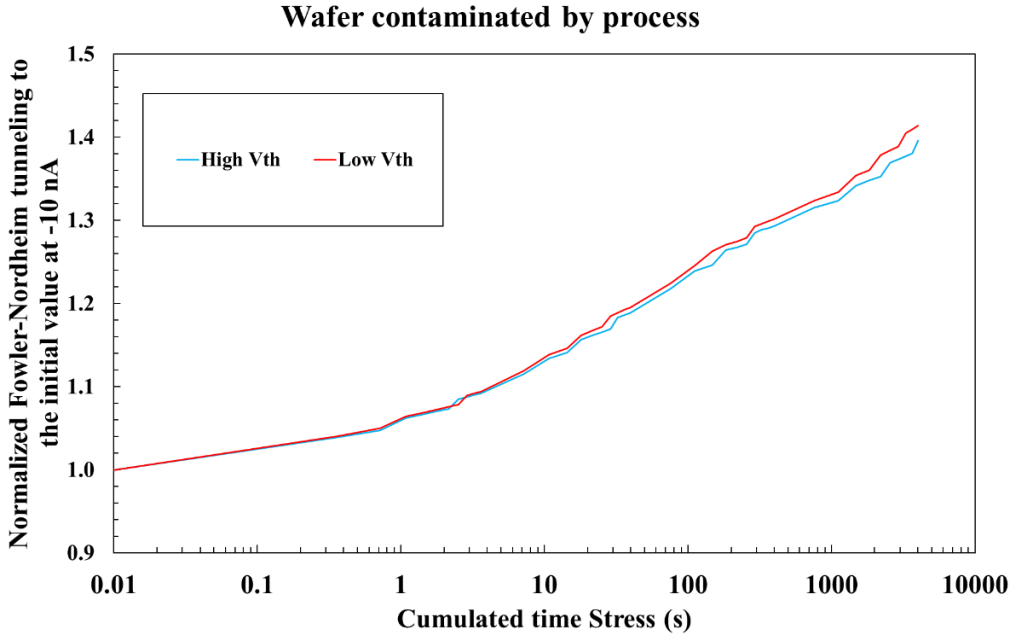

Fig. 19: Normalized Fowler-Nordheim tunneling to the initial value at -10 nA over cumulated time stress. Similar FN drift on both samples

4.3.5 Results on Wafer contaminated by process (I-V Characteristics and F-N Parameter Extraction)

In order to characterize density of states at SiC/ SiO_2 interface I-V characteristics have been carried out as did in previous work on POA effect on interface, which results will be shown in detail later.

In this case, confirming previous results on C-V and F-N shift there is no difference between failed wafer and good one (Fig. 20, 21, 22).

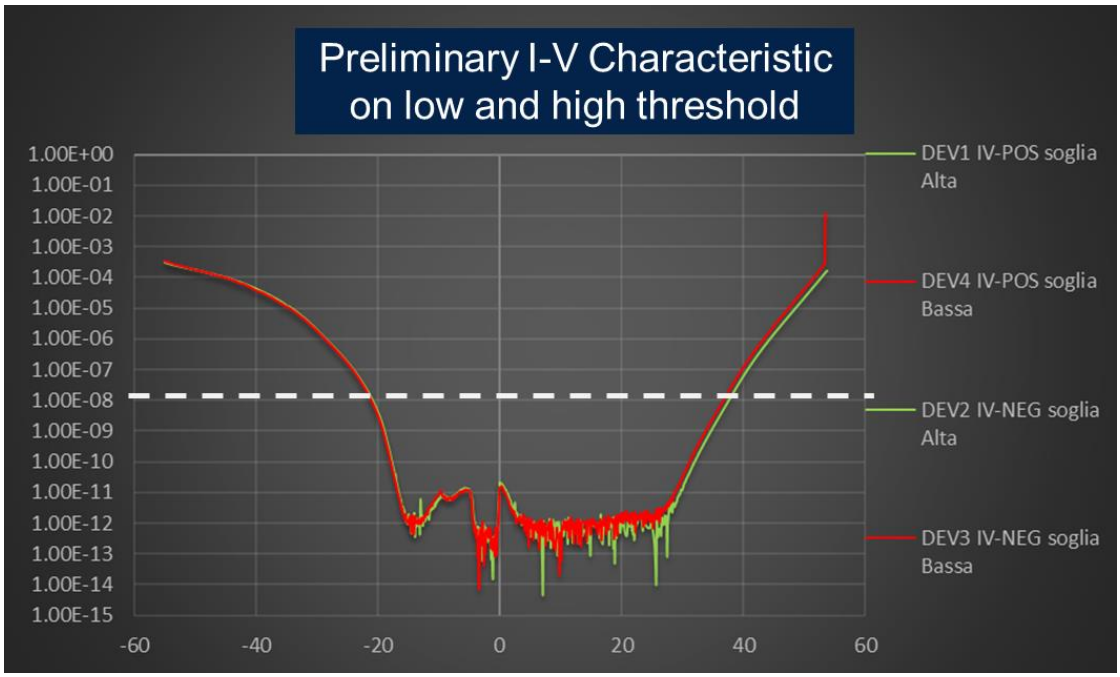

Fig. 20: I-V Characteristics under positive and negative bias

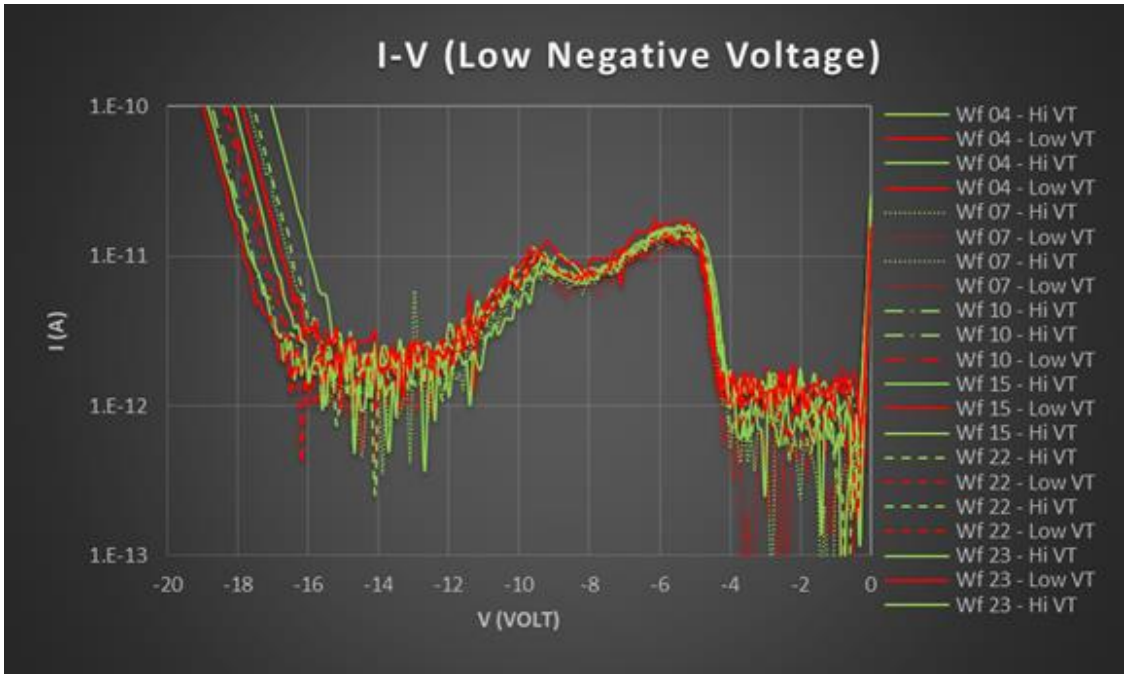

Fig. 61: I-V characteristic under negative bias

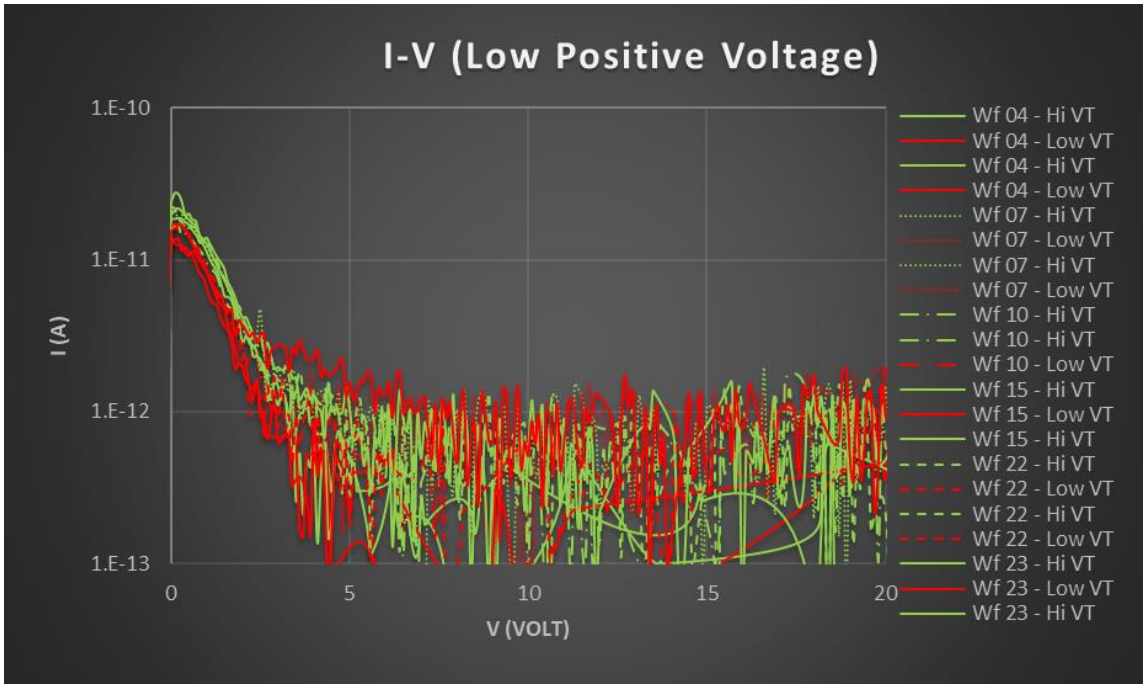

Fig. 22: I-V Characteristic under negative bias

To see any other difference between good and bad wafers F-N plots have been carried out for potential barrier extraction from poly (Fig. 23 and 24) and from SiC (Fig 25 and 26).

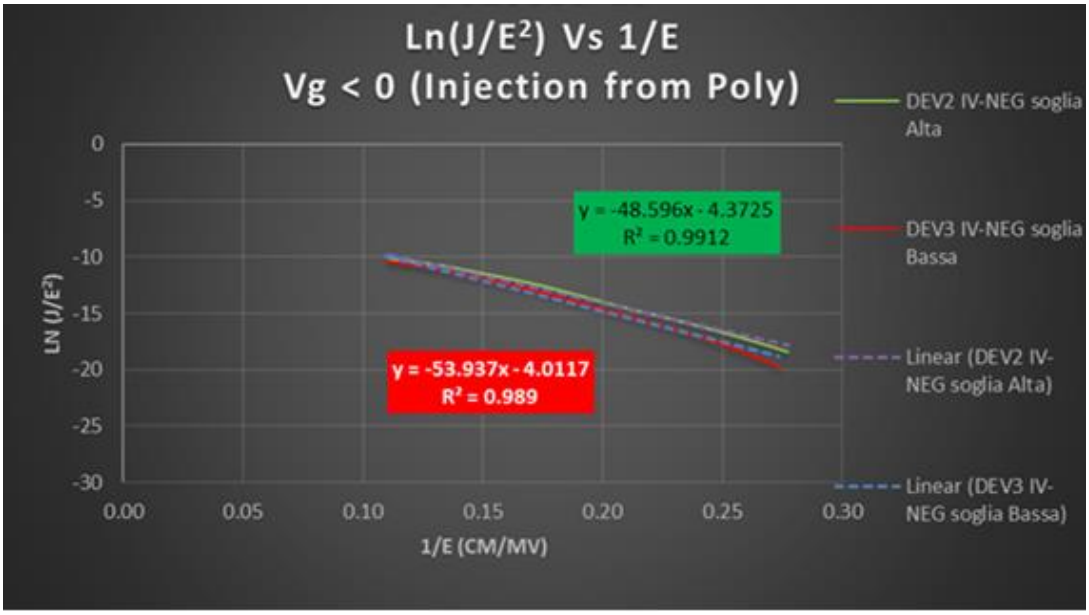

Fig. 23: F-N plot for electrons injection from poly

Wf		IV NEG	
		Low Vth	High Vth
4	ΦB (eV)	0.31	0.31
	THK (A)	533.8	547.2
15	ΦB (eV)	0.27	0.29
	THK (A)	555.1	547.4
22	ΦB (eV)	0.28	0.29
	THK (A)	540.4	529.9
7	ΦB (eV)	0.29	0.29
	THK (A)	551.0	548.9
10	ΦB (eV)	0.32	0.30
	THK (A)	552.7	535.4
23	ΦB (eV)	0.28	0.27
	THK (A)	522.9	528.4

Fig. 24: F-N plot for electrons injection from poly (Summary of results)

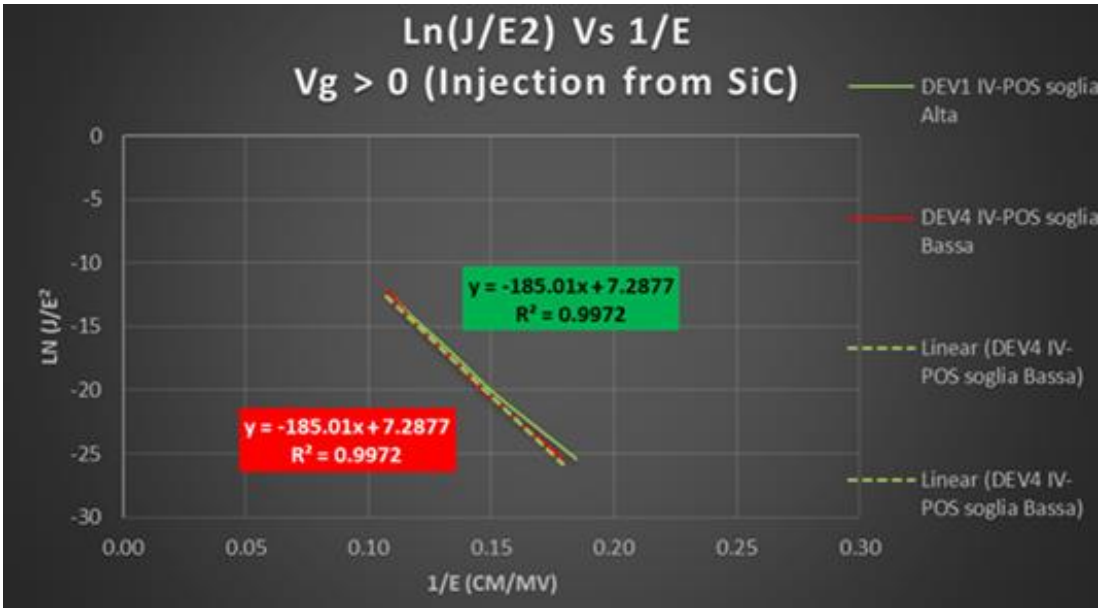

Fig. 25: F-N plot for electrons injection from SiC

Wf		IV POS	
		Low Vth	High Vth
4	ΦB (eV)	0.64	0.64
	THK (A)	544.1	542.4
15	ΦB (eV)	0.63	0.64
	THK (A)	553.2	537.7
22	ΦB (eV)	0.62	0.63
	THK (A)	538.8	539.5
7	ΦB (eV)	0.64	0.64
	THK (A)	544.4	544.3
10	ΦB (eV)	0.63	0.62
	THK (A)	553.3	536.5
23	ΦB (eV)	0.61	0.61
	THK (A)	541.5	523.4

Fig. 26: F-N plot for electrons injection from SiC (Summary of results)

No differences have been noticed between the two samples, confirming the hypothesis that the issue was not related to oxide or SiC/Oxide or Oxide/Poly interfaces.

At the end of this characterization a failure mechanism has been hypothesized as showed in Fig. 27. A positive charge inside the intermediate dielectric, coming probably from the chuck contaminated by $NiSi_2$, could anticipate the transistor threshold without impacting the gate oxide as known in previous studies [13].

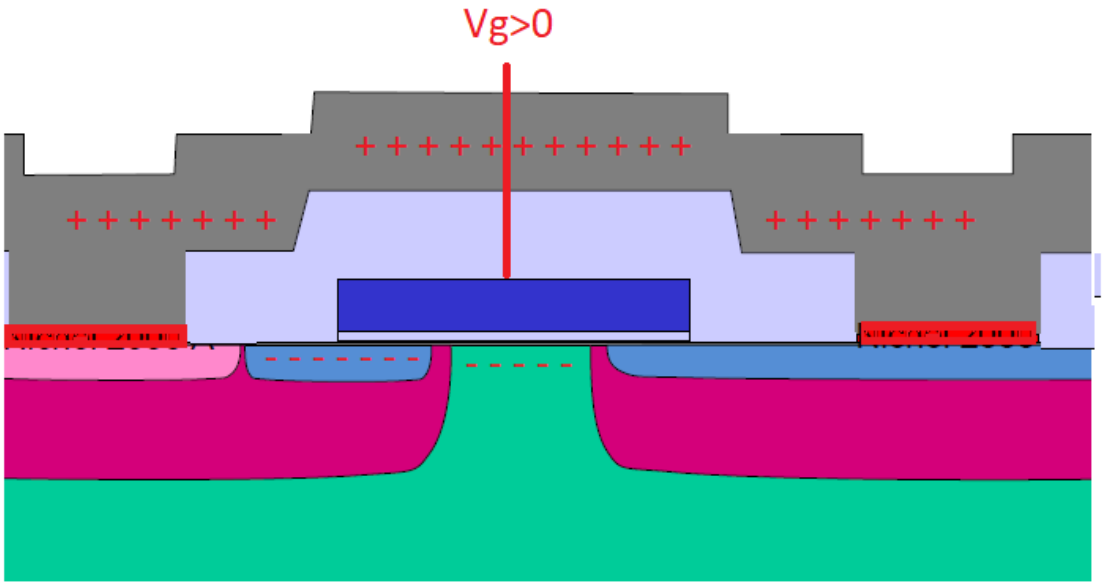

Fig. 27: Failure Mechanism hypothesized: Positive charge in the intermediate dielectric causes threshold lowering.

4.3.6 TVS on elementary structure

In order to study this possible contamination behaviour under temperature and stress a TVS test has been implemented on particular elementary structure Metal 1 on 5000A TEOS oxide on Poly (shown in Fig. 28). Comparing results between good and fail wafer in terms of powerMOSFET threshold.

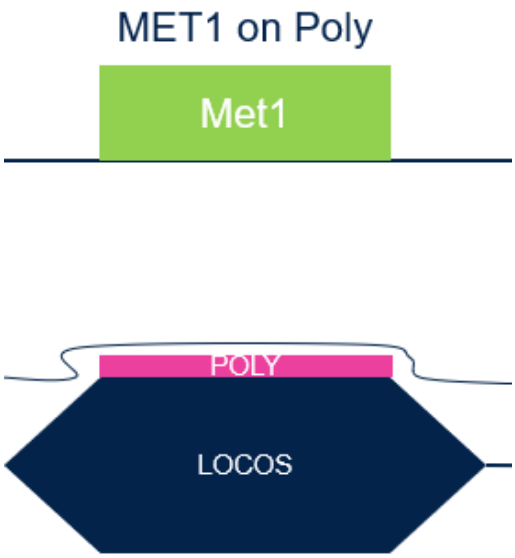

Fig. 28: MET1 on Poly Elementary structure

Even it is usually unlikely to apply this method to metal contamination, in terms of mobility this technique could be interesting on Nickel contamination study and diffusion.
The methodology, shown in fig 29, consists on a 200V bias at 300V applied on metal terminal for 15 minuts and then a slow ramp from 20V to -150V with the purpose to move the contamination in the film.

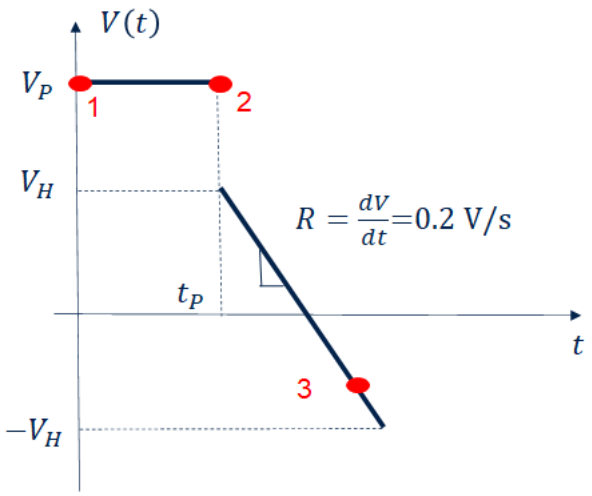

Fig. 29: TVS testing methodology. Metal terminal bias a 200V for 15 minutes and the a controlled ramp voltage bias from 20V to -200V

From the results showed in Fig 30 on wafer fail a difference in Capacitance under TVS test came out.
It could be related to TEOS oxide contamination, but it has to be confirmed with additional test on intentionally contaminated wafers.

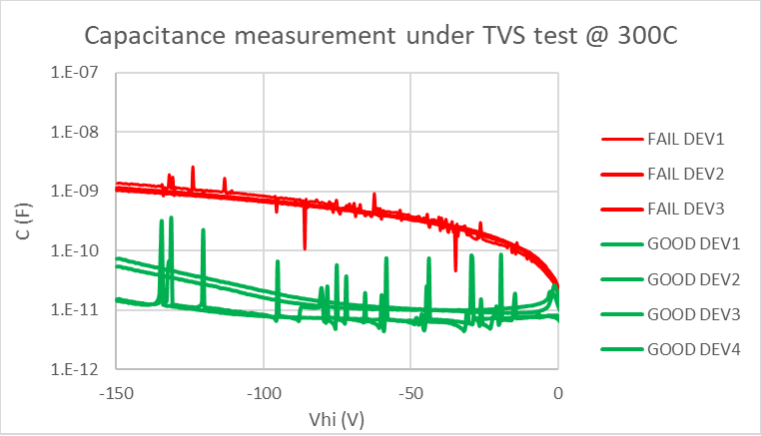

Fig. 30: TVS results under voltage sweeping at metal terminal at 300C

4.3.7 Results on Wafer intentionally contaminated

After the characterization on failed wafers, we ran the same set of tests on the intentionally contaminated wafer so that we could check if the same failure mode occurs. As shown in the Fig. 31, the VTC normalized to the initial value of the "HARD Low Vth" device (red dashed line), under positive stress current, decreases more than the "SOFT Low Vth" and "Low Vth" ones.

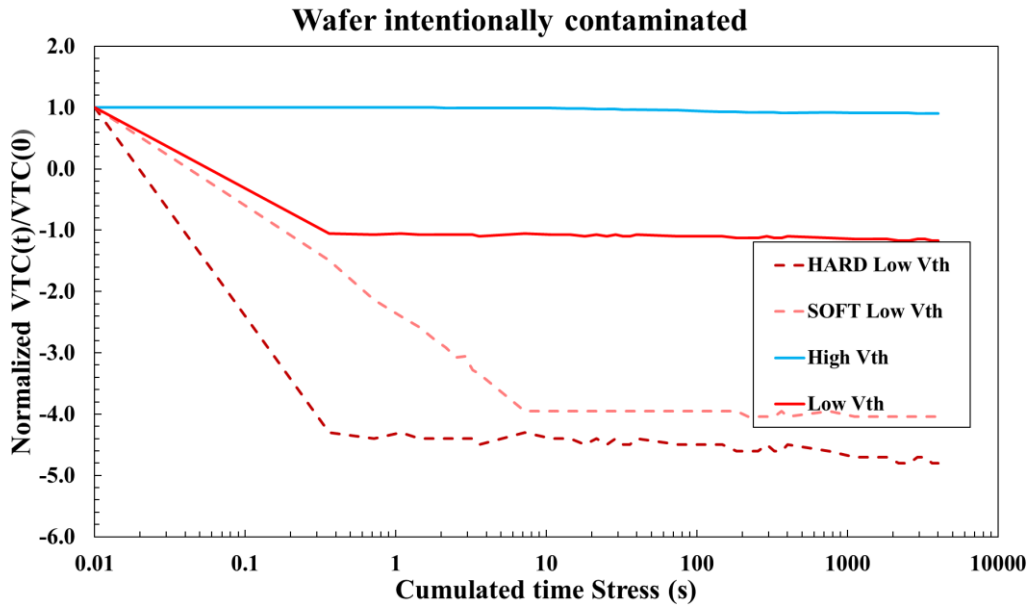

Fig. 31: the VTC normalized to the initial value under positive stress current.

In Fig. 32, the VTC of "HARD Low Vth" under negative stress current, at the end of the test improves the threshold.

On the other hand, the High Vth devices does not exhibit any drift after positive and negative stress.

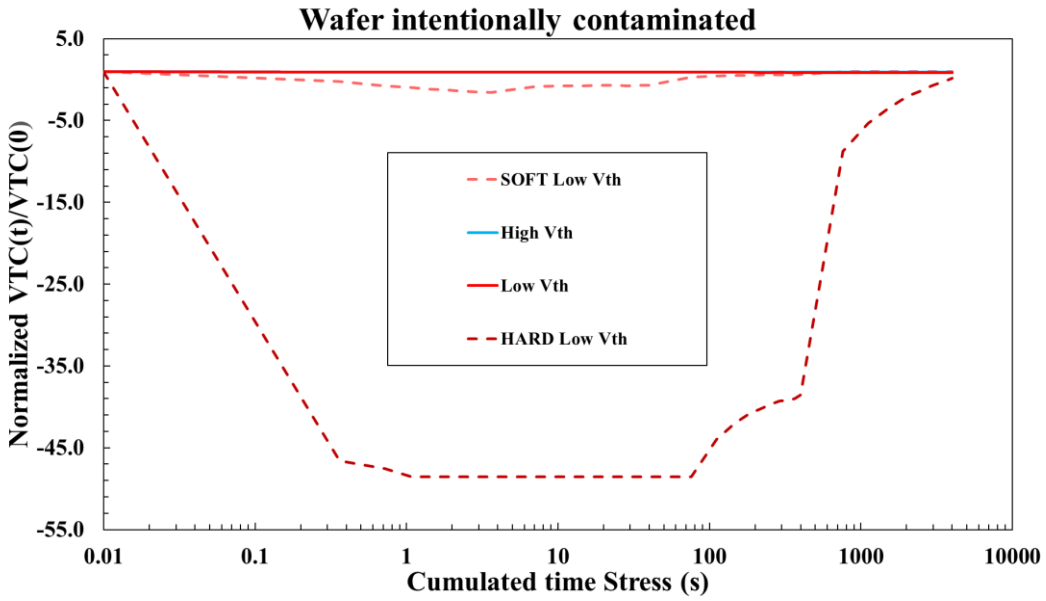

Fig.32: the VTC normalized to the initial value under negative stress current.

We performed also C-V measurements at 20 Hz and 100 kHz, as in the case of the process contaminated wafer, to observe possible states at the interface, as shown in Fig. 33 and Fig. 34.

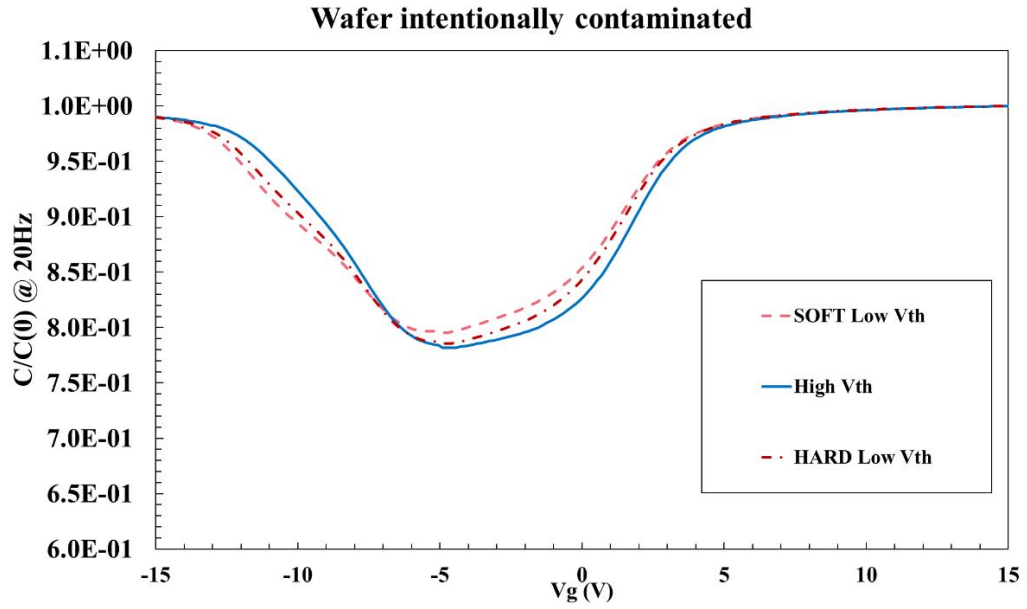

Fig. 33: C-V measurement at 20 Hz

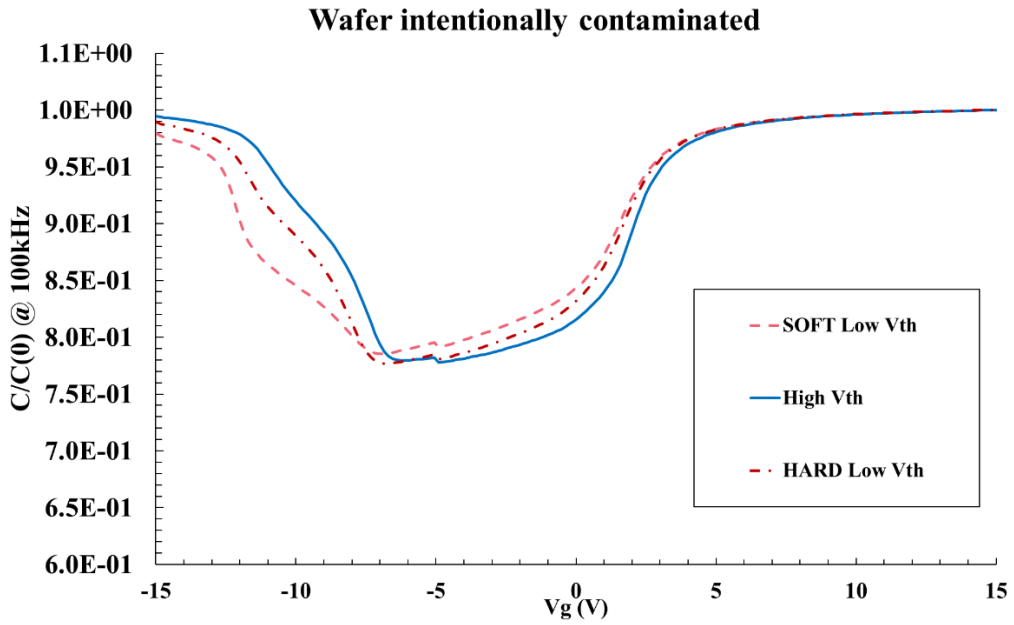

Fig.34: C-V measurement at 10 kHz

From C-V measurements normalized to the capacitance value in accumulation, the Hard and Soft Vth and high Vth are aligned, and it seems there are no states at the interface as the C-V characteristics are not shifted or distorted.

We also analyzed the Fowler Nordheim drift under CCS stress. As shown in Fig. 35 and 36 the Fowler-Nordheim tunnelling measured at +10 nA and -10 nA do not vary on all the samples for Fowler-Nordheim for negative stress as already showed in the failed processed wafers.

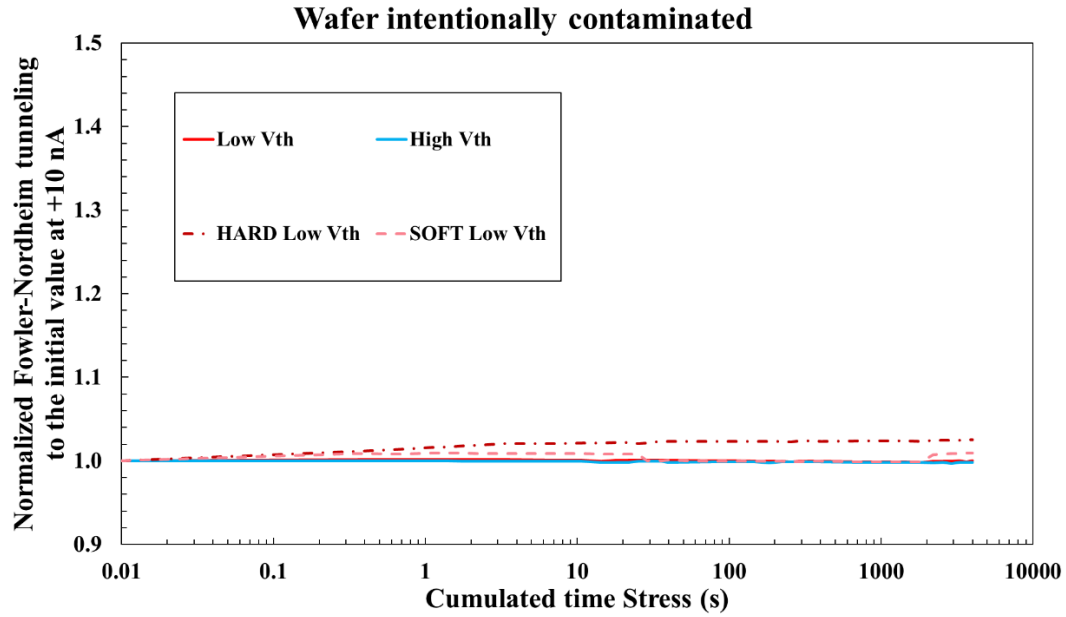

Fig. 35: Normalized Fowler-Nordheim tunneling to the initial value at +10 nA over cumulated time stress.

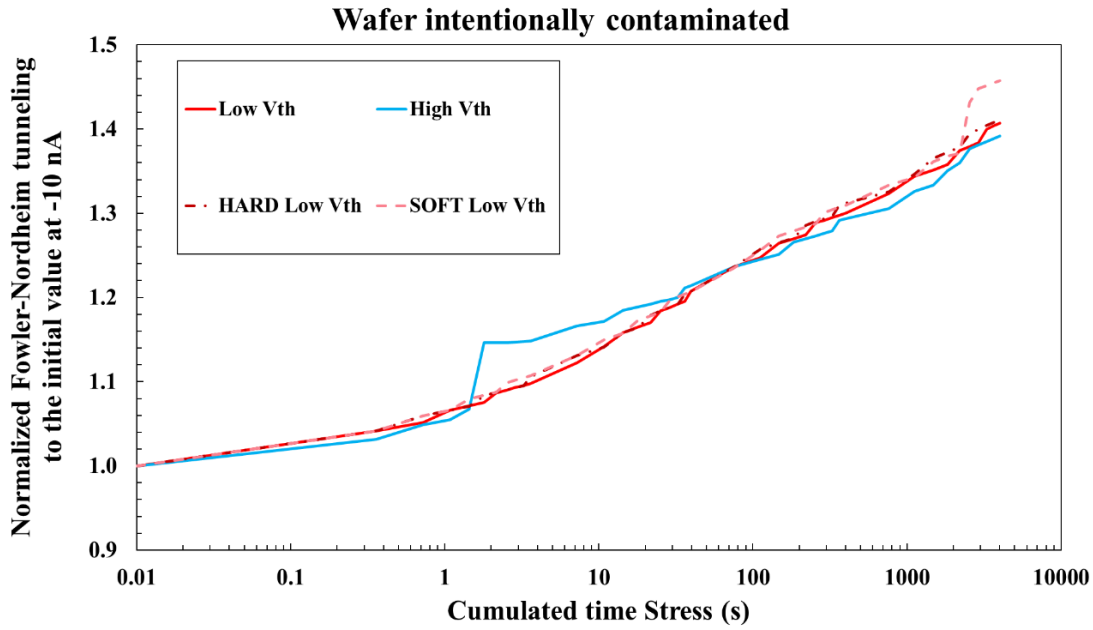

Fig. 36: Normalized Fowler-Nordheim tunneling to the initial value at -10nA over cumulated time stress.

This means, that with the intentionally contaminated wafers we reproduced not only the threshold lowering but also the failure mode of failed processed wafers where it is possible to trigger the threshold voltage by CCS stress without any effect on CV or FN conduction.
Moreover, as shown in Fig. 37, we can reproduce, by the method of DiMaria and Stasiak [14] an ideal gate oxide cross section where the charge is trapped inside the gate calculating the position of the maximum charge trapped inside the gate oxide on all the tested samples.

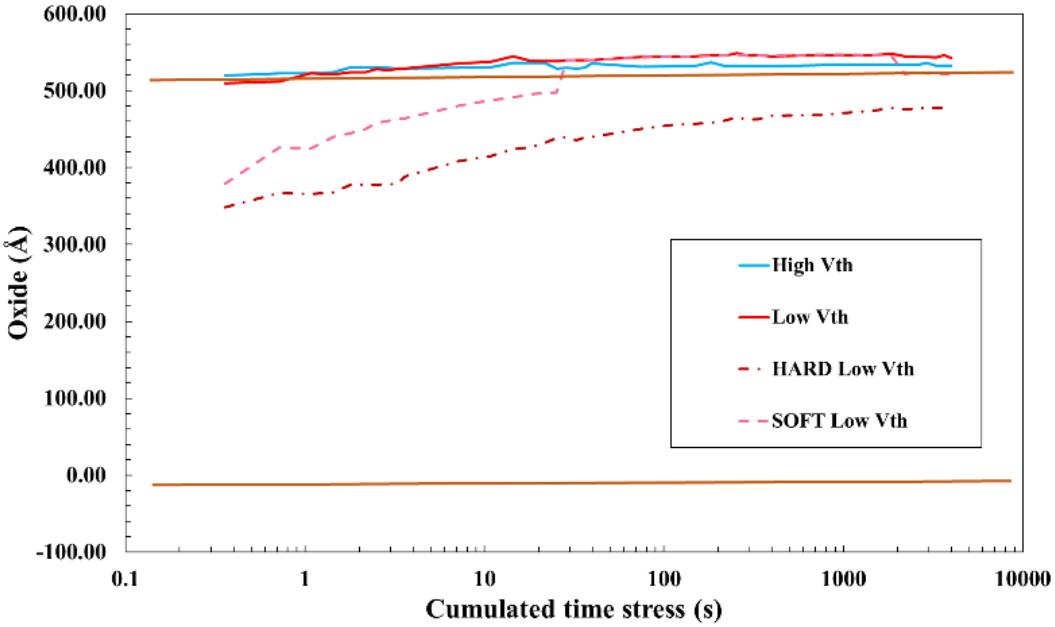

Fig. 37: DiMaria and Stasiak method to determinate the centroid of the maximum trapped charge. This method shows the evolution of the trapped charges in the gate oxide, whose cross section is represented in the ordinate.

It is also possible by the same method, as shown in Fig. 38, the evaluation of the trapped charge as the stress goes on. From this calculation there are no evident differences on the amount of charge trapped in the oxide in the different samples. Therefore, inside the oxide, it does not seem to be collected the positive trapped charge coming from the contaminated intermediate dielectric.

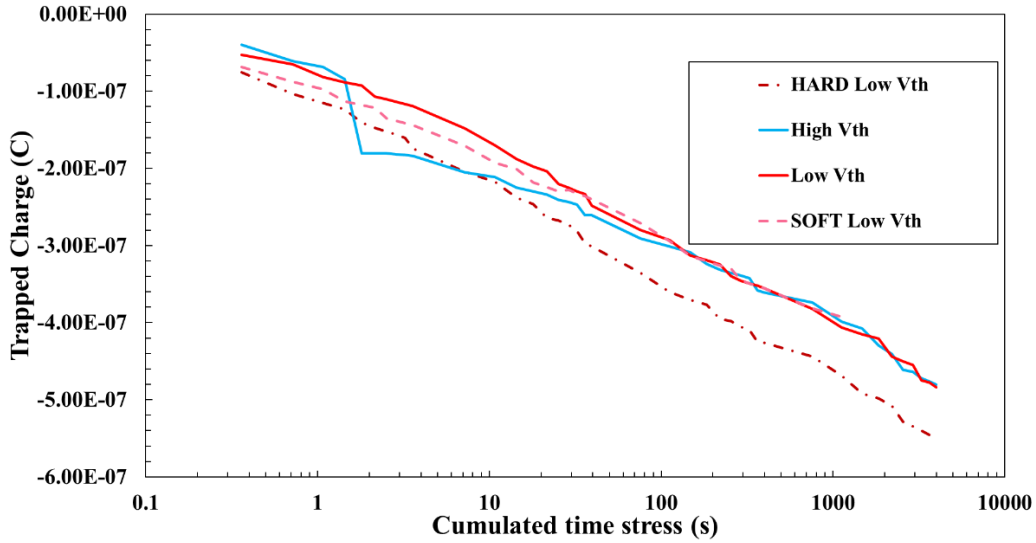

Fig. 38: Trapped charge in the gate oxide through DiMaria and Stasiak method.

4.3.8 Results on Wafer intentionally contaminated

The failure mode related to the 4H-SiC PowerMOSFET transistor threshold reduction has evaluated and it has been supported and refined through a positive and negative Constant Current Stress on gate electrode sensing the threshold, Fowler-Nordheim conduction and C-V test.

It helped to hypothesize the root cause of failure, related to a Nickel cross contamination coming from the metal sputtering chamber, and subsequently incorporated in the intermediate dielectric.

Then the cross contamination induced by metallization process in a metal sputtering chamber, has been validated through an induced and controlled contamination method on a TEOS layer deposited on a 4H-SiC PowerMOSFET.

The intentionally controlled contamination did not affect the PowerMOSFET gate oxide bulk and its interface as in the real process contaminated conditions.

Not only the threshold reduction has been reproduced on contaminated wafers but also the significant signal of its instability under CCS, this seem to be the significant failure mode and fingerprint of the effect of the contamination at Intermediate Dielectric (IMD) layer.

4.4 NIOTS (Near Interface Traps) treatment by POA (Post Oxidation Annealing) in Nitrogen and electrical techniques of characterization

The reduction of the defect density D_{it} at the SiC/SiO_2 interface is a critical aspect in the realization of 4H-SiC MOSFETs with high channel mobility. The growth of oxides in NO or N_2O and/or the post-oxidation anneal of deposited oxides in the same gas atmospheres has proven to be more effective in the reduction of D_{it} rather than the oxidation in O_2 [15,16,17] to achieve higher field-effect mobility in MOS transistors [4,5]. These improvements are due to the reduction of the density of fast interface states [18, 8], either by physical removal or passivation of π-bonded carbon from the interface by nitrogen [19, 20, 21]. Carbon may be present in two configurations, namely, as sp2-bonded clusters with a wide energy gap responsible for interface states in the energy range from the top of the SiC valence band to the middle of the energy gap and as graphite-like clusters providing the interface states over the entire SiC energy gap [22]. Near-interface states are as well reduced by nitridation. For these

reasons, the gate oxides investigated in this work have been realized with different processes, by depositing an oxide layer which was subsequently post-oxidized in N_2O or NO gases.
In this chapter the outcomes of these experiments are presented and discussed in the light of the current understanding of SiC interface passivation and nitridation. The characterization methods introduced in Chapter 3 are extensively employed for the analysis of MOS capacitors and MOSFETs: the extracted MOS parameters are used to evaluate the effect of oxidation processes on the electrical quality of the SiC/SiO_2 interface.

4.4.1 Gate oxides grown or annealed in N_2O or NO

The direct oxidation of SiC in dry O_2 leads to poor electrical performance [4] and presents a technological issue: the growth of an oxide layer of a certain thickness on 4H-SiC is a very slow process as compared to Si and occurs at much higher temperatures. In Si technology usual oxidation temperatures are in the range of 900°C to 1000°C, while for SiC are well above 1100°C in most cases and are strongly dependent on the SiC crystal orientation. To reduce the interface states the nitridation approach (and its various declinations) has been widely accepted and employed in the fabrication of 4H-SiC MOSFETs with higher channel mobilities. This consists in the oxidation or postoxidation (sometimes called re-oxidation in the literature) of oxide layers in N containing gases such as NO or N_2O [20,21]. The direct growth of an oxide in NO or N_2O is even a slower process as compared to dry O_2 and occurs in reasonable times at very high temperatures (in the range of 1200°C − 1300°C). Thus, to reduce the thermal budget (time × temperature) of the oxidation process it is convenient to "quickly" grow an oxide in dry O_2, or to deposit it by a Chemical Vapor Deposition (CVD) method, and subsequently post-oxidize it in N-rich atmosphere [23,18]. MOSFETs with CVD oxides have also shown superior characteristics compared to the thermally grown oxides in terms of effective mobility, probably because less oxidation occurs and thus less carbon must be removed during this process.

4.4.2 Sample preparation

The power MOSFET transistors that we characterized in this work are manufactured using 6" wafers on n-type (0001) 4H-SiC 350 μm thick substrate doped to an effective carrier concentration of 4-5E18 cm^{-3} and resistivity of 0.012-0.025 Ω*cm. The n-epitaxy layer is 6 μm thick and doped to $1.5E^{16}$ cm^{-3}. On the epitaxial layer, a 50-nm-thick oxide has been

deposited through a Low Pressure Chemical Vapor Deposition (LPCVD DCS) in a High Temperature Oxidation (HTO) furnace in dichlorosilane (SiH_2Cl_2) ambient. This process is followed by a Post Oxidation Annealing (POA) performed on horizontal furnaces to nitridate the SiC/SiO_2 interface. Two different processes of POA have been selected for this work, using identical temperature ramps, but different gaseous precursors in N_2O or NO environment with an annealing temperature in the range of 1150-1300°C. In both POA processes, NO molecules are responsible for the interface nitridation. When NO is generated from N_2O molecules pyrolysis, a certain amount of N_2 and O_2 is also produced

generating a not desirable interface oxidation. The total mutual amount of N_2, O_2 and NO produced by N_2O pyrolysis is also affected by many process parameters which often are very difficult to keep under control. On the other hand, NO molecules are very stable when temperature is less than 1300°C. Before defining an oxidation flow, several deposition and post oxidation annealing process trials have been processed on blanket wafers. Then, dynamic TOF-SIMS analysis profiles [a] exhibiting the peak concentration of the nitrogen at the SiC/SiO_2 interface was used to define the desired reaction time, which has been set in order to obtain the N concentration peak of about 7E20 at/cm^3 as reported in Fig. 39.

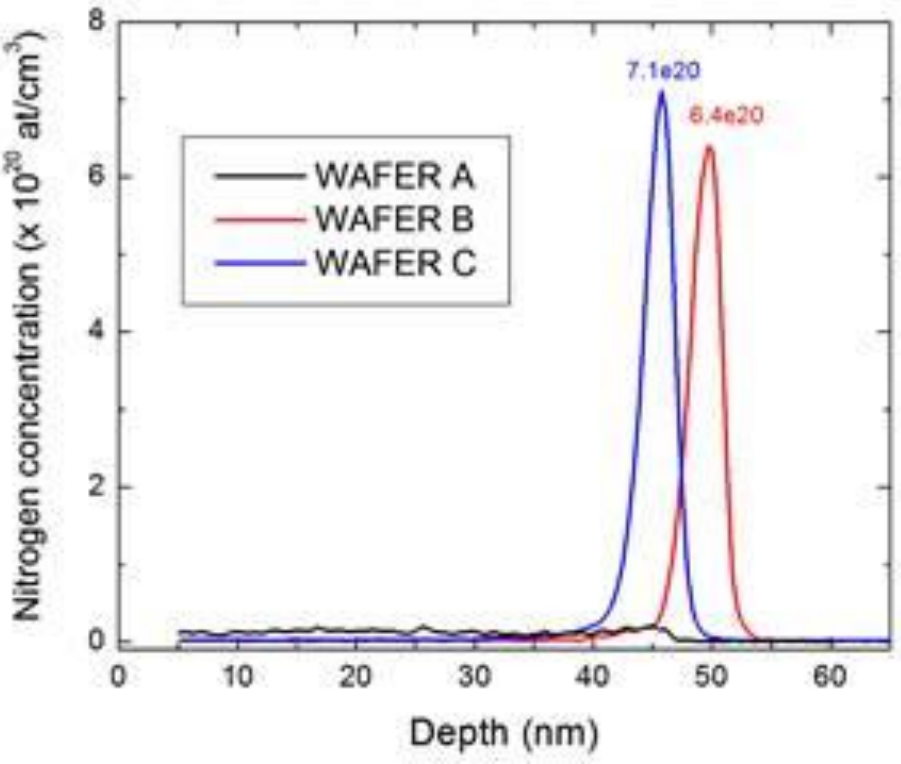

Fig.39: Dynamic TOF-SIMS profiles comparison between NO and N2O Post oxidation annealing

All the data reported in this paper have been recorded using a MPI TS2000-DP semi-automatic probe station equipped with a Keysight B1505A device analyzer with an external LCR Keysight E4980 meter dedicated for capacitance/conductance voltage (C-V/G-V) measurements and a high power source measure unit for current voltage (I-V) testing. Several electrical techniques targeted either to charge trapping analysis or dielectric breakdown have been employed.

4.4.3 Charge-Sensing method under constant current stress

We provide evidence of the better annealing of interface traps using NO POA by employing Constant Current Stress (CCS) from both power MOSFET interfaces (poly-Si to SiO_2 and SiC to SiO_2). The commonly used methods [24,7] to determine interface traps effects and to evaluate and calculate the density of states are related to the analysis of the G-V data obtained at different frequencies (20Hz to 1MHz). The advantage to test directly on the MOSFET structure, instead of the capacitors available on the test element group (TEG), is the lack of availability of minority carriers on the latter. In particular, C-V measurements have been carried out starting by a very slow ramp rate of around 60mV/s assuming to stimulate the charge de-trapping from the levels inside the SiC bandgap. The most significant results are obtained from the C-V and the G-V measurements performed at 20Hz, with an oscillation amplitude of 1V where conductance peaks are detected between -5V and -10V for Vgs (Fig. 40).

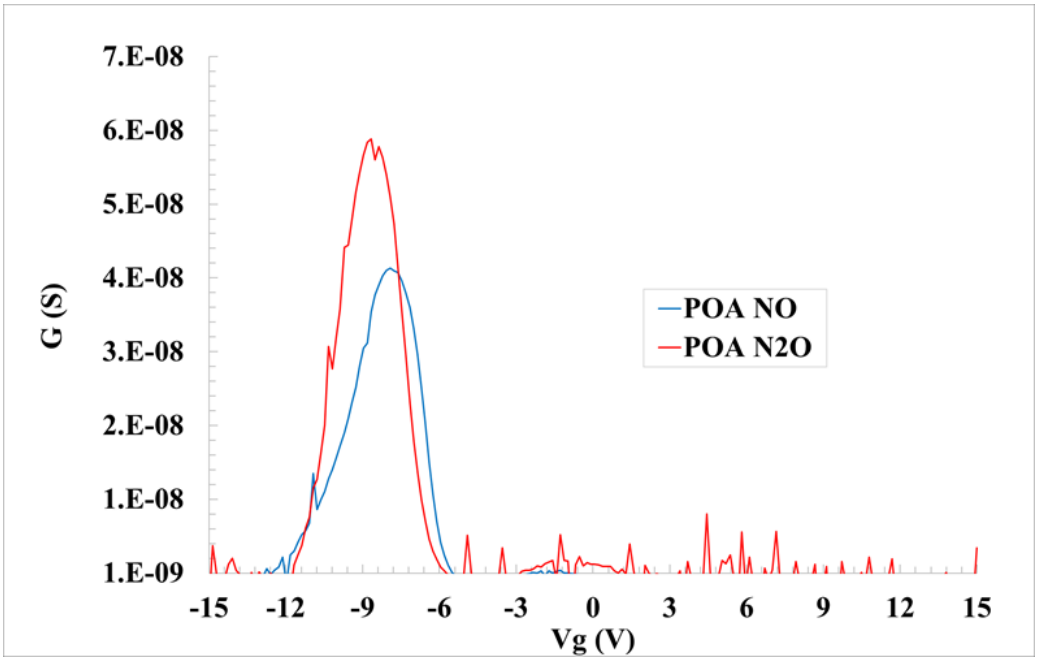

Fig. 40: 20Hz G-V Characteristics comparison between N2O vs NO samples

This test provides a qualitative reference for a quasi-static I-V test in a voltage regime not critical for gate charge injection in the gate oxide. The nitridation efficiency is then correlated to the reduction of traps in the SiC bandgap and the peak displacement gate current [25] as shown in Fig. 41.

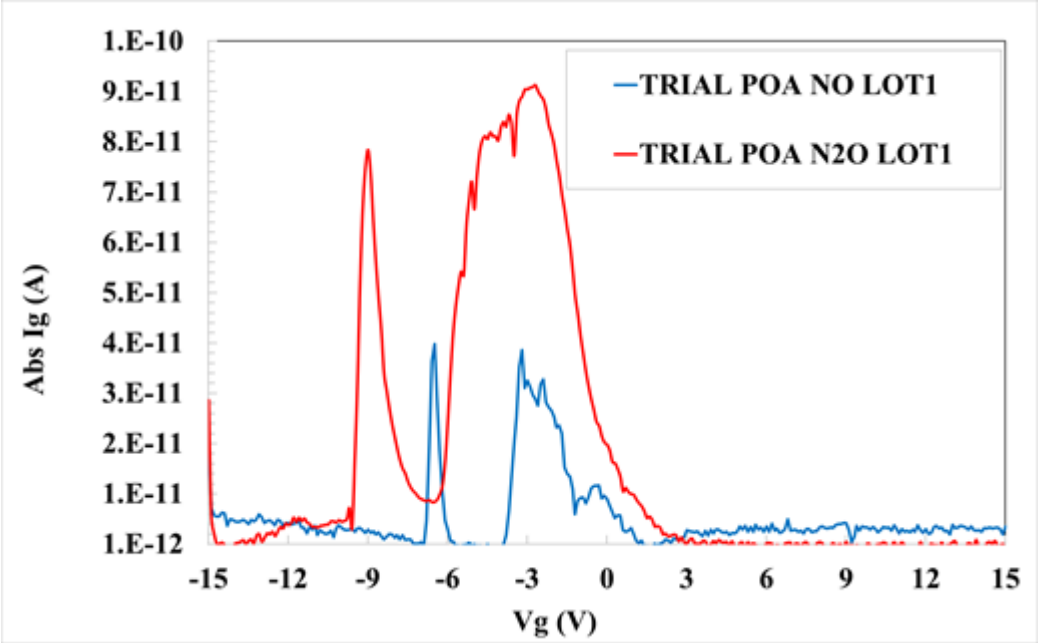

Fig. 41: I-V Characteristics comparison between N_2O vs NO samples. Peaks from N_2O sample are higher and wider than NO one

Compared to the GV data at 20Hz, the I-V measurements exhibit sharper peaks. At a first sight they could be addressed to current leakage but rather they must be related to drift or displacement current due to the interface states capacitance variation when they trap charges. In particular, the data for NO samples exhibits sharper peaks whose height is significantly lower than for N_2O samples. We attribute this to a better saturation of the dangling bonds at the SiC/SiO_2 interface, reducing charge trapping/de trapping due to interface defects. Hence, we can state that we have a qualitative nitridation efficiency evidence by the I-V current peak. Based on this result, the study was extended to 5 wafers from 5 different lots using either the NO or the N_2O POA process. As the I-V test does not damage the device under test, the wafer can remain in the line and follow subsequent processing. From Fig.42, it is confirmed that not only the peak shape and the intensity of the two processes, but also the reproducibility of the N_2O POA can be demonstrated using the I-V ramp. The data obtained from N_2O POA samples shows peaks varying in voltage and intensity. This is related to the difficulty to provide a constant, stable, and reproducible amount of N_2, O_2 and NO during N_2O pyrolysis at different process times (lot-tolot variability). In contrast, the I-V characteristics for wafers coming from the same lot exhibits a low variation.

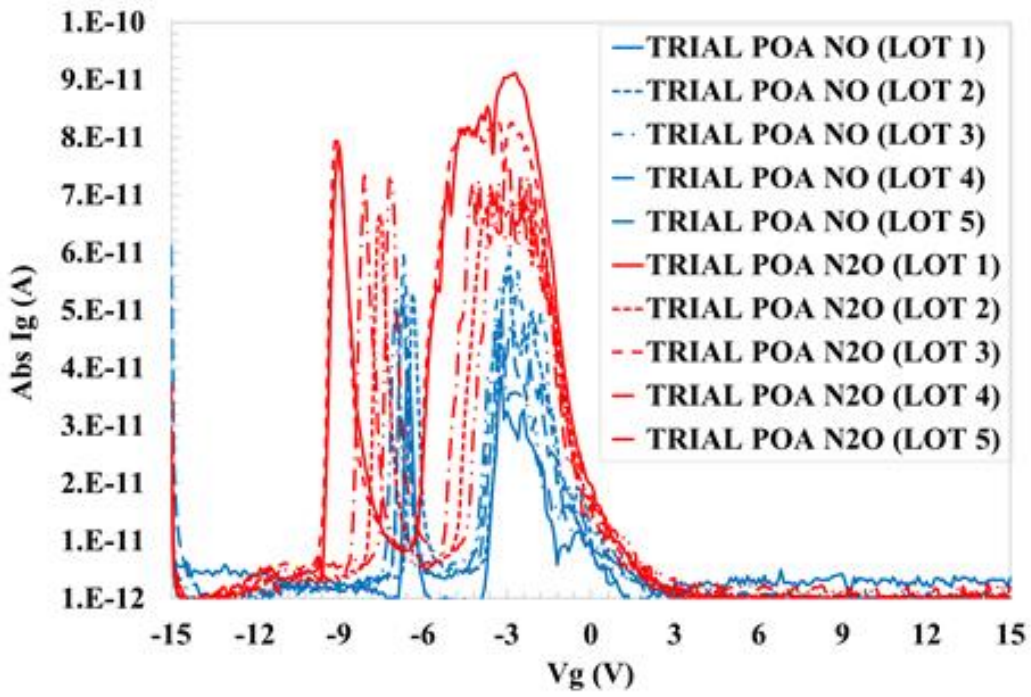

Fig. 42: I-V Characteristics comparison between N_2O vs NO samples. It is an evidence also of NO process stability

We now demonstrate that the charge sensing techniques, which are commonly used to track and spatially locate the trapped charges (both positive and negative) in the gate oxide bulk, are is also efficient to track also the trapped charge as a function of the injected electron fluence at SiC/SiO_2 interface. The stress between two readouts increases according to a power law starting from 360ms to 3600s per single stress pulse. The estimated trapped charge and the position of the charge centroids, as function of the cumulated current stress time following the method shown by DiMaria and Stasiak [14].

The method consists in alternating measurement or sensing test and stress test injecting charge in a specific gate oxide interface (With polysilicon or Silicon Carbide epitaxy). The correct choice of the sensing test is fundamental to isolate the contribution of interface states from the traps located inside the gate oxide bulk or from the charges or contamination sources present in the intermediate isolation dieletric.

Results have been shown in Fig. 43. Here, the charge sensing method probes the charge centroid for the N_2O POA near the interface and confirms the lower efficiency in the treatment of near interface oxide traps (NIOTs) compared to the NO process. The chart represents an ideal gate oxide cross section between SiC and the poly-silicon contact. The dashed lines represent the gate oxide thickness which is higher for the N_2O process, as it provides a thin oxidation layer at the SiC/ SiO_2 interface.

Definitely this technique allowed to detect with an high precision how the injected charge is trapped in the gate oxide and the higher trapping annealing properties of NO POA at SiC/SiO_2 interface.

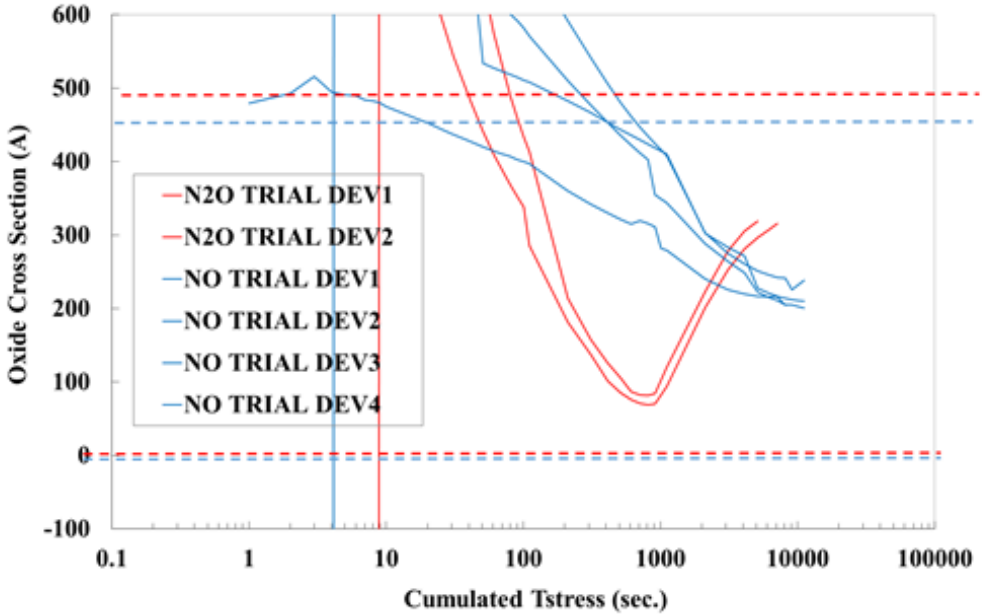

Fig. 43: Centroid Charge trapped evolution under Constant Current Stress Injection on both samples in an ideal 470Å (POA NO) /500Å(POA N_2O) nitridated gate oxide cross section.

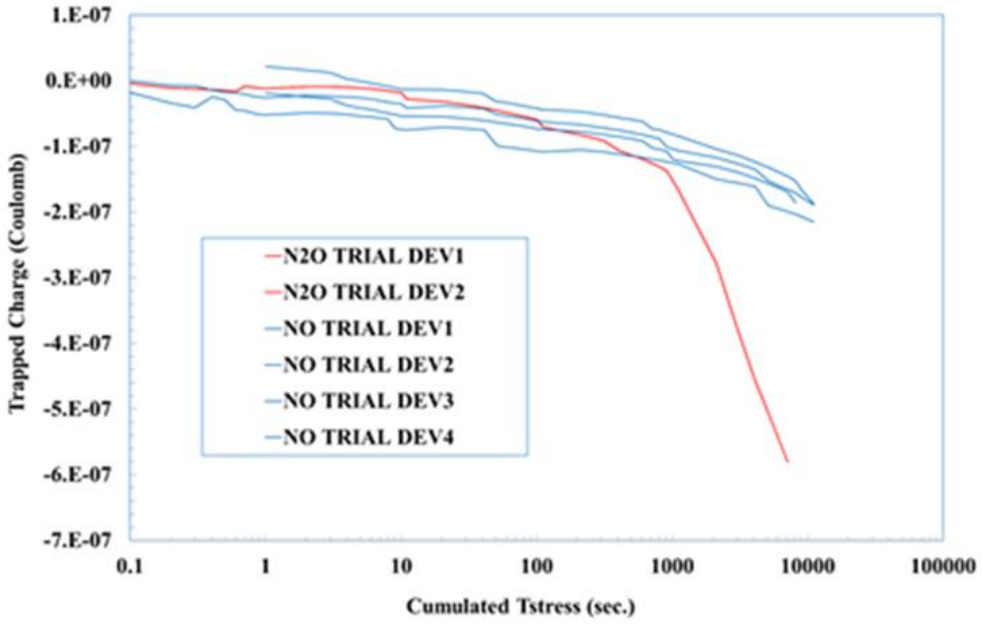

Fig. 44: Charge trapped under Constant Current Stress Injection on both samples. After 10ks stress an higher negative charge is trapped in the N_2O Sample

4.4.4 TDDB Test

To complete the characterization, and to confirm the findings of a higher reliability for the NO POA, a Time Dependent Dielectric Breakdown (TDDB) test under Constant Voltage stress (CVS) at 200°C and 9MV/cm and 9.5MV/cm has been performed. In Fig. 45, we present the cumulative failure distribution collected under 9MV/cm constant gate field stress at 200ºC for both samples. The study then allows us to determine the gate oxide resistance and leakage evolution under accelerated conditions such as high voltages and high temperatures. They provide a first evaluation of the reliability improvement caused by the NO POA process.

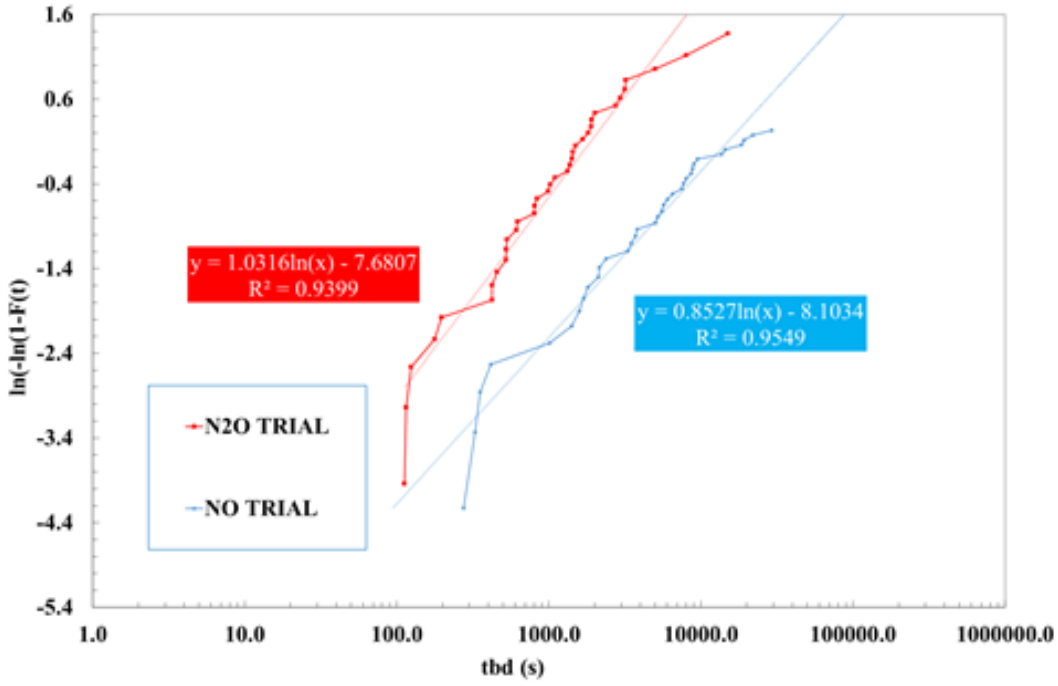

Fig. 45: Cumulative failure distribution of time to breakdown under constant field stress at 200ºC

The hypothesis of a better effect of the nitrogen induced by NO process near the SiO_2/SiC interface has been validated by the C-V test and by the analysis of the peaks detected by Ig-Vg and the mobility data provided by EWS (Electrical Wafer Sorting) on all the devices. The data are summarized in Table 2.

	Thickness	DUTs	t_{bd} (s) under 9MV/cm 200ºC	Channel mobility (cm/Vs)	I-V peak (A)	Position of trapped charge
N_2O	500Å	36	1719	41	~85pA	~30 Å
NO	470Å	48	14609	52	~40pA	~200 Å

Table 2: Significant results for the experiments under analysis

The tests provide a useful and easy method towards an efficient monitoring of the reduction of interface states. Furthermore, Fowler-Nordheim conduction as a function of the stress time is correlated to the charge centroid in the investigated POA schemes. The effects of different POA processes on the gate oxide lifetime is investigated. Finally, the reduced amount of charges obtained by NO POA allowed to achieve the best performance under high voltage stress, improving the time to breakdown. Charge distribution obtained for different POA is correlated to the resulting oxide lifetime. For all the above reasons, the NO POA process is strongly recommended in a production line.

Furthermore, we demonstrate that a simple I-V test in a gate voltage range lower than Fowler-Nordheim conduction can be used for in-line monitoring of the nitridation efficiency.

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Conclusion

As deeply discussed, the reduction of defectivity in Silicon Carbide is one of the main topic to improve the devices quality and reliability. In this thesis work, we investigated several techniques for identifying and characterizing defects in gate oxide and at the SiO_2/SiC or SiO_2/Si interface. This study has made it possible to improve the processes, such as oxidation and metallization, involving the production of SiC or Si devices. In particular, electrical measurement methods have made it possible to observe where, in the device, the defects are present, whether they are extended or contaminants. This information is fundamental in a production line because in this way it is possible to understand which process step was not successful. Furthermore, these methods have been useful to both characterize a new process compared to a standard one (such as POA in NO and POA in N_2O) and also, through an in-depth study of comparison between the various methods, to use a simple measurement such as I-V measurements in non conduction region to evaluate the peaks due to the interface states density without resorting to more demanding measurements, such as C-V and G-V measurements. It would be interesting, in the future, determinate the location of the states at the interface in the bandgap, transforming peaks obtained from measurement IV into a signal expressed in eV. It would also be useful to do a qualitative analysis of the peaks, so as to be able to identify the contaminants. For this purpose, DLTS signals can be used, which, based on the activation energy associated with the peaks, to give information on the elements that contaminate that given material.

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