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Thermal management characterization for 4H-SiC power devices: modeling, optimization, and analysis.

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Abstract

The growing demand for efficient and reliable power management solutions in electric vehicles has led to the emergence of innovative technologies based on silicon (Si) and silicon carbide (SiC). These semiconductor materials offer significant advantages, such as high electrical resistance, excellent thermal conduction, and the ability to operate in high temperature environments. The above features make them ideal for high-power applications, including inverters, high-speed on-board chargers based on high-performance MOSFETs and diodes.

For example, on-board chargers face peculiar thermal challenges in order to ensure reliability and durability in the automotive framework in the presence of harsh environments. Power losses can occur during the switching phase in the circuit and can cause a significant temperature rise inside the cabinet, compromising the all system lifetime. Therefore, it is essential to develop effective thermal strategies to manage and dissipate the heat generated during the operation of chargers.

During the thesis work, a scalable fast charger solution for automotive applications, capable of managing a power flow of 7 kW, was studied and proposed. In order to accurately assess the high temperatures reached by the active silicon and silicon carbide devices during normal operation, at steady

state and at the maximum permissible power, an extensive thermal simulation using COMSOL Multiphysics will be conducted.

COMSOL Multiphysics is a sophisticated simulation software that provides an advanced modeling environment very suitable for addressing the study of the thermal behavior of Si and SiC devices in the proposed charger. Using the software, it will be possible to evaluate the overall thermal performance of the system and get the heat dissipation and temperatures reached inside the devices in different operating conditions. The model obtained can be used to evaluate the reliability and lifetime of the inverter.

To support the market requirement, the production of ever greater volumes of SiC devices is required. This point is reflected in the production process which requires to be optimized not only to obtain high devices performance, but also to optimize production yield and thus satisfy market demands.

Among the different steps involved in the device production, we focused on the Wafer Level Annealing (WLA) technique that is largely was explored in order to study the thermal stability of 4H-SiC silicon carbide substrates. This represent a thermal process which take place after the growth of SiC substrate before epitaxy. WLA involves controlled treatments at temperatures below 1600 ºC in the argon atmosphere. Using some characterization techniques such as Micro-Raman spectroscopy, atomic force microscopy and Electrostatic Force Microscopy. It will be possible to study the effect of heat treatments on the crystallographic structure of SiC

substrates. Special attention will be paid to the graphitization process that can occur during heat treatments, which leads to SiC devices failures.

The above represents a small contribution to the progress of power applications based on silicon carbide technology and may suggest a path to new innovative solutions in the field of power management in electric vehicles. This will contribute to the advancement of power applications based on silicon carbide technology and pave the way for innovative new solutions in the field of power management in electric vehicles.

Chapter 1

Revolutionizing Electronics: The Rise of wide bandgap semiconductors

In the framework of modern electronics, the consistent pursuit of enhanced performance, efficiency, and reliability has ushered in a new era of semiconductor materials. Silicon, the backbone of the electronics industry for decades, has reached its limits in terms of power handling, thermal management, and frequency operation. As electronic devices continue to evolve and find applications in increasingly demanding fields such as electric vehicles, renewable energy systems, and high-frequency communication, the quest for more advanced semiconductor materials has become imperative. Two candidates have emerged at the forefront of this revolution: silicon carbide (SiC) and gallium nitride (GaN). Their exceptional physical properties and unique characteristics are propelling them to the forefront of semiconductor technology, poised to replace traditional silicon technology and unlock a new era of innovation.

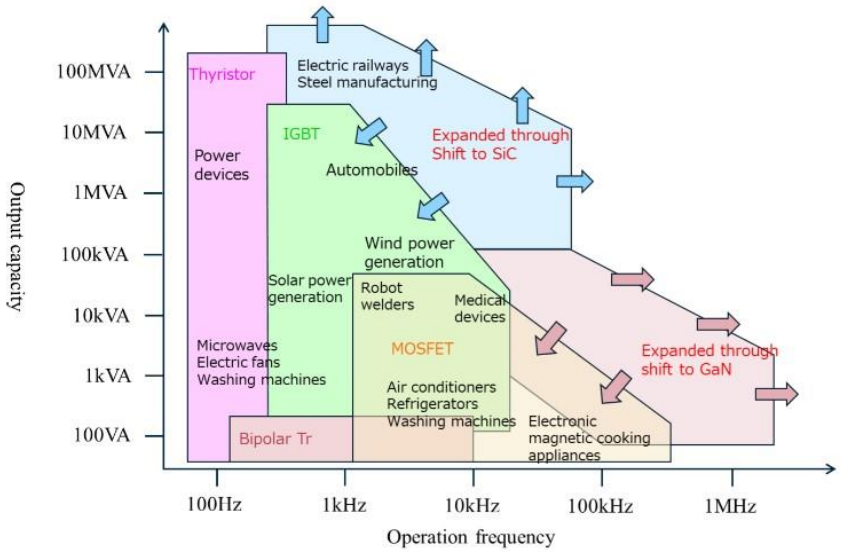


Fig.1.1 SiC market integration and applications

The rise of Silicon Carbide

Silicon carbide, a compound consisting of silicon and carbon, has long been recognized for its extraordinary properties. Originally discovered in the late 19th century, SiC found limited use due to the challenges associated with its production and processing. However, recent advancements in material science and manufacturing techniques have rekindled interest in this remarkable material.

Exceptional physical properties

One of the primary factors driving the adoption of SiC is its exceptional physical properties. SiC exhibits a wide bandgap, a measure of the energy required to move electrons from the valence band to the conduction band. This attribute makes the SiC highly suitable to work at high temperatures and high voltage, making it ideal for high-power and high-temperature applications. Unlike traditional silicon-based devices, SiC devices can operate efficiently at temperatures exceeding 600 degrees Celsius, making them particularly well-suited for aerospace, automotive, and industrial applications.

Efficiency and power handling

SiC's unique properties extend beyond high-temperature resilience. SiC semiconductors possess higher electron mobility than silicon, enabling faster switching speeds and reducing energy losses during operation. This high-speed switching capability translates into improved efficiency and reduced power consumption, crucial factors in contemporary electronics. Furthermore, SiC's capability to handle higher voltages and currents compared to silicon counterparts enhances its utility in power electronics, enabling the development of compact and efficient power converters for electric vehicles and renewable energy systems.

Enabling electric mobility and renewable energy

The automotive industry is undergoing a transformative shift toward electric vehicles (Evs) as concerns about fossil fuels and emissions mount. SiC's suitability for high-power applications and its inherent efficiency have positioned it as a pivotal technology in the

EV revolution. SiC-based power electronics offer higher efficiency and reduced cooling requirements, thus extending the driving range and enhancing overall performance of electric vehicles. Additionally, SiC's high-temperature stability ensures reliable operation in the harsh conditions found within automotive powertrains.

Renewable energy systems, such as solar and wind power, also stand to benefit from SiC technology. The ability to operate at high temperatures enables SiC-based inverters to handle the rigorous demands of power conversion in renewable energy installations, improving overall system efficiency and minimizing maintenance needs.

Miniaturization and power density

The miniaturization of electronic components and systems has been a driving force in the semiconductor industry. SiC's high electron mobility not only facilitates high-frequency operation but also allows for the creation of smaller, more compact devices. SiC-based transistors can be designed with smaller footprints, leading to increased power density, and reduced overall system size. This characteristic is particularly significant in applications such as space-constrained consumer electronics and satellite communication systems.

The shift away from silicon technology: a paradigm transformation

The transition from traditional silicon technology to silicon carbide and gallium nitride represents a paradigm shift in the electronics industry. While silicon has served as the foundation for countless innovations, the emergence of SiC and GaN signifies the industry's need to overcome limitations and embrace materials that can meet the demands of the future.

Overcoming Si limitations

Silicon's dominance in the semiconductor industry has been built on its ease of manufacturing, abundance, and well-established fabrication processes. However, as the requirements for higher efficiency, faster operation, and extended temperature ranges increase, silicon's inherent limitations become apparent. SiC and GaN have stepped forward to address these limitations, offering superior performance and efficiency in specific application domains.

Right after the mains disadvantages:

- Defects and dislocations in SiC and difficulties in the industrial procedure for themanufacturing of GaN.
- High costs.
- Relatively limited availability.
- No standard packaging technology for high temperatures SiC-devices.

The GaN, came after the SiC, and it is not widely used because of the cost, yield and reliabilityissues [19]. Although GaN-based devices offer a very high switching speed, thanks to the considerable mobility of the electrons. Nevertheless, the lower thermal conductivity, the limited power density potential and the lack of robustness make their use still not preferableto the SiC based devices. Moreover, the reduced natural dissipation capability, fundamental characteristic for high power converters, makes these devices unsuitable unless fluid coolingprocedures are used. This makes trickly their industrial production by requiring a more cumbersome and more expensive assembly. It seems clear that these devices, that must operate at high frequency and temperatures, require additional innovative design solutions to become effective from an industrial point of view.

Bridging the Performance

The pursuit of SiC and GaN technologies is not just a matter of replacing silicon; it is about bridging the performance gap that exists in various electronic applications. SiC's capability to handle high temperatures and high voltages allows for unprecedented power electronics efficiency, directly contributing to the global push for energy-efficient technologies. GaN's excellence in high-frequency operation and optoelectronic applications is reshaping how we communicate, illuminate, and interact with the digital world.

The Path forward

As SiC and GaN technologies mature and their manufacturing processes become more streamlined, their adoption across industries will accelerate. The transition to these materials requires collaboration between research institutions, semiconductor manufacturers, and end-users feedback to develop robust supply chains, optimized design

methodologies, and innovative solutions. Ultimately, the emergence of SiC and GaN marks not only a technological shift but also a reimagining of the possibilities that lie ahead in the world of electronics.

Chapter 2

Silicon carbide and its properties

SiC was discovered by Professor Jons Jakob Berzelius in 1823 at the Karolinska Institute in Stockholm. After that, SiC, also known as carborundum, was "discovered again" in 1891 by the renowned French chemist Henri Moissan. His discovery, however, occurred in an unusual way: not through laboratory experiments, but rather through the analysis of a meteorite.

Moissan, a pioneer in research into refractory materials and silicon-based compounds, was examining a meteorite fragment from a crater in Arizona known as Canyon Diablo. During his investigations, he discovered unusual crystalline formations within the meteorite. After careful analysis and extensive study, Moissan identified these formations as silicon carbide. It was the first time that this compound was found in nature and not artificially synthesized. Moissan attributed the presence of silicon carbide in the meteorite to extreme conditions and combination of silicon and carbon in space. This discovery was an important contribution to our understanding of the chemistry and materials in the universe and he provided further confirmation of the abundance of complex and unusual compounds that can form in the cosmic context. Since then, synthetic silicon carbide has been produced and used in numerous industrial applications due to its outstanding properties, such as high hardness and strength. However, Moissan's discovery in the Canyon Diablo meteorite remains a significant moment in the history of chemistry and space exploration, revealing a new perspective on the presence of complex chemical compounds beyond our planet.

Silicon carbide (SiC) crystallizes in several forms, each with their own array of electrical, optical, thermal, and mechanical characteristics. The physical characteristics of SiC are crucial fields of study as well as vital criteria for successful device modeling. This chapter summarizes SiC's physical and electric features.

2.1 Crystal Structure

Due to the fact that SiC is a compound semiconductor, only a rigorous stoichiometry of 50% silicon (Si) and 50% carbon (C) is permitted. In their ground states, the neutral atoms Si and C have the following electronic structures:

$$Si, 14e^- : \ 1s^2 2s^2 2p^6 3s^2 3p^2$$

$$C, 6e^- : \ 1s^2 2s^2 2p^2$$

Si and C atoms are both tetravalent, with four valence electrons in their outer shells. In order to generate a SiC crystal, Si and C atoms are tetrahedrally connected with covalent bonds by sharing electron pairs in sp^3 hybrid orbitals. Each Si atom is surrounded by four C atoms, and vice versa. Because the Si-C bond energy is quite high (4.6 eV), SiC has several exceptional characteristics, which are discussed right after.

SiC is a good example of polytypism in crystallography [1-5]. Polytypism is the phenomenon in which a material can have distinct crystal structures that differ in one dimension (that is, stacking sequence) but not in chemical composition. Different crystal shapes, known as polytypes, originate from variations in the occupied sites along the c-axis in a hexagonal close-packed system. Take a look at the occupied locations in the hexagonal close-packed system depicted schematically in Figure 2.1.

Let's take A, B, and C as the three expected positions. Two layers cannot occupy the same site in consecutively; the following layer on top of a "A" layer must occupy either "B" or "C" sites (and, similarly, "A" or "C" is permitted above "B"). Though in theory there are almost unlimited possibilities of the stacking sequence when stacking a number of layers, for most materials, only one stacking structure (typically either the zincblende or wurtzite structure) is generally stable. However, SiC crystallizes in a surprising number of polytypes (around 200).

Polytypes are denoted in Ramsdell's notation by the number of Si-C bilayers in the unit cell and the crystal system (C for cubic, H for hexagonal, and R for rhombohedral). Figure 2.2 depicts the architectures of three prominent SiC polytypes: 3C-SiC, 4H-SiC, and 6H-SiC, with open and closed circles denoting Si and C atoms, respectively. A, B, and C are the possible occupied spots in the previously stated hexagonal close-packed configuration. Because of these site names, 3C-SiC may be characterized by the repeating sequence ABCABC, or simply ABC.

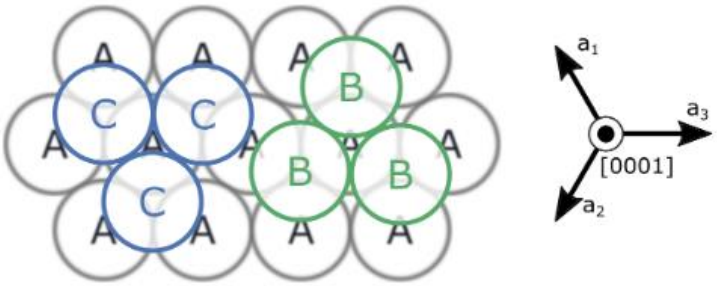


Figure 2.1 Sites of occupation (A, B, and C) in the hexagonal close-packed arrangement [182]

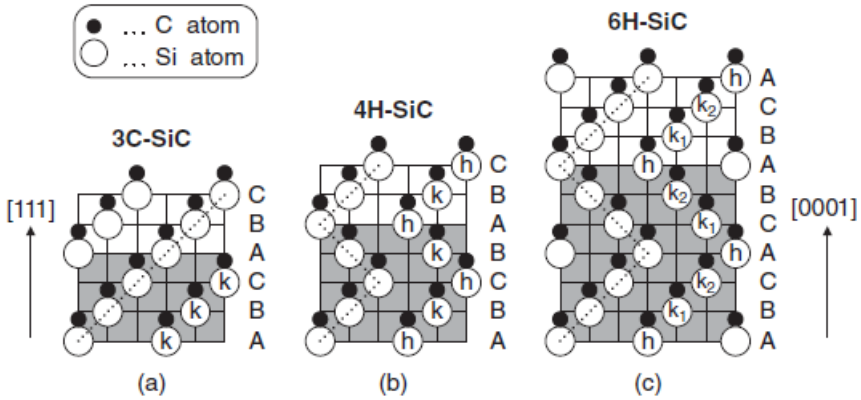


Fig 2.2 Structures of common SiC polytypes (a) 3C-SiC, (b) 4H-SiC, and (c) 6H-SiC are shown schematically. The open and closed circles represent respectively Si and C atoms [170].

SiC crystalline structure is wurtzite-like, which is also seen in GaN and ZnS. However, it is still unclear why there are so many SiC polytypes. In general, crystals with strong covalent bonding form in the zincblende structure, whereas crystals with significant ionicity crystallize in the wurtzite structure.

Due to several ways to arrange Si-C bilayers, SiC has multiple lattice locations that differ in their near neighbor structures. Lattice sites with hexagonal-structured surroundings are referred to as “hexagonal sites,” while those with cubic-structured surroundings are referred to as “cubic sites.” The hexagonal and cubic sites are denoted by “h” and “k,” respectively, in Figure 2.2. 4H-SiC has one hexagonal and one cubic site, while 6H-SiC has one hexagonal and two inequivalent cubic sites and 3C-SiC solely has cubic sites.

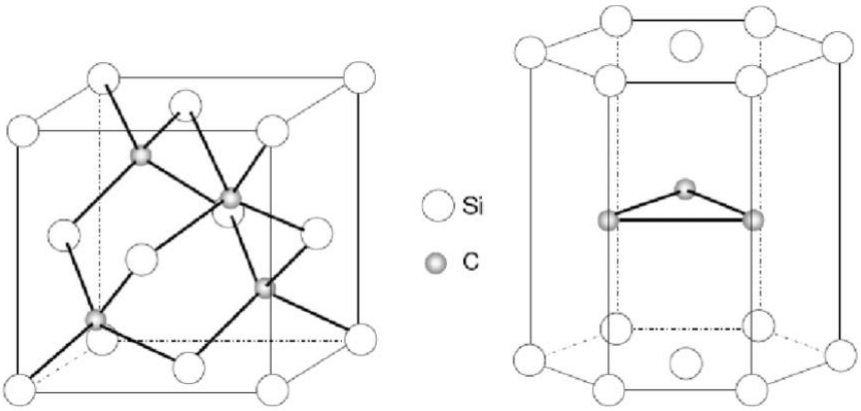


Fig. 2.3 Primitive cells and fundamental translation vectors of (a) cubic (3C) SiC and (b) hexagonal SiC [171].

The placement of the second-nearest neighbors differs between hexagonal and cubic sites, resulting in distinct crystal fields. The energy levels of dopants, impurities, and point defects (such as vacancies), for example, vary depending on the lattice site (hexagonal/cubic). This is known as the "site effect" [6-8].

Polytype	*a* (Å)	*c* (Å)
3C	4.3596	–
4H	3.0798	10.0820
6H	3.0805	15.1151

Table 2.1 Lattice constants of major SiC polytypes at room temperature

The lattice constants of main SiC polytypes at room temperature are shown in Table 2.1 [9]. Though the lattice constants for different SiC polytypes appear highly varied (due to their distinct crystal structures), all SiC polytypes have about the same Si-C bond length (1.89 Å). Thus, the height of the Si-C bilayer along the c-axis (unit height) is 2.52 Å, whereas 3C-SiC and 2H-SiC are somewhat lower (2.50 Å). As with other semiconductor materials, the lattice constants fluctuate with temperature and doping density.

Temperature has a considerable influence on the stability and nucleation likelihood of SiC polytypes [10]. For example, at temperatures exceeding 1900-2000 °C, 3C-SiC degrades and transforms into hexagonal SiC polytypes such as 6H-SiC [11]. Because 3C-SiC is unstable, it is difficult to develop big 3C-SiC ingots at a suitable pace. At high temperatures, 2H-SiC is equally unstable, and massive 2H-SiC crystals have not been formed. Thus, 4H-SiC and 6H-SiC polytypes are quite popular and have received a lot of attention [12-18]. Another common polytype is 3C-SiC, which may be produced

heteroepitaxially on Si substrates [17-19]. In addition to these three primary polytypes, 15R-SiC is infrequently formed and has been examined [18, 20].

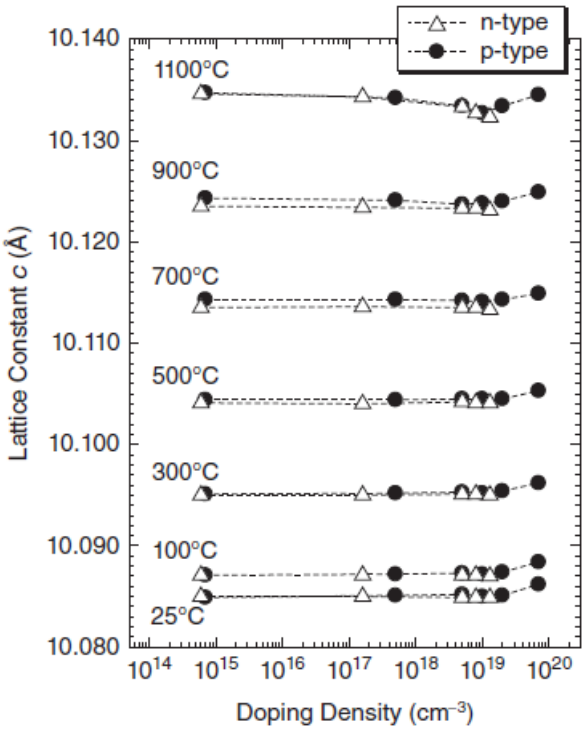


Fig. 2.4 The c-axis lattice constant of 4H-SiC as a function of doping density (nitrogen or aluminum) from ambient temperature to 1100 C [32].

In general, extremely high ($> 10^{19} cm^3$) nitrogen doping induces lattice contraction, while very high aluminum doping promotes lattice expansion. This tendency becomes more apparent at temperatures exceeding 1000 degrees Celsius. As a result, mismatch-induced stress should be expected at the n-/n+, p-/p+, p-/+n, n+/p-, and p+/n+ interfaces, which can result in the formation of extended defects such as basal plane dislocations.

Because all SiC polytypes are composed of comparable Si-C bonds, mechanical characteristics like as hardness are relatively similar [22]. Distinct periodic potentials in distinct SiC polytypes, on the other hand, result in significantly diverse electronic band structures and, as a result, different optical and electrical properties. This means that it is critical for device applications to generate just the required SiC polytype hence; polytype control is an important feature of SiC crystal formation.

Crystal planes and orientations in SiC polytypes are typically stated using four Miller-Bravais indices [23], except for 3C-SiC. When the following relations are met, a crystal plane ($h_1 h_2 h_3 h_l$) is identical to a plane (h k l) defined by three Miller indices in a monoclinic system:

$$h1 = h,\ h2 = k,\ h3 = -(h + k),\ \text{and h} = l \qquad \text{Eq. 2.1}$$

Due to the fact that SiC is a compound semiconductor, valence electrons are somewhat concentrated around C atoms, which are more electronegative than silicon (C: 2.5, Si: 1.8). In this view, Si atoms are cations, while C atoms are anions. This ionicity gives birth to polarity in SiC, which is of academic and technological relevance.

2.2 Electrical and Optical Properties

2.2.1 Band Structure

The first Brillouin zones of (a) 3C-SiC and (b) a hexagonal SiC polytype are shown in Figure 2.5 [9, 22]. Because of the varying values of the lattice parameter, c, the height of the Brillouin zone varies for cubic to hexagonal polytypes.

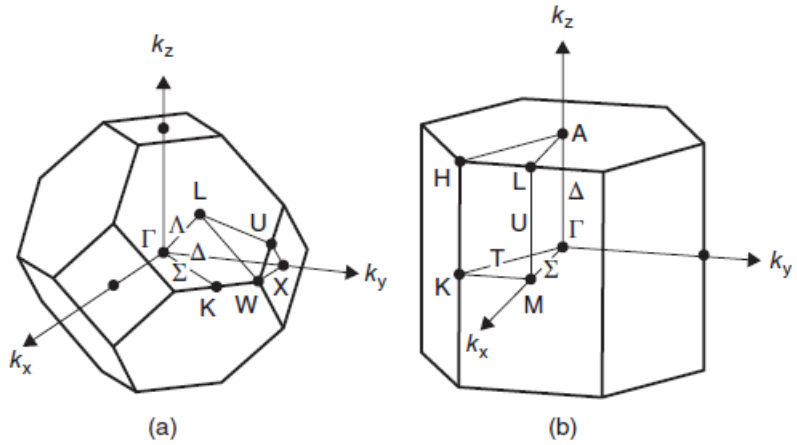


Fig. 2.5 Brillouin zones of (a) 3C-SiC and (b) a hexagonal SiC polytype [32].

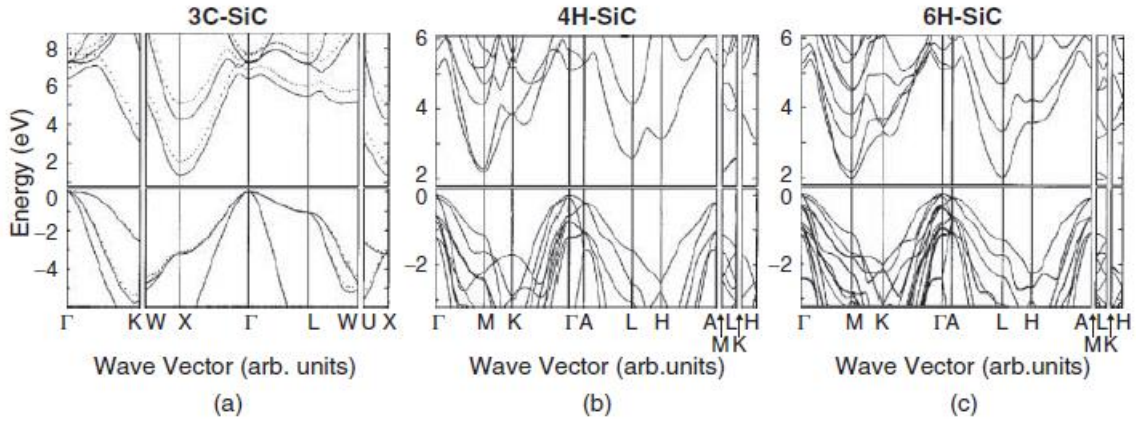


Fig. 2.6 Electronic band structures of (a) 3C-SiC, (b) 4H-SiC, and (c) 6H-SiC [32].

Si-like, all the SiC polytypes have an indirect band structure. The top of the valence band is located at the Γ point in the Brillouin zone,whereas the conduction band minima appear

at the Brillouin zone boundary. The conduction band minima are located at the X point for 3C-SiC, M point for 4H-SiC, and U point (along the M–L line) for 6H-SiC.

Thus, the number of conduction band minima in the first Brillouin zone (*M*c) is 3 for 3C-SiC, 3 for 4H-SiC, and 6 for 6H-SiC. Due to Si-C covalent bonds are common to all SiC polytypes, the valence band structure is similar amongst the different polytypes, except for the splitting. The top of the valence band is doubly degenerate in 3C-SiC, as a result of its cubic symmetry, and the next valence band is shifted 10meV from the top by the spin–orbit interaction [25]. The crystal field, which exists in all hexagonal polytypes, splits the valence band degeneracy. The magnitudes of the spin–orbit splitting and crystal-field splitting for 4H-SiC are 6.8 and 60meV, respectively [26].

The electron effective mass and anisotropy are significantly polytype dependent, but the hole effective mass is very weakly polytype dependent. The former causes a wide range of electron mobility in various polytypes, as well as anisotropic electron transport.

Figure 2.6 shows the exciton gaps of several SiC polytypes at 2K as a function of "hexagonality" [27, 28]. In this context, hexagonality refers to the ratio of hexagonal sites to total Si-C bilayers (hexagonal and cubic sites) in a unit cell (hexagonality is 1 for 2H-SiC, 0 for 3C-SiC, 1/2 for 4H-SiC, and 1/3 for 6H-SiC). It's worth noting that the bandgap of SiC polytypes grows monotonically with hexagon ality. At ambient temperature, the bandgap for 3C-SiC is 2.36 eV, 3.26 eV for 4H-SiC, and 3.02 eV for 6H-SiC.

The bandgap (*E*g) decreases with increasing temperature because of thermal expansion, and its temperature dependence can be semi-empirically expressed as [29]:

$$E_g(T) = E_{g0} - \frac{\alpha T^2}{T + \beta} \qquad \text{Eq. 2.2}$$

In which E_{g0} is the bandgap at 0 K, T the absolute temperature, and α and β are fitting parameters (α = 8.2 × 10−4 eV K−1, β = 1.8 × 10^3 K). To highlight that the bandgap is also depending on the doping density; high impurity doping, above $10^{19} cm^{-3}$, has as consequence bandgap to shrink because of the formation of pronounced tail states near the band edges [30].

2.2.2 Impurity Doping and Carrier Density

SiC is an outstanding wide bandgap semiconductor in that it is reasonably straightforward to manage both n- and p-type doping across a large range. Nitrogen or phosphorus are used for n-type doping, whereas aluminum is used for p-type doping. Boron was formerly used as an acceptor, but it is no longer recommended due to its high ionization energy (350 meV) [31], development of a boron-related deep level (D center) [53, 54], and anomalous diffusion [32, 33].

Gallium and arsenic act as acceptor and donor in SiC, respectively. Their ionization energies, on the other hand, are rather high, and their solubility limits are low. Nitrogen replaces carbon at the C sub-lattice site, whereas phosphorus, aluminum, and boron replace Si at the Si sub-lattice site.

The ionization energy of dopants in SiC is influenced by the lattice site, specifically whether it is hexagonal or cubic (site effect). The ionization energy of the donors is generally low in the case of nitrogen or phosphorus doping, and the ionization ratio of donors at room temperature is quite high, ranging from 50 to almost 100% depending on polytype and doping density. In contrast, aluminum has a high ionization energy, and incomplete ionization (5-30%) of acceptors is found at ambient temperature. It is worth noting that when the doping density increases, the ionization energy lowers due to bandgap reduction and the creation of an impurity band. Efros et al. [40] explain the relationship of dopant ionization energy, E_{dopant}, on dopant density:

$$\Delta E_{dopant} = \Delta E_{dopant,0} - \alpha\left(N_{dopant}\right)^{1/3} \qquad \text{Eq. 2.3}$$

Here $\Delta E_{dopant=0}$ is the ionization energy in lightly-doped materials, N_{dopant} the dopant density, and α a parameter (α = (2–4) × 10^{-8} eV). When the dopant density exceeds $10^{-19} cm^{-3}$, the ionization energy decreases sharply. As a result, near-perfect ionization is observed in heavily aluminum-doped SiC (>5 × 10^{-20} cm^{-3}), in spite of the relatively large ionization energy of aluminum [41].

Because the band structure (bandgap, effective mass) is known, one can calculate the effective densities of states in the conduction band N_C and valence band N_v as well as the intrinsic carrier density n_i as follows [42]:

$$N_C = 2M_C\left(\frac{2\pi m_{de} * kT}{h^2}\right)^{3/2}$$

$$N_V = 2\left(\frac{2\pi m_{dh} * kT}{h^2}\right)^{3/2}$$

$$n_i = \sqrt{N_C N_V} exp\left(-\frac{E_g}{2kT}\right) \quad \text{Eq. 2.4}$$

Here, M_C is the number of conduction band minima, *m*de∗ and *m*dh∗ the effective mass of electrons (holes), and *h* the Planck constant. By using the effective mass of electrons (holes) and the number of conduction band minima, the *N*C and *N*V values for 4H-SiC at room temperature are calculated as 1.8×10^{-19} and $2.1 \times 10^{-19}\ cm^{-3}$, respectively. These values are important as they allow us to estimate whether the material will be degenerate when heavy impurity doping is performed. Figure 2.14 plots the temperature dependence of (a) the effective densities of states in the bands and (b) the intrinsic carrier density for major SiC polytypes, together with that of Si. Here, the temperature dependence of bandgaps is considered.

Here *n*(*p*) is the free electron (hole) density, *N*comp,A (*N*comp,D) the density of compensating acceptor (donor) levels, *N*D (*N*A) the donor (acceptor) density, ⊿*E*D (⊿*E*A) the ionization energy of the donor (acceptor), and *g*D (*g*A) are the degeneracy factors for donors (acceptors), respectively. When multiple donor (or acceptor) levels exist, the sum for corresponding dopants must be considered in the right-hand term of the equation 2.4. This is the case for hexagonal SiC polytypes, because the donor (and acceptor) impurities at inequivalent lattice sites (e.g., *i* = k, h for 4H-SiC) exhibit different energy levels.

The position of the Fermi level *E*F in non-degenerate semiconductors is calculated by [42]:

$$E_F = E_C - kTln\left(\frac{N_C}{n}\right)$$

$$E_F = E_V - kTln\left(\frac{N_V}{p}\right) \quad \text{Eq. 2.5}$$

where *E*C (*E*V) is the energy of the conduction (valence) band edge. Thanks to the wide bandgap, the Fermi level does not approach the midgap (intrinsic level) even at a fairly high temperature of 700–800 K;

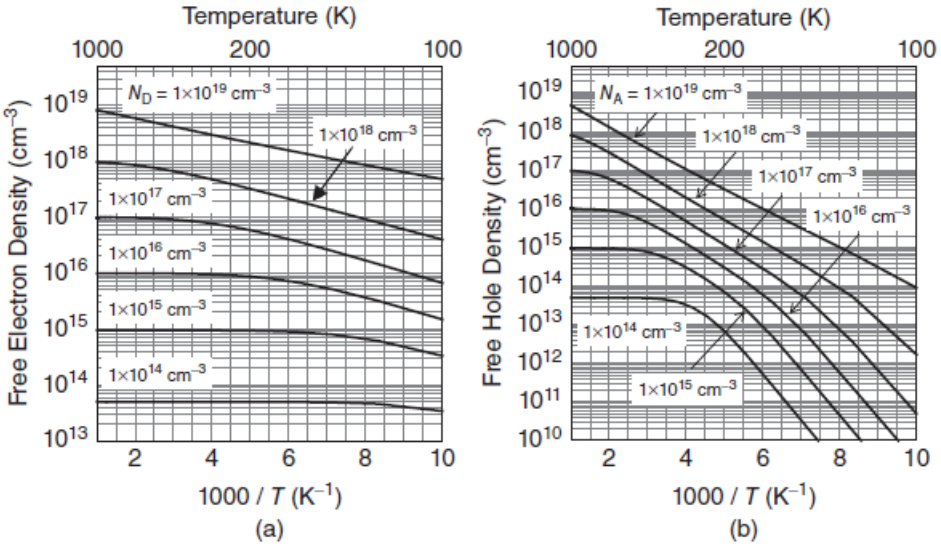


Fig. 2.7 Arrhenius plots of the free carrier density in (a) nitrogen-doped and (b) aluminum-doped 4H-SiC. Here, the temperature dependence of the bandgap and the doping-density dependence of the ionization energies are taken into account [32].

2.2.3 Mobility

Mobility is defined as the modulus of the drift rate of a charge carrier per unit of electric field,it is defined positive both for the electrons and for the holes (even if their speed of drift, under the action of an electric field, is opposite). The electron mobility of 4H-SiC is almost double that of 6H-SiC at a given dopant density, and 4H-SiC exhibits a slightly higher hole mobility than 6H-SiC. The low-field electron and hole mobilities can be expressed by *Caughey–Thomas equations* as follows [41, 43–48]:

$$\mu_e(4H-SiC) = \frac{1020}{1+\left(\frac{N_D+N_A}{1.8\times 10^{17}}\right)^{0.6}}(cm^2V^{-1}s^{-1})$$

$$\mu_e(6H-SiC) = \frac{450}{1+\left(\frac{N_D+N_A}{2.5\times 10^{17}}\right)^{0.6}}(cm^2V^{-1}s) \qquad \text{Eq. 2.6}$$

N_D and N_A are provided in cm^2 units here. The modest discrepancies in doping-dependence characteristics between 4H- and 6H-SiC are due to variances in dopant ionization energies. It should be emphasized that the electron mobility of hexagonal (and rhombohedral) SiC polytypes is very anisotropic [43, 49]. The mobility anisotropy is

relatively small in 4H-SiC, where the electron mobility along the *c*-axis direction is approximately $1200\ cm^2V^{-1}s^{-1}$ at room temperature, which is 20% higher than that perpendicular to the *c*-axis. This is one of the major reasons why 4H-SiC is the most attractive polytype for vertical power devices fabricated on SiC{0001} wafers.

In nondegenerate semiconductors, the diffusion coefficients of carriers (*D*) can be obtained by using the Einstein relation [42]:

$$D = \frac{kT}{q}\mu \qquad \text{Eq. 2.7}$$

Here q is the elementary charge.

when high temperatures are reached, the doping dependence of mobility becomes small, because the influence of impurity scattering decreases.

In moderately-doped p-type SiC, the hole mobility is mainly determined by acoustic phonon scattering at or below room temperature, and by nonpolar optical phonon scattering at high temperature (>400 K). In heavily-doped p-type SiC, the major scattering process is neutral impurity scattering over a wide temperature range, since most Al acceptors remain neutral because of their large ionization energy. Acoustic-phonon scattering (ac), polar-optical-phonon scattering (pop), nonpolar-optical-phonon scattering (npo), intervalley scattering by phonons (iph), ionized-impurity scattering (ii), and neutral-impurity scattering (ni) are all carrier scattering processes.

2.2.4 Drift Velocity

At low electric fields, carrier drift velocity (v_d) is proportional to electric field strength (E), $v_d = \mu E$. When the electric field is strong, the accelerated carriers transfer more energy to the lattice by generating more phonons, resulting in nonlinear drift velocity dependency [50]:

$$v_d = \frac{\mu E}{\left\{1 + \left(\frac{\mu E}{v_s}\right)^{\gamma}\right\}^{1/\gamma}} \qquad \text{Eq. 2.8}$$

where v_s is the sound velocity in a semiconductor and γ the parameter. At sufficiently high electric fields, carriers start to interact with optical phonons, and finally the drift

velocity becomes saturated. The *saturated drift velocity* (υsat) is approximately given by [42, 50]:

$$v_{sat} = \sqrt{\frac{8\hbar\omega}{3\pi m^*}} \qquad \text{Eq. 2.9}$$

where $\hbar\omega$ is the energy of the optical phonon (LO (longitudinal optical) phonon) emitted. Figure 2.8 shows the measured drift velocity of electrons versus applied electric field for n-type (a) 4H-SiC and (b) 6H-SiC [77]. For 4H-SiC, a low-field mobility of 450 $cm^2V^{-1}s^{-1}$ was determined from the slope at low electric fields (< 104 $V^{-1}s^{-1}$ V) at room temperature. The saturated drift velocity is determined as 2.2 × 10^7 $cm\ \ s^{-1}$ at room temperature. This value is also in good agreement with that estimated from Equation 2.9. As indicated in Figure 2.8, the saturated drift velocity decreases with increasing temperature. Note that a so-called transferred-electron effect (Gunn effect) is not observed in SiC because of its indirect band structure.

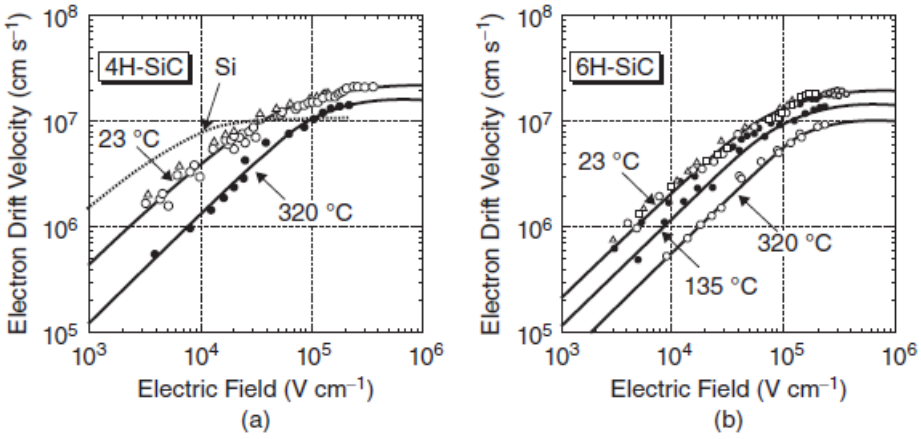


Fig. 2.8 Drift velocity of electrons versus applied electric field for n-type (a) 4H-SiC and (b) 6H-SiC [32].

2.2.5 Breakdown Electric Field Strength

Due to the existence of minority carriers thermally generated inside the depletion area, the current in a p-n junction (or a Schottky diode) tends to grow with increasing applied electric field in reverse polarization. The p-n junction finally fails if the amplitude of the electric field is sufficiently large. Failure mechanisms can be classified into:

2.2.6 Avalanche effect (breackdown)

Avalanche is a phenomenon of electric current amplification caused by extremely strong electric fields. The charge carriers are driven from the field at tremendous speeds, and as they travel through the material, they collide with the atoms. If the field is strong enough, the energy of the particles is high enough to ionize the lattice atoms (impact ionization). At this point, both the beginning carriers and the carriers arising from atom ionization will participate in the conduction process and be accelerated, potentially resulting in an avalanche if the field is sufficiently strong. If the field is not powerful enough, the carriers' speeds are insufficient to maintain the avalanche breakdown, and the carriers are reabsorbed by the atoms. When dealing with modestly doped junctions (small depletion zones), this effect is prominent.

Avalanche breakdown is well described by using the *impact ionization coefficients* of electrons and holes [42, 51]. Breakdown can be defined as when the multiplication factor of the current approaches infinity, which has been shown to be equivalent to the following relationship [42, 51]:

$$\int_0^W \alpha_h exp\left\{-\int_o^x (\alpha_h - \alpha_e)dx'\right\}dx = 1 \qquad \text{Eq. 2.10}$$

2.2.7 Zener effect (tunneling)

It is an effect that occurs in p-n junctions, heavily doped, in reverse polarization. The applied electric field favors the tunnel effect of the semiconductor charge carriers: the electrons pass from a valence band to a conduction band. This generates a sudden increase in reverse current.

Although both effects concern the minority charge carriers, the two effects differ for the physical reasons that arise from them. The two effects can also occur simultaneously. The Zener breakdown is temperature-dependent, so it is particularly inversely proportional to T: as the temperature increases, the gap decreases, therefore the Tunneling barrier; for the same reasons we have the opposite reasoning for the avalanche effect [52].

The breakdown field can be expressed in terms of voltage applied as follows [53]:

$$V_B = \frac{E_{cr}^2}{eqN_d}\varepsilon_r\varepsilon_0 \qquad \text{Eq. 2.11}$$

where N_d is the n-type doping, q is the electron charge, $\varepsilon = \varepsilon_r \varepsilon_0$ is the dielectric constant of the vacuum multiplied for the relative constant of the semiconductor used to realize the diode, E_{cr} is the critical field, that is the maximum value of the electric field applicable to a junction of a given material.

2.2.8 Thermal conductivity

Figure 2.9 shows the temperature dependence of thermal conductivity for SiC and Si, with itssignificant contribution from phonons, has a much higher thermal conductivity than Si. It hasbeen reported that the thermal conductivity is not sensitive to the SiC polytype but dependson the doping density and the crystal direction.

Silicon carbide has a high thermal conductivity. This is an advantage with regard to heatdissipation, as the thermal resistance is defined as:

$$R_{th-jc} = \frac{d}{\lambda A} \qquad \text{Eq. 2.12}$$

where λ is the thermal conductivity, d is the thickness of the device and A is the section. Therefore, the thermal resistance for the same thickness, is much lower than that of Silicon, and this allows a greater transfer of heat from the junction to the case, therefore towards the heat sinks, and finally towards the external environment.

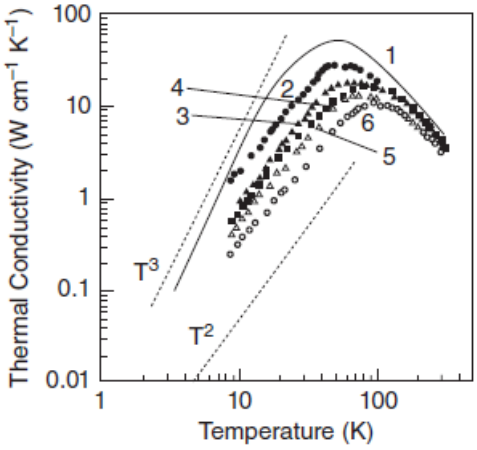


Fig. 2.9 Temperature dependence of thermal conductivity for SiC and Si [32].

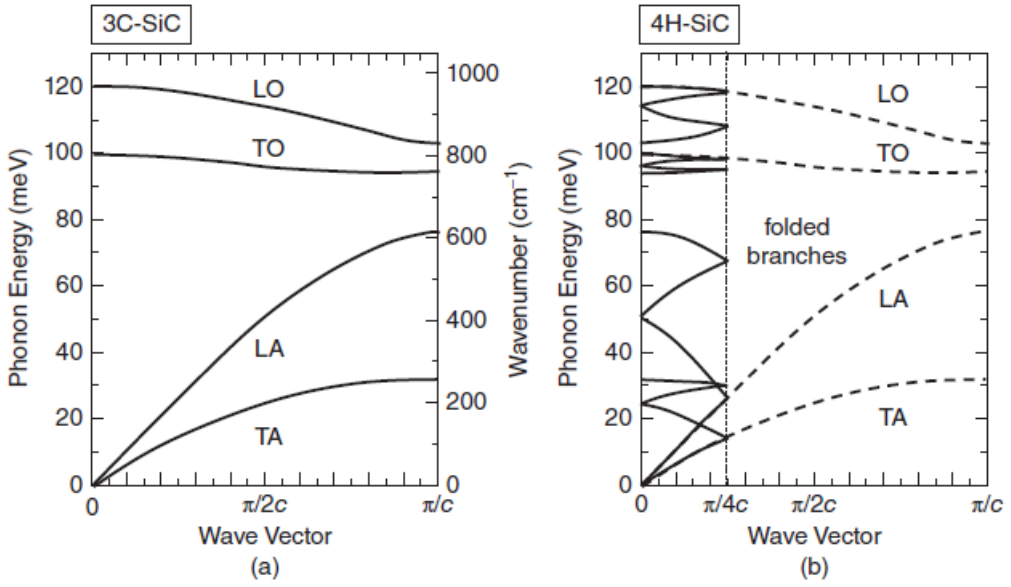


Fig. 2.10 Phonon dispersion relationships for (a) 3C-SiC and (b) 4H-SiC [32].

2.2.9 Phonons

Figure 2.10 shows the phonon dispersion relationships for (a) 3C-SiC and (b) 4H-SiC [54, 55]. The basic branches consist of TA (transverse acoustic), LA (longitudinal acoustic), TO (transverse optical), and LO phonons, as in other semiconductors. Due to the large energy of Si-C bonds, the phonon frequencies in SiC are high. The unit cell length of the *n*Hpolytype (*n* = 2, 4, 6 …)along the *c*-axis is *n* times larger than the unit length (Si-C bilayer). Thus, the Brillouin zone in the direction of Γ–L is reduced to 1⁄*n* of the

basic Brillouin zone [23]. The dispersion curves of the phonons propagating along the <0001> direction in such polytypes can be approximated by folding the basic dispersion curve.

This zone folding provides new phonon modes at the Γ point, which are called "*folded modes*." The number of atoms in the unit cell is 2 for 3C-SiC, 8 for 4H-SiC, and 12 for 6H-SiC. Therefore, the number of phonon branches is 6 for 3C-SiC, 24 for 4H-SiC, and 36 for 6H-SiC, neglecting the degeneracy.

The major phonon energies (or wavenumber) can be directly observed by Raman scattering spectroscopy. Different phonon frequencies in different SiC polytypes enable identification of individual polytypes by Raman scattering measurements. It is known that the observed frequency of LO phonons increases with increasing carrier density because of a carrier–LO phonon coupling effect [56]. Phonon energies are also important in luminescence measurements.

In particular, photoluminescence (PL) at low temperature is a powerful tool to characterize the purity and quality of SiC crystals. Because SiC has an indirect band structure, phonons are intensively involved in carrier recombination processes. As a result, strong multiple phonon replicas of a zero-phonon emission line are often observed in PL spectra of SiC. For example, the

energies of major phonons which create phonon replicas in PL from 4H-SiC{0001} are 36 (TA), 46, 51, 77 (LA), 95, 96 (TO), 104, and 107 meV (LO).

2.2.10 Hardness and Mechanical Properties

The mechanical properties of SiC are also unique; SiC is one of the hardest known materials.

The hardness and Young's modulus (380–700 GPa [57]) of SiC are much higher than those of Si, while the Poisson's ratio (0.21) of SiC is very similar to that of other semiconductors. SiC retains its high hardness and elasticity, even at very high temperatures. The yield (fracture) strength of SiC is as high as 21 GPa at room temperature and is estimated to be 0.3 GPa at 1000 ∘C, while the yield strength of Si falls to 0.05 GPa at 500 ∘C [58].

Chapter 3

SiC-based devices

During the PhD and the job in situ in STMicroelectronics, I had to face to different SiC-based devices, mainly diodes and MOSFETs, studying electric and thermal issues both in substrate/epitaxy process flow level and after the finished product in order to evaluate thermal reliability, a crucial step in power electronics.

3.1 SiC diodes.

The main SiC diodes are three:

- Schottky diodes,
- Junction barrier Schottky (JBS) diodes,
- PIN diodes.

Figure 3.1 [59] depicts the fundamental structures.

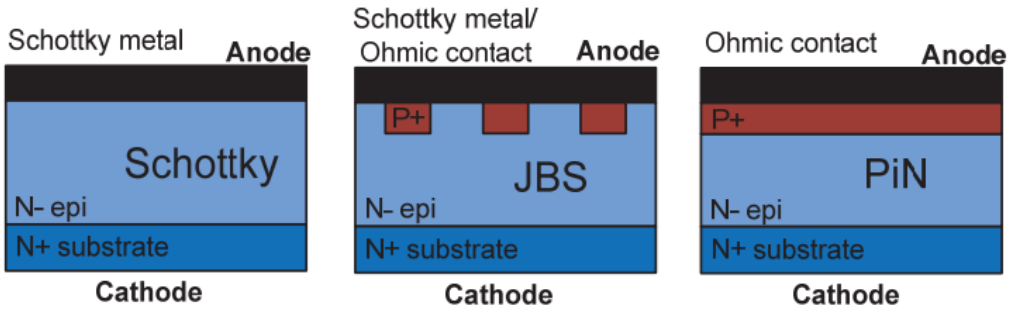


Fig. 3.1 Three basic SiC diode structures.

The SiC Schottky barrier diode (SBD) is an appropriate substitute for the Si PIN diode due to its combination of a Schottky diode structure and SiC material. The majority carrier electron current traveling from the anode to the cathode conducts current in the forward condition. The voltage drop is defined by the N-layer resistance plus the Schottky barrier height, which is usually between 0.7 and 0.9 V. Because of the majority carrier conduction method, the device quickly switches from ON to OFF, and there is almost little reverse recovery current. The only current that must flow in the opposite direction needs to charge the junction capacitance. Its most notable benefit over the Si PIN diode is its exceptionally quick reverse recovery feature. The low reverse recovery current not only enables prospective efficiency increases, but it also greatly decreases converter

oscillation and the associated electromagnetic interference (EMI) issue during diode turn-off. Because the Schottky barrier lowering effect causes the leakage current in the SBD to grow rapidly at higher temperatures, the blocking voltage of commercially available SiC SBDs is restricted to 600 V. The JBS structure is used by the majority of marketed SiC diodes. Multiple P+ regions are incorporated to surround the Schottky region in the SiC JBS diode. They direct the highest electrical field away from the Schottky barrier and toward the P+ region's bottom. As a result, even at the rated junction temperature, which is often less than 175qC, the off-state leakage current is minimized. The JBS's speed is not impacted since device conduction is still via majority carrier electrons.

As a result, the JBS diode performs admirably throughout a large voltage range, e.g., 600 V-3.3 kV. For high-frequency applications, a 15 kV JBS diode has also been built and tested [60]. However, the dependable voltage blocking capacity needs yet be demonstrated, since the blocking voltage in the examined samples was found to be approximately 13kV. The merged PIN Schottky (MPS) diode is another working mode of this device; the internal PIN junction diode is switched on only with a strong forward bias, boosting the current handling capabilities. In the power semiconductor business, progress has been made toward numerous generations of the SiC JBS/MPS diode [61]. The trench structure SiC Schottky diode is also shown to minimize leakage current [62]. Recent research also shown that contemporary SiC Schottky diodes are particularly resistant to leakage current thermal runaway, since the temperature rise required to double the leakage current is more than in the Si PIN diode [63].

Through conductivity modulation, the bipolar SiC PIN diode may efficiently minimize drift area resistance. This makes it appealing in ultra-high-voltage levels like 10-20 kV [64]. The I-V curves of a 10 kV SiC JBS diode and a 10 kV PIN diode with the same chip size are compared in Fig. 3.2. Despite having a larger knee voltage, the differential resistance of the SiC PIN diode is significantly lower than that of the JBS diode due to conductivity modulation. Another benefit of the SiC PIN diode over the JBS or SBD is its substantially lower leakage current, making it a good option for higher temperature operation. However, when the blocking voltages are less than 3.3 kV, the SiC PIN is rendered useless due to the 3 V PN junction knee voltage, which is specified by the SiC material. In these voltage ranges, SiC JBS diodes are recommended. Because of the minority carrier held in the device, the SiC PIN diode has a significant reverse recovery current, as seen in Fig. 7 (b), resulting in considerable reverse recovery losses in converter applications.

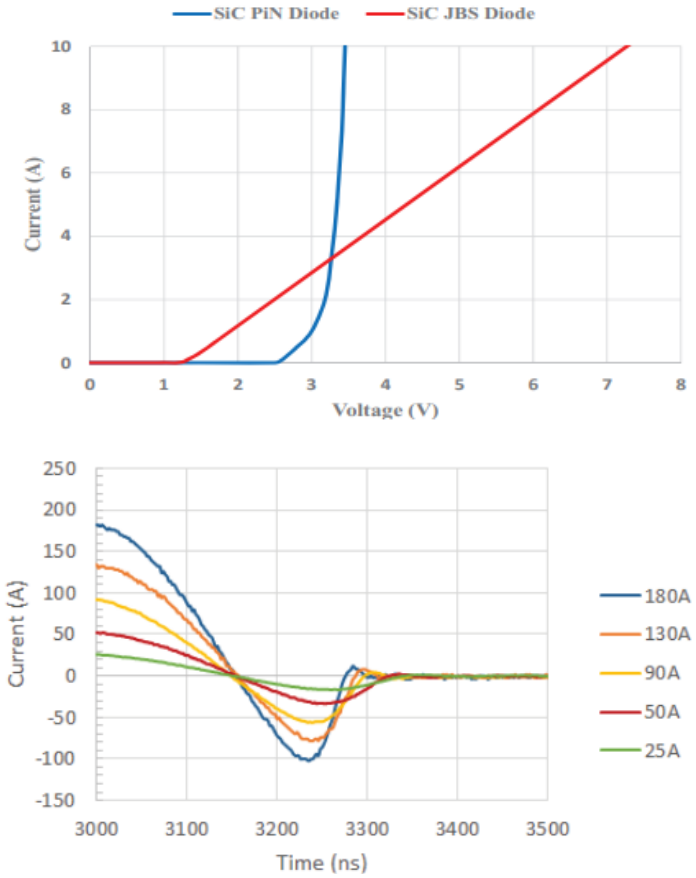


Fig. 3.2 (a) The 10 kV SiC JBS diode and PIN diode I-V curves at room temperature with the same chip size. (b) Reverse recovery current tested at VR=7kV for a 15 kV SiC PIN diode (T=25 °C) [172].

One of the main technological hurdles for high-voltage SiC devices is the lowering of the surface electrical field near the device's edge. Numerous planar edge termination strategies in SiC diodes have been proven, the majority of which are based on similar ideas utilized in Si power devices. The most basic include junction termination extension (JTE) [65–67], floating field ring (FFR) [68–70], field plates [71–72], mesa structure [73], bevel structure [74–75], and hybrid solution approaches [75–78]. For high-voltage SiC devices, the JTE and FFR are recognized as the most effective approaches [79]. The JTE is designed to extend the connection in the lateral direction while reducing electric field congestion at the extension's border. As a development, Fig. 3.3(a) depicts a multiple-zone JTE idea in which the dosage is gradually reduced near the JTE margin [66]. This changes the form of the electrical field distribution from triangular to rectangular, increasing the breakdown voltage. The process complexity of a multiple-zone JTE is a difficulty owing to the many implant procedures required.

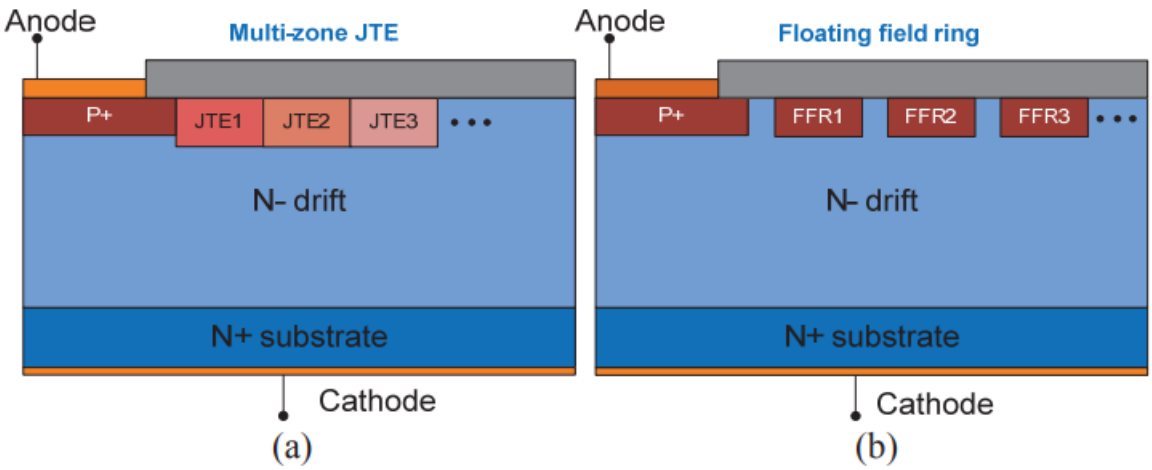


Fig. 3.3 Edge termination methods for high-voltage SiC devices. (a) Multi-zone JTE termination; (b) FFR termination.

3.1.1 MOS Diodes

The MOS diode is constituted by a metal-semiconductor junction. The metal layer acts as the diode's anode, while the semiconductor operates as the cathode. The mix of metal and semiconductor defines the diode's threshold voltage, or the voltage that must be supplied to the device before it begins to conduct. The diameter of the depletion area reduces as the concentration of dopants in the semiconductor rises. Charges can be tunneled through the emptying region below a specific width. The ideal MOS is distinguished by the following electric states.

3.1.2 Flat energy bands at $\Delta V = 0$

In the absence of polarization, the energy difference between the extraction work of the metal $q\varphi m$ and the semiconductor extraction work $q\varphi s$ is zero, i.e. for a p-type semiconductorthe difference of the extraction works is null:

$$q\varphi_{m,s} = (q\varphi_m - q\varphi_s) = \underset{q\varphi_m}{} - (q\chi + \frac{E_g}{2} + q\varphi_B) = 0 \qquad \text{Eq.3.1}$$

where $q\chi$ is the electron affinity of the semiconductor and $q\varphi B$ is the energy differencebetween the Fermi level E_F and the intrinsic Fermi level E_i.

3.1.3 Oxide infinite resistivity

When a continuous polarization is applied, there is no transport of charges through the oxide.

3.1.4 Carrier charges

For each polarization, the carrier charges are those in the semiconductor and those, with opposite sign, at the metal-oxide interface.
When an external polarization is applied to the diode, it can occur two different phenomenadepending on the applied positive or negative voltage.

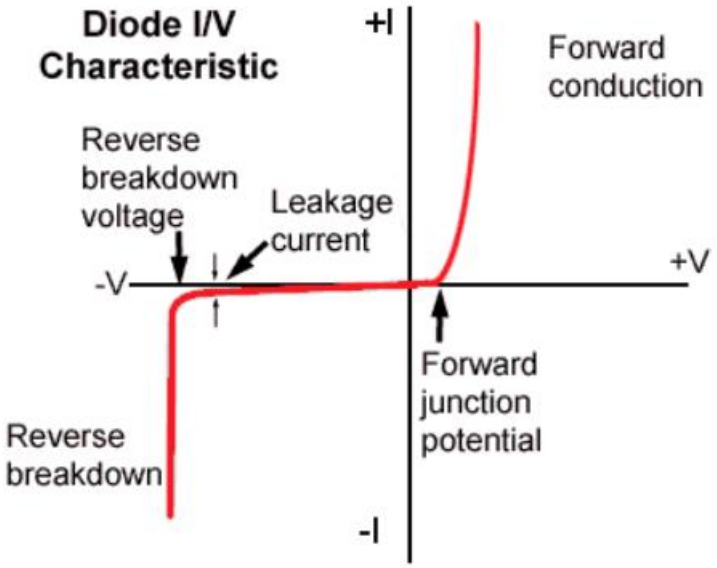


Fig. 3.4 Diode I/V characteristic [173]

3.1.5 Inverse polarization (V<0)

By applying a negative voltage to the metal electrode, the energy bands will bend upward, next to the semiconductor surface: in the device there is no current passing, regardless of the applied voltage. This occur because the electric field generated by the battery has the same direction of the built-in field (voltage that is created at the edges of thedepletion region) resulting in an enlargement of the depletion region [80]. The density of carriers in the semiconductor depends exponentially on the E_i-E_F energy difference, ie:

$$p_p = n_i e^{(E_i - E_F)/kT} \qquad \text{Eq. 3.2}$$

The upward curve of the energy bands at the semiconductor's surface increases the energy differential Ei-EF, causing a rise in concentration, i.e. an accumulation of holes near the oxide-semiconductor interface. This is referred to as accumulation, and the related charge distribution is seen on the right side of Figure 3.5.

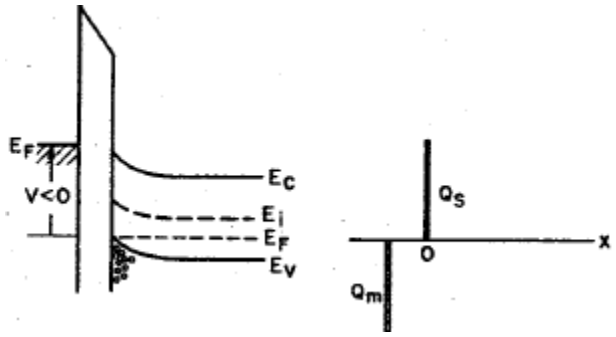


Fig. 3.5 Energy band and Charges distribution for V<0

3.1.6 Direct polarization (V>0)

When a little positive voltage is applied to the device, the energy bands tend to bend downwards, and the majority carriers (holes) are emptied, resulting in depletion of the depletion area, as seen in figure 3.6:

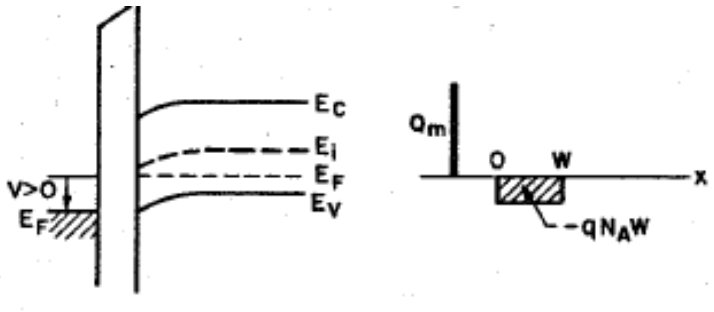


Fig. 3.6 Energy band and Charges distribution for V>0

The space charge per unit area Q_{SC} in the semiconductor is formed by the charge in the depleted zone [26]:

$$Q_{sc} = -qN_A W \qquad \text{Eq. 3.3}$$

In which *W* is the thickness of the depleted zone.

3.1.7 Direct polarization (V>>0)

When a greater positive voltage is supplied, the energy bands bend even further, as seen in Figure 3.6, and the intrinsic energy level Ei crosses the energy Fermi level EF.

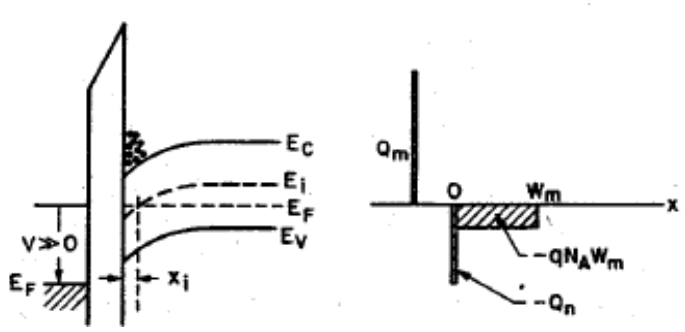


Fig. 3.6 Energy band and Charges distribution for V>>0

The electron concentration depends exponentially on the energy difference *EF-Ei* and is given by:

$$n_p = n_i e^{(EF-Ei)/kT} \qquad \text{Eq. 3.4}$$

In the condition depicted in the figure above, (EF-Ei)>0; hence, the concentration of electrons at the Fermi surface is larger than the concentration of holes, resulting in a further drop in the number of holes. A population inversion has occurred when the number of electrons (minority carriers) exceeds the number of holes (majority carriers). If the bands are increasingly inflected, the conduction band limit approaches the Fermi level, at which point the electron concentration at the surface rapidly increases [80]. Furthermore, the charge Qn of the electrons of the thin n-type inversion layer with thickness xi

constitutes the majority of the extra negative charges in the semiconductor. Typical xi values range between 10 and 100, which is less than the thickness of the surface emptying layer. The thickness of the surface emptying layer reaches a maximum once an inversion layer has developed. This is because, once the bands have been bent downwards sufficiently to produce a strong inversion, any further downward curvature, even if very small (such as causing a very small increase in the thickness of the inversion layer), causes a large increase in the Qn charge of the inversion layer. As a result, in the presence of substantial inversion, the charge per unit area is given by:

$$Q_s = Q_n + Q_{sc} \qquad \text{Eq. 3.5}$$

where:

$$Q_{sc} = -qN_A W_m \qquad \text{Eq. 3.6}$$

and W_m is the maximum thickness of the surface emptying region.

Figure 3.7 shows, in greater detail, the diagram of the energy bands at the surface of the semiconductor. The electrostatic potential φ is zero within the semiconductor. At the surfaceof the semiconductor, it is $\varphi=\varphi_S$ where φ_S is the surface potential.

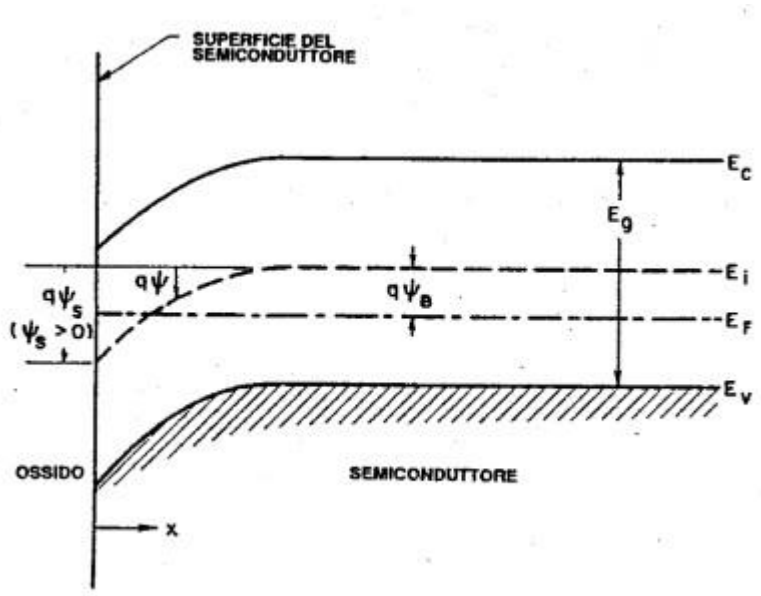


Fig. 3.7 Energy band for V>>0.

The concentrations of electrons and hole can be expressed as:

$$n_p = n_i e^{q(\varphi - \varphi_B)/kT}$$

$$p_p = p_i e^{q(\varphi_B - \varphi)/kT} \qquad \text{Eq. 3.7}$$

where it is assumed that φ_S is positive when the band diagram has a downward curvature. Consequently, on the surface the concentrations are:

$$n_S = n_i e^{q(\varphi_S - \varphi_B)/kT}$$

$$p_S = n_i e^{q(\varphi_B - \varphi_S)/kT} \qquad \text{Eq. 3.8}$$

Based on these equations, we can distinguish different situations regarding the surface potential:

- $\varphi_S < 0 \rightarrow$ holes accumulation (bands curve upwards)
- $\varphi_S = 0 \rightarrow$ flat band condition
- $\varphi_B > \varphi_S > 0 \rightarrow$ holes depletion (bands curve downwards)
- $\varphi_S = \varphi_B \rightarrow$ center of the forbidden band with $n_S = n_P = n_i$ (intrinsic concentration)
- $\varphi_S > \varphi \rightarrow$ population inversion (bands curve downwards)

It is possible to establish a criterion to fix the point of strong inversion. For this purpose, we define the concentration of the electrons at the surface equals the concentration of the impurities in the substrate:

$$n_s = N_A \qquad \text{Eq. 3.9}$$

Therefore, a potential equal to φ_B is needed to curve down the energy bands up to the intrinsic condition ($E_i = E_F$), then a further φ_B is necessary to obtain the strong inversion condition.

3.2 MOSFETs

As a switching device for power applications, the Bipolar Power Transistor (BPT) has a few drawbacks. This has led to the creation of the power Metal Oxide Semiconductor Field Effect Transistor (MOSFET). Power MOSFETs are utilized in a variety of applications including Switched Mode Power Supplies (SMPS), computer peripherals, automotive, and motor control. Continuous research has strengthened its abilities to replace the BJT. Si MOSFETs with a trench gate structure dominate the market in applications below 600 V, whereas Si super junction MOSFETs and Si insulated gate bipolar transistors (IGBTs) with field stop and injection enhancement concepts dominate the market from 600 V to 6.5 kV. Regardless of these advances, Si power devices are reaching their performance limits. The IGBT's maximum blocking voltage is less than 6.5 kV, and the realistic working temperature is less than 175 C [3]. IGBT switching rates are also quite slow due to the bipolar current conduction process, confining them to lower switching-frequency applications. Future progress in Si power device technologies will continue, although at a slower pace.

3.2.1 History

The principle underlying the Field Effect Transistor (FET) has been known from 1920-1930, 20 years before the invention of the bipolar junction transistor. In that period, J.E. Lilienfeld proposed a transistor type with two metal contacts on each side and an aluminum plate on top of the semiconductor. The electric field created by the voltage applied to the metallic plate at the semiconductor surface allows control of the current flow between the metal contacts. This was the FET's initial concept. Development was extremely sluggish due to a shortage of adequate semiconductor materials and underdeveloped technology. In 1952, William Shockely invented Junction Field Effect Transistors (JFETs). In 1953, Dacey and Ross improved on it.

In JFETs, the metallic field of Lilienfeld is replaced by a P-N junction, the metal contacts are referred to as source and drain, and the field effect electrode is referred to as a gate. Until new products were launched in the 1970s, research in small-signal MOSFETs proceeded without any notable breakthroughs in power MOSFET design.

3.3.2 FETS

3.3.2.1 Junction Field Effect Transistors (JFETs)

JFETs come in a couple of different forms: N-channel types and P-channel types. They both employ the voltage applied to the gate to control the drain-to-source current. If the bias is not applied at the gate, as shown in Figure 3.8 (a), the current flows from the drain to the source. As illustrated in Figure 3.8 (b), when the bias is applied at the gate, the depletion region starts to expand and lowers the current. The reverse bias between the gate and the drain, VDG (=VGS+VDS), is higher than the bias between the gate and the source, VGS, which accounts for the drain's wider depletion zone than the source's depletion region.

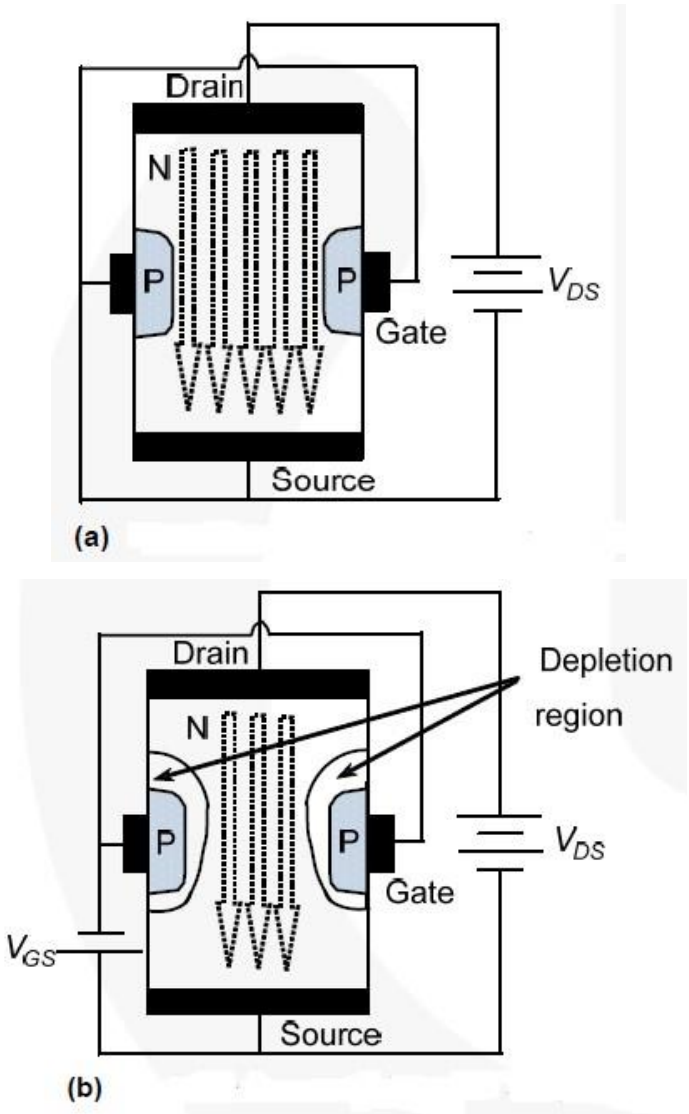


Fig. 3.8 Structure of a JFET and its Operation in which in (a) VGS (Gate-Source Voltage) is not Supplied and (b) VGS (Gate-Source Voltage) is supplied [174]

3.3.2.2 Metal Oxide Semiconductor Field Effect Transistors (MOSFETs)

The two kind of MOSFETs are depletion type and enhancement type, and each of them has a N/P–channel type. Referring to Figure 3.9, the depletion type is typically active and functions as a JFET. The drain-to-source current rises as the gate voltage rises since the enhancement type is typically off. When the gate is not given any voltage, no current flows (see Figure 3).

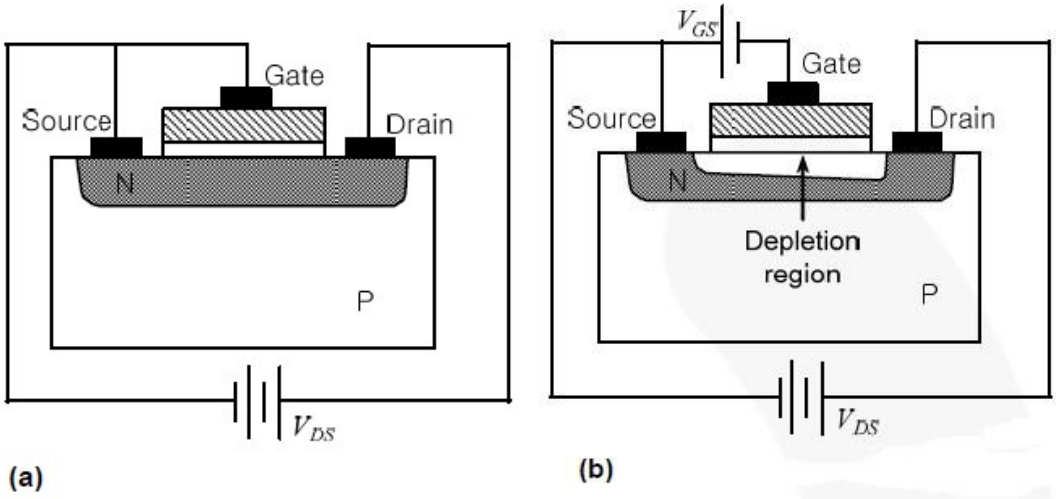


Fig 3.9 Structure of a depletion Type MOSFET and its operation in which (a) VGS Gate-Source Voltage is not supplied and in (b) VGS (Gate-Source Voltage) is supplied [174]

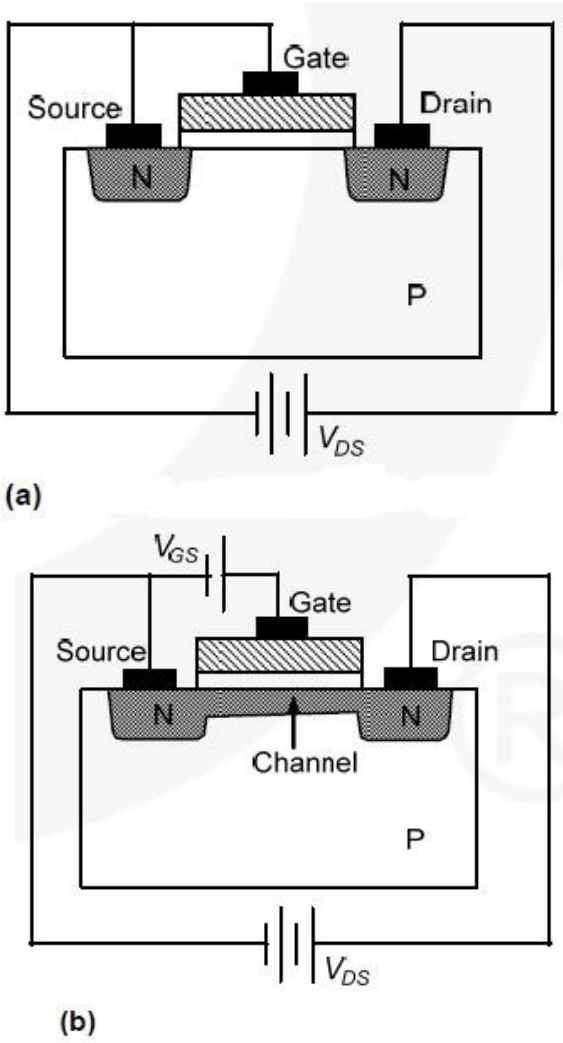


Fig. 3.10 Structure of a enhancement Type MOSFET and its operation in which in (a) VGS (Gate-Source Voltage) is not supplied and in (b) VGS (Gate-Source Voltage) is supplied [174]

3.3 Structure of a MOSFET

3.3.1 Lateral Channel Design

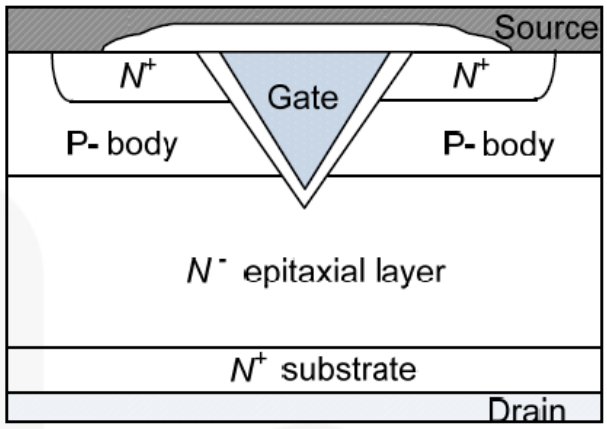
The drain, gate, and source terminals are placed on the surface of the wafer. This is suitable for integration but not for achieving high power ratings since the distance between source and drain must be substantial in order to get superior voltage blocking capacity. The current from the drain to the source is proportional to the length.

3.3.2 Vertical Channel Design

In vertical design, the recently most use topology, the drain and source are placed on the opposite sides of the wafer. This is properly fitting for a power device application since greater section can be used as a source. By increasing the length between the source and

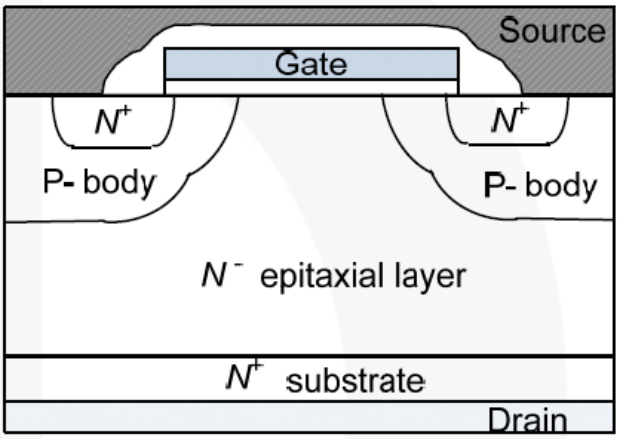
drain, the drain-to-source current rating and voltage blocking capabilities can be increased by developing the epitaxial layer (drain drift area). Right after the kind of vertical MOSFETs in commerce:

1. The VMOSFET Design: The first commercialized design, this one has a V-groove at the gate area, as shown in Figure 4 (a). VMOSFETs were replaced with DMOSFETs due to manufacturing stability issues and a large electric field at the tip of the V-groove.



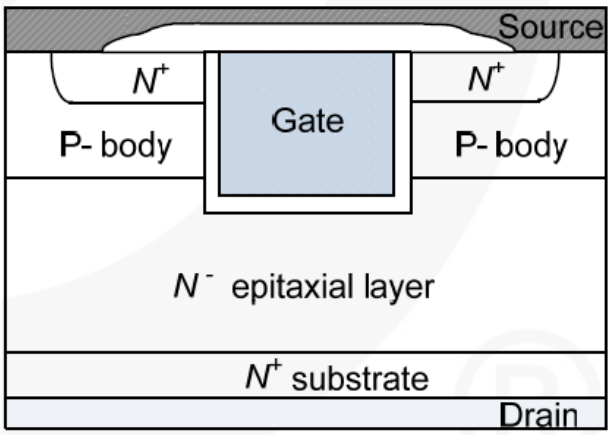
3.11 VMOSFET Design [174]

2. As shown in Figure 4 (b), the DMOSFET Design features a double-diffusion structure with a P-base area and a N+ source region. It is the design that has had the most commercial success.



3.12 DMOSFET Design [174]

3. The UMOSFET Design: This design has a U-groove at the gate area, as shown in Figure 4 (c). When compared to VMOSFETs and DMOSFETs, higher channel density reduces on-resistance. The trench etching technology was used to market UMOSFET designs in the 1990s.



3.13 UMOSFET Design [174]

3.4 Advantages of MOSFETs

3.4.1 High Input Impedance and Voltage and Controlled Device

To keep the current-controlled device (BJT) in the on state, a base drive current equal to one-fifth or one-tenth of the collector current is required. For the high-speed turn-off of the current-controlled BJT, a greater reverse base drive current is required.

Because of these qualities, designing a base drive circuit becomes complicated and costly. A voltage-controlled MOSFET, on the other hand, is a switching device that is driven by a channel at the semiconductor's surface via the field effect caused by the voltage supplied to the gate electrode, which is isolated from the semiconductor surface. The drive circuit design is simpler and less expensive because the needed gate current during the switching transient, as well as the on and off states, is modest.

3.4.2 Unipolar device, majority carrier density and high fast switching speed

Because there are no delays due to minority carrier storage and recombination, the switching speed is orders of magnitude faster than the BJT. As a result, it has an advantage in a high-frequency operation circuit with substantial switching power loss.

3.4.3 Wide Safe Operation Area (SOA)

Because high voltage and current may be delivered simultaneously for a short period of time, it has a broader SOA than the BJT. This eliminates the possibility of destructive device failure owing to a second breakdown.

3.4.4 Forward Voltage Drop Associated with a Positive Temperature Coefficient

When the temperature rises, so does the forward voltage loss. When two devices are connected in parallel, the current flows through them evenly. As a result, the MOSFET is easier to utilize in parallel than the BJT, which has a negative temperature coefficient and a forward voltage loss.

3.4.5 Disadvantage

In high breakdown voltage devices over 200 V, the conduction loss of a MOSFET is bigger in respect to a BJT,

which has the same voltage and current rating due to the onstate voltage drop.

3.4.6 Basic Characteristic

The P-type body region is transformed into a base, the N+ source region is transformed into an emitter, and the N-type drain region is transformed into a collector (see Figure 3.14). When the parasitic BJT is turned on, the breakdown voltage lowers from BVCBO to BVCEO, which is 50% of BVCBO. If a drain voltage greater than BVCEO is applied in this state, the device enters an avalanche breakdown state. The second breakdown destroys the drain current if it is not externally limited. To prevent the parasitic BJT from turning on, the N+ source region and the P-type body region must be shorted by metallization.

If the VDS rate of increase is high in the high-speed turn-off state, a voltage drop occurs between the base and the emitter, causing the BJT to switch on. This is avoided by raising the doping density of the P- body region, which is at the bottom of the N+ source region, and by slowing the switching speed of the MOSFETs by designing the circuit with a high gate resistance. Because the source area is short, another parasitic component, the diode, forms. This is employed in half-bridge and full-bridge converters.

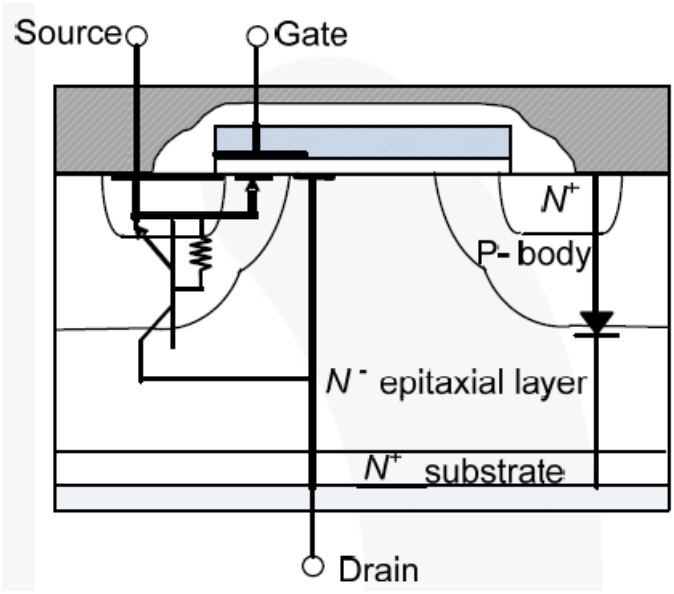


Fig. 3.14 MOSFET Vertical Structure Showing Parasitic BJT and Diode [174]

3.4.7 Output Characteristics

ID characteristics are due to VDS in various VGS conditions. The following are the three zone, as you can see in Fig. 3.12.

1. Ohmic region: A zone of constant resistance. If the drain-to-source voltage is zero, regardless of the gate-to-source voltage, the drain current is also zero. This region is on the left side of the boundary line VGS - VGS(th) = VDS (VGS - VGS(th) > VDS > 0). Even if the drain current is quite high, power dissipation is maintained in this region by limiting VDS(on).

2. Saturation region: A constant-current region. It is at the right side of the VGS – VGS(th) = VDS boundary line. Here, the drain current differs by the gate-to-source voltage, and not by the drain-to-source voltage. Hence, the drain current is called saturated.

3. Cut-off region: gate-to-source voltage is lower than the VGS(th) (threshold voltage).

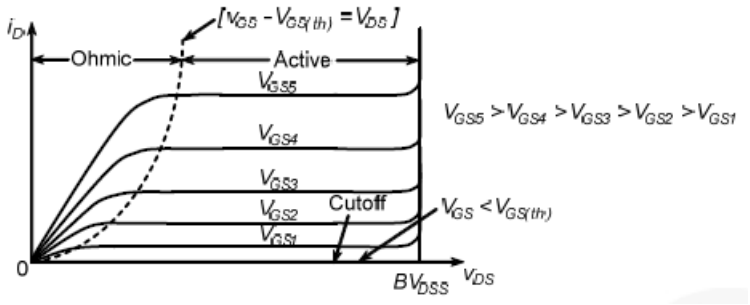


Fig. 3.15 Output characteristic

3.4.8 Transfer Characteristics

According to Equation 3,10, a logic-level device has a parabolic transfer curve. This is true only in the low i_D of the transfer curve of a power MOSFET; the other sections exhibit linearity. This is because the carrier's mobility is not constant but diminishes when the electric field increases along with the i_D at the inverse layer. i_D characteristics due to VGS in the active region (refer to Figure 3.16). i_D equation due to V_{GS}:

$$i_D = K\left(v_{GS} - V_{GS(th)}\right)^2$$

$$K = \mu_n C_{ox} \frac{W}{2L} \qquad \text{Eq. 3.10}$$

where:

un : majority-carrier mobility;

C_{ox} : gate oxide capacitance per unit area;

$C_{ox} = \varepsilon_{ox}\, S/T_{ox}$;

ε_{ox} : dielectric constant of the silicon dioxide;

T_{ox} : thickness of the gate oxide;

W: channel width; and

L: channel length.

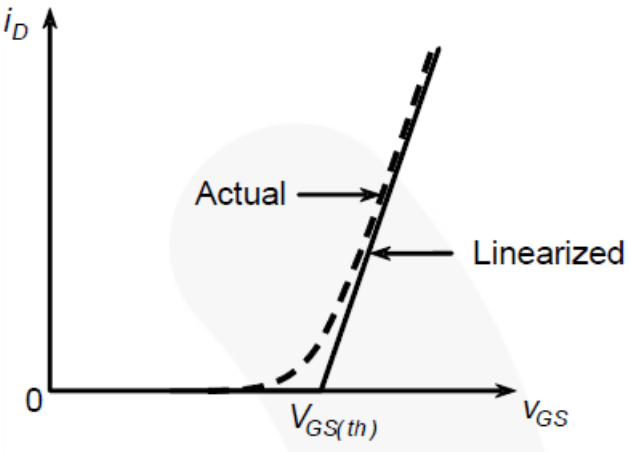


Fig. 3.16 Transfer Curve

3.5.9 OFF State

BVDSS

BVDSS is the highest drain-to-source voltage that a MOSFET can withstand without the bodydrain P-N junction avalanche breaking down in the off state (when the gate and source are shorted) and one of the best parameters to evaluate doping profile in MOSFETs. The measurement circumstances are VGS = 0 V, ID = 250 A, and the BVDSS determines the length of the drift region (N- epitaxy). Breakdown is caused by avalanche, reach-through, punch-through, Zener, and dielectric breakdowns. Three of these factors are discussed more below:

1. Avalanche Breakdown**:** The mobile carriers' sudden avalanche breakdown caused by the increasing electric field in the depletion region of the body-drain P-N junction up to a critical value. It is, among other things, the primary cause of breakdown.
2. Reach-Through Breakdown: possible case of avalanche breakdown occurring when the depletion region of the N– epitaxy contacts the N+ substrate.
3. Punch-Through Breakdown: When the depletion zone of the body-drain junction reaches the N+ source region, an avalanche occurs.

IDSS

The drain-to-source leakage current when the gate is shorted to the source in an off state. The increase in i_{DSS}, which is temperature sensitive, is substantial with increasing temperature, whereas the increase in BV_{DSS} is relatively little.

3.5 Turn-On Transient

Process of Channel Formation

Formation of the depletion region

When the gate electrode receives a tiny positive gate-to-source voltage (see Fig. 3.17).

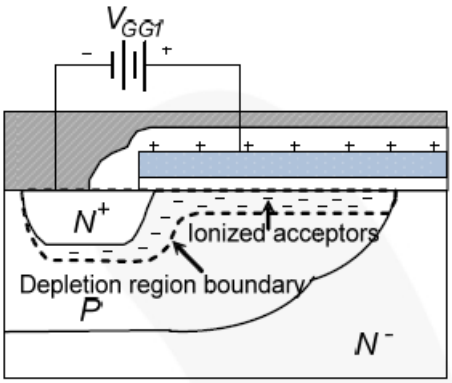


Fig. 3.17 Formation of Depletion Region [174]

A positive charge created in the gate electrode induces the equivalent amount of negative charge at the oxide-silicon interface (the P--body region beneath the gate oxide). An electric field pushes holes into the semiconductor bulk, and acceptors with a negative charge form the depletion area.

3.5.1Formation of the inversion layer

As the positive gate-to-source voltage increases (Fig. 3.18) the depletion region expands towards the body, dragging free electrons to the interface. Thermal ionization produces these free electrons. Free electrons form free holes, which are driven into the semiconductor bulk. The electrons drawn by the positive charge of the holes from the N+ source neutralize the holes that have not been driven into the bulk. As the provided voltage increases, the density of the body's free holes and the interface's free electrons becomes equal. The free electron layer is now referred to as an inversion layer. The inversion layer allows current to flow by serving as the conductive pass (=channel) for the MOSFETs' drain and source.

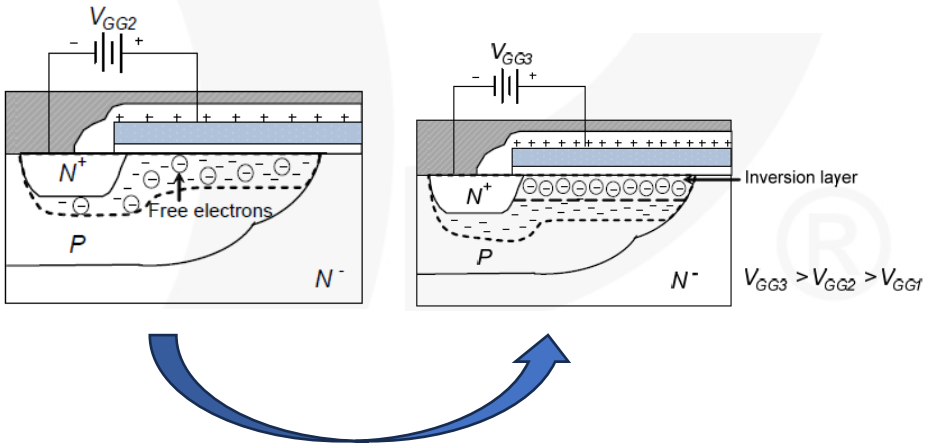


Fig. 3.18 Formation of the inversion layer and successive channel creation [174]

3.5.2 ON State

The rise in drain-to-source voltage (V_{DD}) causes a change in drain current (i_D) (V_{GS} remains constant). When the channel is created and V_{DD} is applied, i_D begins to flow. When the VGS remains constant while the V_{DD} increases linearly, the i_D increases linearly as well. When the real V_{DD} exceeds a particular threshold, the rate of growth in i_D slows, as illustrated in the MOSFET output characteristics graph. It eventually becomes a constant value that is independent of V_{DD} and depends on V_{GS}.

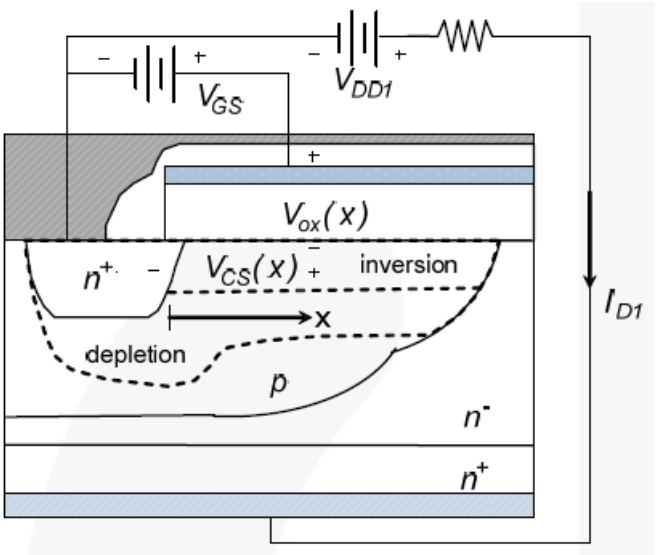


Fig. 3.19 Spatially uniform: Inversion Layer Thickness Changes [174]

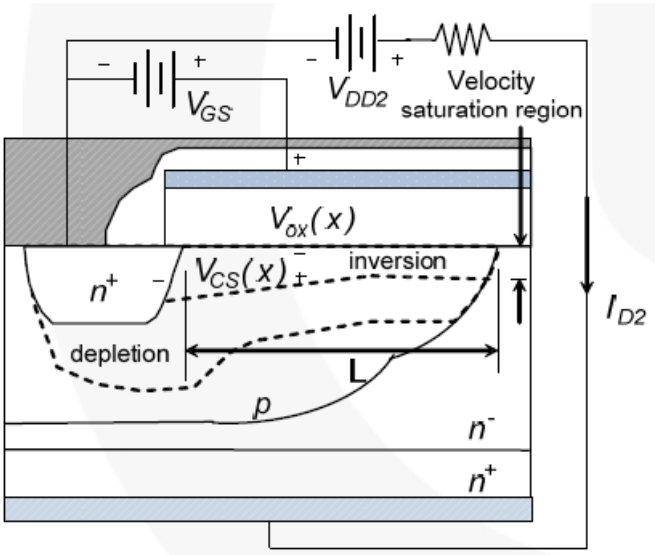


Fig. 3.20 Spatially not-uniform: Inversion Layer Thickness Changes due to the Increase of the Drain-to-Source Voltage [174]

In order to understand the characteristics, take a look to Fig. 3.20, in which the voltage drop at $V_{CS}(x)$ due to ohmic resistance when i_D is flowing at the inverse layer. $V_{CS}(x)$ is the channel-to-source voltage at x distance from the source. At all x values, this voltage equals the $V_{GS}(x)$ - $V_{ox}(x)$ is the gate-to-body voltage that crosses the gate oxide from the source at a distance of x, and it reaches its maximum at V_{DS} at x=L (the channel's drain end). When low voltage V_{DD}=V_{DD1} is given, as illustrated in Figure 3.18, low i_D (=i_{D1}) flows, with nearly little voltage drop of $V_{CS}(x)$. Because $V_{ox}(0) - V_{ox}(L)$ is constant, the inversion layer's thickness remains constant.

As V_{DD} is increased, i_D increases, $V_{CS}(x)$ voltage drops, and the value of $V_{ox}(x)$ lowers. Starting at x=L, these lower the thickness of the inversion layer. As a result, the resistance rises and the i_D graph begins to flatten rather than rise with the increase in V_{DD}. When $V_{ox}(L)$ =$V_{GS} - V_{DS}$ =$V_{GS}(th)$, when i_D grows, the inversion layer at x=L does not evaporate due to the high electric field (J=E) created by the thickness reduction, and it retains the minimal thickness. The high electric field not only keeps the inversion layer's thickness to a minimum, but it also saturates the velocity of the charge carrier at $V_{ox}(L)$ =$V_{GS} - V_{DS}$ =$V_{GS}(th)$.

The velocity of the charge carrier first increases with the increase in the electric field and eventually becomes saturated. When the electric field hits 1.5x10^4[V/cm] and the electron drift velocity exceeds 8x10^6 [cm/s], silicon begins to saturate. The device enters the active zone at this point. When a greater V_{DD} is applied the electric field at x=L

expands and the channel region with the smallest thickness expands towards the source. V_{DS} becomes $V_{DS} > V_{GS} - V_{GS}(th)$ as V_{DD} increases, while i_D remains constant.

Chapter 4

Raman Spectroscopy

The experimental stress measurements in power electronic devices are not conventional since they contain a wide range of materials and have a complex structure. It is now essential to measure local stress or the presence of contaminant layers of semiconductor devices using a non-invasive technique; a viable solution for this purpose could be Raman spectroscopy. This technique is particularly effective in SiC devices because phononic modes modes frequencies changes by applying a mechanical stress as a result in a local variation in polarizability; additionally, SiC is distinguished by strong covalent bonds, hence Raman signals are particularly intense and accurate measurements is possible.

4.1 Introduction

Sir Newton made the first optical measurement in 1666, passing the sun's rays through a triad of glass prisms. Examining the image on a piece of paper, he noticed that the white light had produced colors ranging from red to violet. This combination of lines of various colors is known as a spectrum. The foundations of analytic spotting were laid in 1814, the year in which Fraunhofer demonstrated how the spotting of the sun was not continuous, as distinguished by the presence of dark bands. Kirchhoff arrived at the notion that each element has its own perception in 1859. The result will be nothing more than the result of a probe interaction with the material, i.e., the probe after the interaction will carry the fingerprint of the material with which it interacted. Based on the characteristics of the probe and the measured properties, spectroscopy can be classified into several way, referring to the probed property and depending on the used technology. If the interaction involves the structural properties of the crystal, it is called Raman spectroscopy, named after the physicist who discovered it and won the Nobel Prize in 1930.

The first observation of the Raman effect was made by Raman and Krishnan, who illuminated various liquids and gases purified with blue-ultraviolet components of solar light and saw that a certain amount of light emerged at lower energies. They also discovered that the frequency difference between incident and emitted light depends on the sample used, demonstrating one of the differences between Raman spectroscopy and the more often used fluorescence. Furthermore, it became quickly clear that the frequency

change corresponded to the infrared absorbed frequencies of the samples. The effect was then related to the material's vibratory properties.

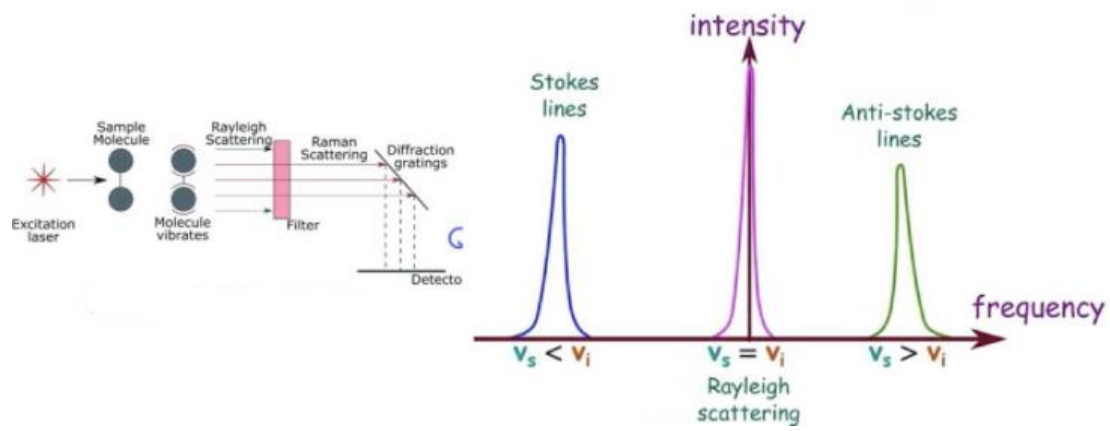


Fig. 4.1 Exemplification of Raman scattering with relative scattering

4.2 Theoretical background

The Raman spectroscopy provides important information on the structural properties of materials, its working principle consists of the effects of the electrical field of the optical radiation on the crystals or molecules that interacts with the field due to their polarizability. The goal is to characterize the stress applied to a 4H-SiC crystal. This is possible by Raman spectroscopy as the stress induces a strain in the crystal and hence it works on the polarizability resulting in a “Raman shift”, i.e. in the frequency shifting of some Raman modes.

Before analyzing the case, it is useful to review the models used in this technique's research. The first treatment is the classic; assume the moment of induced dipole in a molecule via electrical radiation:

$$\bar{\mu} = \tilde{\alpha}\bar{E} \qquad \text{Eq. 4.1}$$

Where can "E" be rephrased analytically, such as:

$$\bar{E} = \overline{E_0}\ \cos(\omega_0 t) \qquad \text{Eq. 4.2}$$

Let’s now introduce polarizability as follows:

$$\tilde{\alpha} = \alpha_0 + \left(\frac{\partial \alpha}{\partial q}\right) q \qquad \text{Eq. 4.3}$$

With:

$$q = q_0 \cos(\omega t + \delta) \qquad \text{Eq. 4.4}$$

When we replace 4.2 with 4.1 and use trigonometric note relationships, we get:

$$\bar{\mu} = \alpha_0 \bar{E} \cos(\omega_0 t) + \frac{1}{2}\left(\frac{\partial \alpha}{\partial q}\right) q_0 \overline{E_0} \{\cos[(\omega - \omega_0)t - \delta] + \cos[(\omega - \omega_0)t + \delta]\} \qquad \text{Eq.4.5}$$

The equation 4.5 contains three terms, each of which refers to a specific phenomenon:The first term refers to Rayleigh scattering, which is proportional to $\cos(\omega_0 t)$; the second term represents Stokes Raman diffusion, which is proportional to $\cos[(\omega - \omega_0)t - \delta]$; and the third and final term is Raman anti-Stokes diffusion, which is proportional to $\cos[(\omega - \omega_0)t + \delta]$.

One crucial need is that in order to appreciate Raman diffusion, the following conditions must be met:

$$\left(\frac{\partial \alpha}{\partial q}\right) q_0 \overline{E_0} \neq 0$$

$$\Longrightarrow \left(\frac{\partial \alpha}{\partial q}\right) \neq 0 \qquad \text{Eq. 4.6}$$

This means that the active Raman vibrations are only those that cause polarizability to vary.

We will return briefly to the meaning of Raman spectroscopy. We propose that you have a molecule in a vibratory state $|g\rangle$ and that an incidental photon with $\hbar\nu_i$ energy be absorbed, causing a transition to a virtual state. In this case, the molecule decade via a Stokes transition, ejecting a photon with energy $\hbar\nu_s < \hbar\nu_i$. According to the energy conservation principle, the difference $\hbar\nu_i - \hbar\nu_s$ causes the molecule to vibrate at a higher frequency $|c\rangle$ (figura 4.2 (a)).

Alternatively, if the initial state is one of excitement (a condition that can be easily obtained by squeezing the material), the molecule, after absorbing and emitting the photon, can decade into a lower-energy state, resulting in an anti-Stokes transition. In this case, $\hbar\nu_s > \hbar\nu_i$, which means that some of the molecular's vibratory energy ($\hbar\nu_{ba} = \hbar\nu_s - \hbar\nu_i$) has been converted into radiant energy (figura 4.2 (b)). In both cases, the

difference in energy between ν_s e ν_i corresponds to the difference between distinct energetic levels of the studied structure. The modern discoveries, based on numerous tests and studies, have revealed that when a crystal transmits or reflects electromagnetic radiation, in the infrared region, small amounts of assorbiment can be observed, assuming that the elemental cell has a permanent dipole moment or that it has been vibrated.

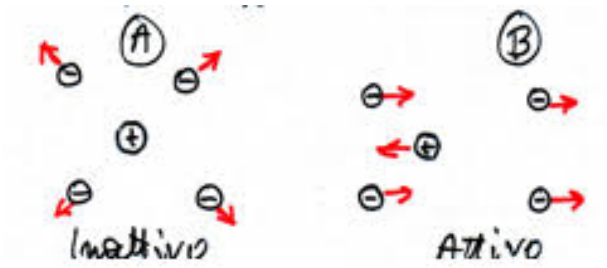


Fig 4.2 In case B, the vibration causes a dipole moment in the axial direction, which changes sign at each half-period, whereas in case A, the total-simmetric vibration does not cause a dipole moment.

The above states that the Raman effect will be found just for the stretching button B and mode A will not produce any Raman spectra. Indeed a configuration like the one shown in Fig. 4.2 B will result in a periodic variation in polarization, which may be observed using Raman spectroscopy.

If we take Maxwell's first equation in the simplest case, namely for an isotropic, homogeneous, and electrically neutral medium, we get:

$$div\ \bar{D} = div\ (\varepsilon_1(\omega)\bar{E}) \qquad \text{Eq.4.7}$$
$$= \nabla \cdot (\varepsilon_1(\omega)\bar{E}) = 0$$

Where$\varepsilon_1(\omega)$ is the real portion of the dielectric function recognized in $\tilde{\varepsilon}(\omega) = \varepsilon_1(\omega) + i\varepsilon_2(\omega)$.. If we substitute $\bar{E} = \overline{E_0}\ e^{i\bar{k}\cdot\bar{r}}$, or the solution of a sphere, with k the depth of the sphere, we get:

$$i\varepsilon_1(\omega)\bar{k} \cdot \bar{E} = 0 \qquad \text{Eq. 4.8}$$

This equation is satisfied in two circumstances:

1. When $\bar{k} \cdot \bar{E} = 0, \forall\ \varepsilon_1(\omega)$;; means that for each photon that is absorbed, a photon with an orthogonal edge E to is created, which is transversal (TO), since the dipole vibration follows the electric field.

2. $\varepsilon_1(\omega) = 0$, ∀ orientation of k. Longitudinal oscillations (LO) are observed in relation to the zeros of the real part of the dielettric function.

In the case of the 4H-SiC, the normal modes at the limit of wave length are four $(A_1 + B_1 + E_1 + E_2)$; it is worth noting that the modes B_1 are Raman inactive, while the modes A_1 and E_1 are acustic: this means that only the modes $3A_1, 3E_1\ e\ 4E_2$ are observable.

4.3 SiC Raman spectra.

As previously predicted, the silicon carbide can crystallize in different structures (polymorphism) with distinct characteristics. The most common allotropic shapes are the 4H, 6H, and 3C, for which we will show the relative angles and main characteristics.
Figure 4.3 depicts the Raman spectrum of a 6H-SiC microwire.

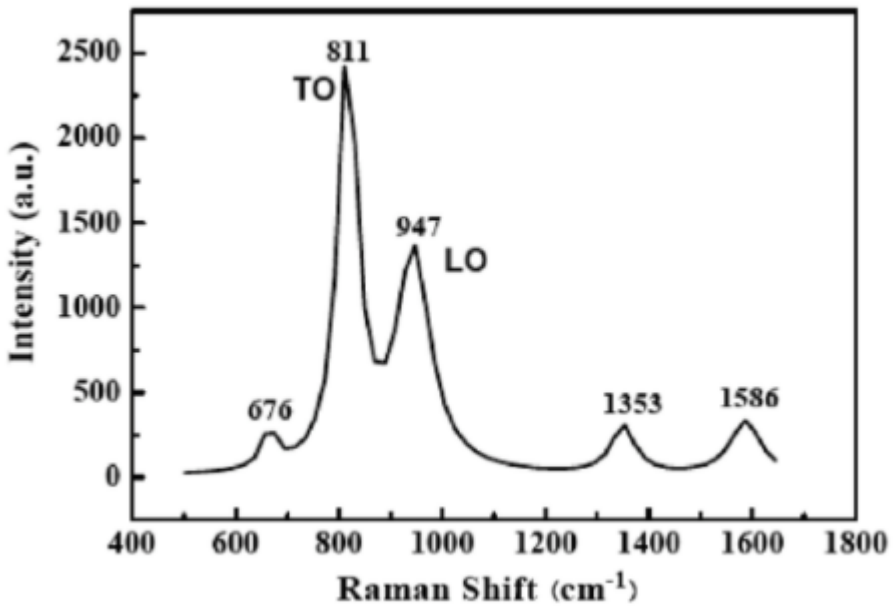


Fig. 4.3 6H-SiC Raman spectra [175]

In fig. 4.3, five peaks can be seen at approximately 676, 811, 947, 1353 e 1586 cm^{-1}.The first is due to faulty phononic modes [1, 2]. Peackes that fall at 811 e 947 cm^{-1} represent the transversal and longitudinal modes of the 6H-SiC, respectively.
SiC in 3C cristalline structure, as you can see in Fig. 4.4, has 6 Raman peacks: the Si phononic one at 521,7 cm^{-1}, longitudinal and trasverse mode due to bonding Si - C rispectively at 794,4 cm^{-1} and at 965,7 cm^{-1}, the ones due to C - C at 1355,8 cm^{-1} e a 1596,8 $cm^{-1}$and the one due to C – O at 1122,6 cm^{-1} [4].

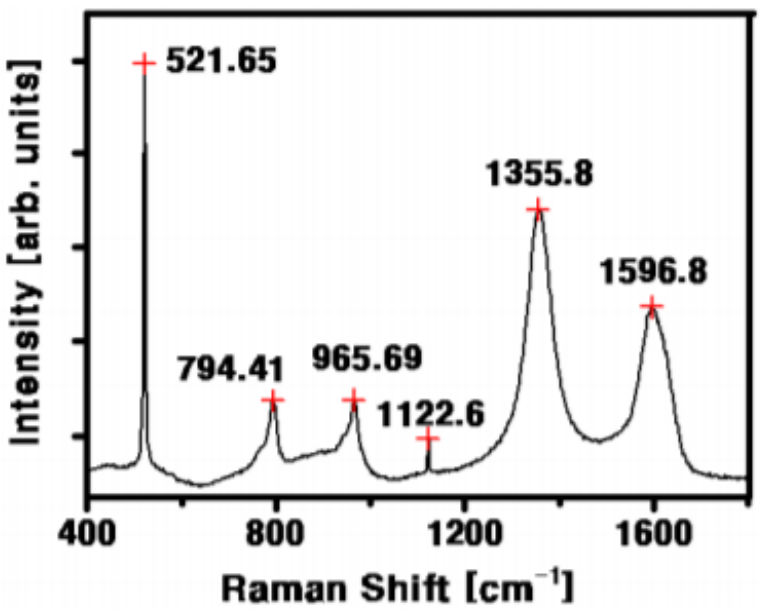


Fig. 4.4 3C-SiC Raman spectra [176]

The polytype studied in the thesis work is the 4H-SiC, which has two transversal acoustic modes of 203 cm^{-1} and at 265 cm^{-1}, one longitudinal acoustic mode at 611 cm^{-1}, two transversal optically active modes of 779 cm^{-1} and at 796 cm^{-1}, and two optically active modes of 1524 cm^{-1} and at 1714 cm^{-1}.

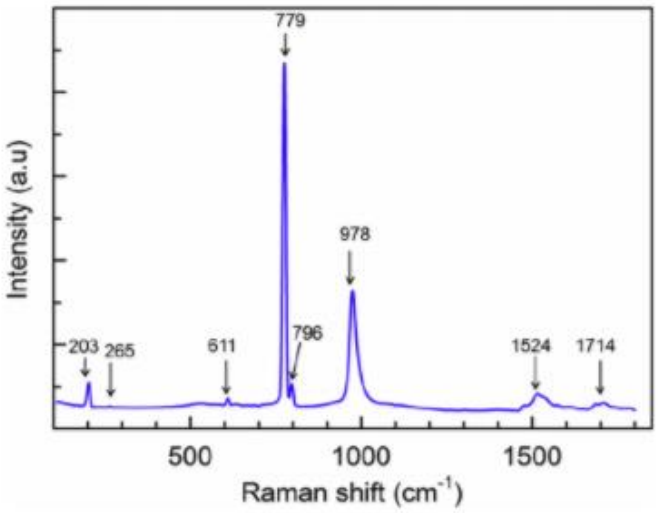


Fig. 4.5 4H-SiC Raman spectra [175]

Raman confocal system experimental setup

The Raman system is depicted schematically in Fig. 4.6.

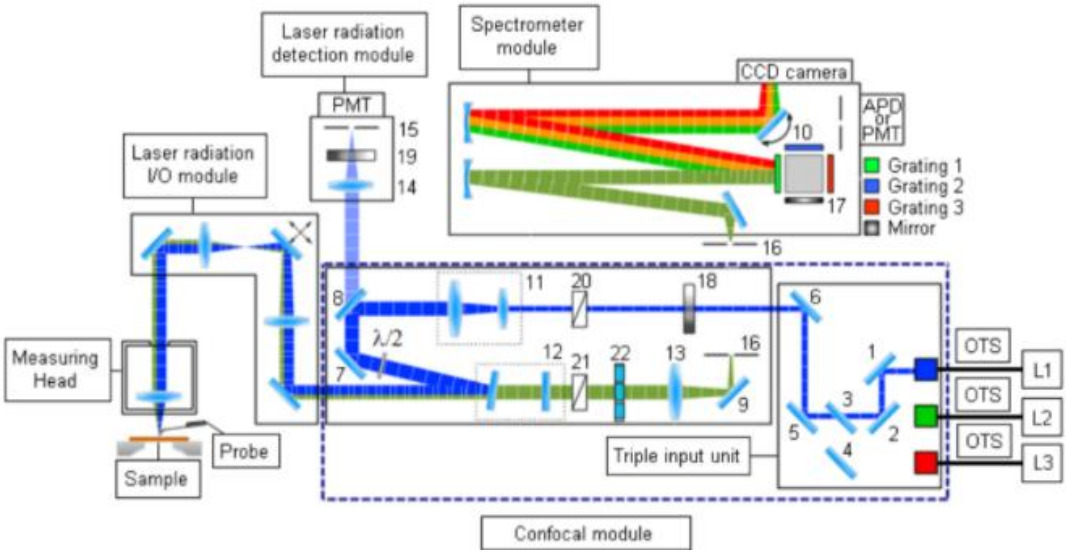


Fig. 4.6 Raman spectroscopy schematic diagram

It consists of a combined system with an AFM head, designed for the execution of both TERS and Raman measurements. The system is outfitted with two solid-state lasers (DPSS: Diode Pumped Solid State Laser) that operate at 532 nm and 473 nm, as well as a gas laser that operates at 632.6 nm (laser HeNe).

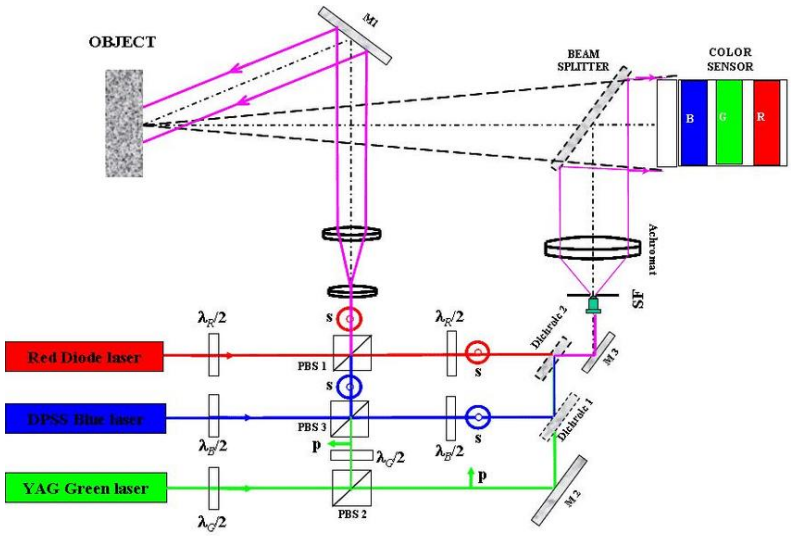


Figure 4.7: A laser system comprised of two DDPSLs and a HeNe-gas source.

The sources may be changed by simply moving the mirrors, making the system extremely flexible. The laser light passes through a neutral filter that acts as a reversible attenuator and allows to change the optical density used for measurement. Then a beam expander and a mirrors and a focalization optic complete the optical equipment. This last optical

part is a 100X objective with a long working distance (WD=6mm) and a large numerical aperture (Mitutoyo M Plan Apo 100X /0.70).

Fig. 4.8 Mitutoyo M Plan Apo 100X /0.70 camera lens

Camera lens is used in order to allows for the collection of a good amount of light from the sample while remaining at a safe distance from the indagated surface, ensuring the possibility of installing the TERS (Tip Enhanced Raman Scattering) system between the optic and the sample holder. The light reflected by the sample and collected by the objective travels down the same optical path until it reaches a system of filters designed to eliminate laser radiation. The quality of these filters is one of the key factors in achieving overall system quality. In our case, two band rejection filters (Razo Filter Semrock) were installed; the first serves as a mirror and is installed on a mechanism that is optimally oriented, while the second serves to improve the overall dynamic of the instrument.

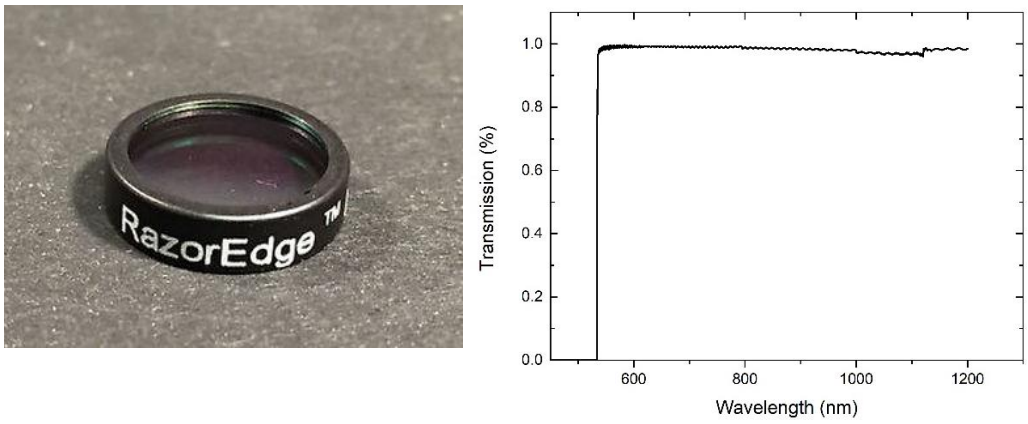


Fig. 4.9 Filter Razo Filter Semrock (on the left) and its optical transmission curve (on the right).

The light that passes through the second filter is focused by a lens system on a pinhole, the size of which may be adjusted, and a confocal assembly is realized in conjunction with the spectrometer's focalization system. The spectrometer is outfitted with four differentiating gratings with varying numbers of rows per millimeter, allowing to tailor the dispersive power to a specific experiment. The detector used is an cooled camera Andor IDUS with a triple Peltier and outfitted with an external cooling liquid system. The camera can work down to -65°C.

Chapter 5

SiC Substrate growth techniques, defectivity and Wafer Level Annealing (WLA)

Due to the increasing demand for more efficient and reliable power devices, the growth of sufficient amount of SiC ingots stands as a pivotal step become a crucial target of SiC industries. Unfortunately the growing process is not easy and the presence of defects in the epitaxial active regions have hampered the production: high yield and low defect density are essences of SiC commercialization. Defects arise as a result of deviations in growth kinetics and contamination during the process, so it's of paramount importance archive high quality ingot, trying to optimize the growing and post processing processes. Threading screw dislocations (TSDs), threading edge dislocations (TEDs), basal plane dislocations (BPDs), micro-pipes (MPs), inclusions, polytypes, and stacking faults (SFs) are the most common defects in SiC single crystal. To date, the density of MPs has been reduced to nearly nothing, although TSDs, TEDs, and BPDs are abundant. Threading dislocations (TDs) have been found to have a substantial link with diode breakdown voltage and leakage current [81].

MP originates as a pinhole that extends through the entire SiC wafer along the <0001> crystal direction, resulting in substantial performance deterioration such as high leakage current and early breakdown. BPD degrades SiC bipolar devices by causing Shockly-type SFs to form during carrier injection, resulting in shortened carrier lifespan due to rising on-state resistance [82]. As a result, it is critical to eliminate defects by optimizing SiC single crystal growth processes and corresponding main parameters.

Even today's best SiC wafers have several structural defects, including a substantial number of screw dislocations ($\sim 10^6 cm^{-2}$), that limit the quality of epitaxial layers,. When compared to the number of SiC-based power devices on the market, the availability of a wide range of optoelectronic and other devices made from SiC highlights the fact that the full potential of this material has yet to be realized.

In this chapter, growth techniques will be described and the defectivity will be analyzed. More in particular, the Wafer level annealing (WLA) technique , a thermal process able to reduce defectivity in SiC substrate, will be described and studied.

As previously said, it's almost impossible avoid all the kinds of defectivity during the epitaxy process. It was studied and confirmed that the generation of a defects can be reduced using process optimization during and after the ingot growth. WLA is a thermal treatment applied before epitaxy. This process presents some issues both coming due the natural SiC process and equipment. In the first case it's shown that thermal cycles with a temperature between 1200 °C and 1800 °C generate a graphite/graphene layer of about some nanometers which interfere with epitaxy and so electrical performances; in the second one carbon contaminations due the equipment can help the formation of unwanted layers. However, WLA has the power to help recombination in the crystal, almost transmuting BPDs in a kind of defectivity which has a quite lower killer rate (i.e. that does not kill the device during its normal operation reducing its lifetime).

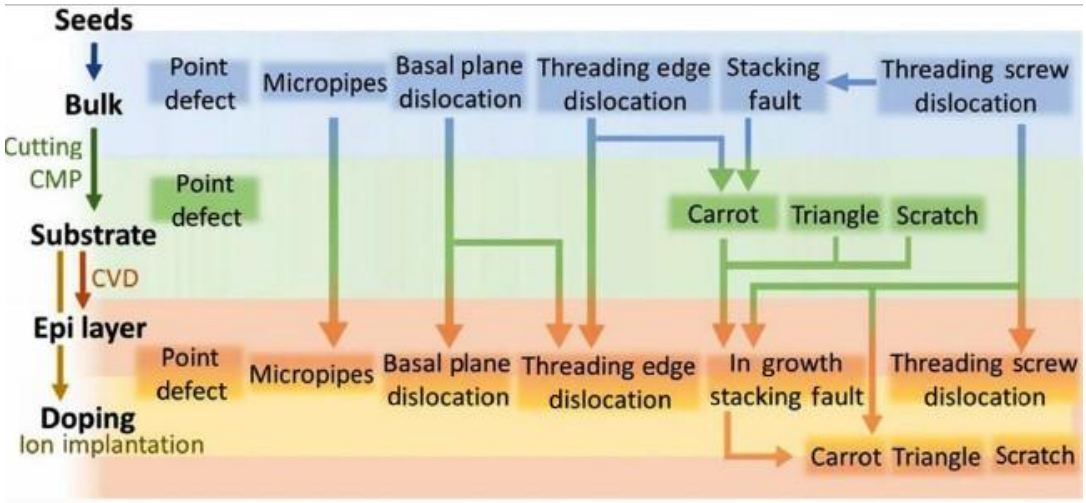


Fig 5.1 Defectivity on SiC substrate and relative possible evolution [177].

5.1 SiC material growth

The phase diagram of SiC in an inert gas atmosphere at ambient pressure is characterized by a disintegration of stoichiometric SiC at about 2800 °C into carbon and a Silicon solution containing approximately 13% carbon [83, 84]. (Fig. 5.2).

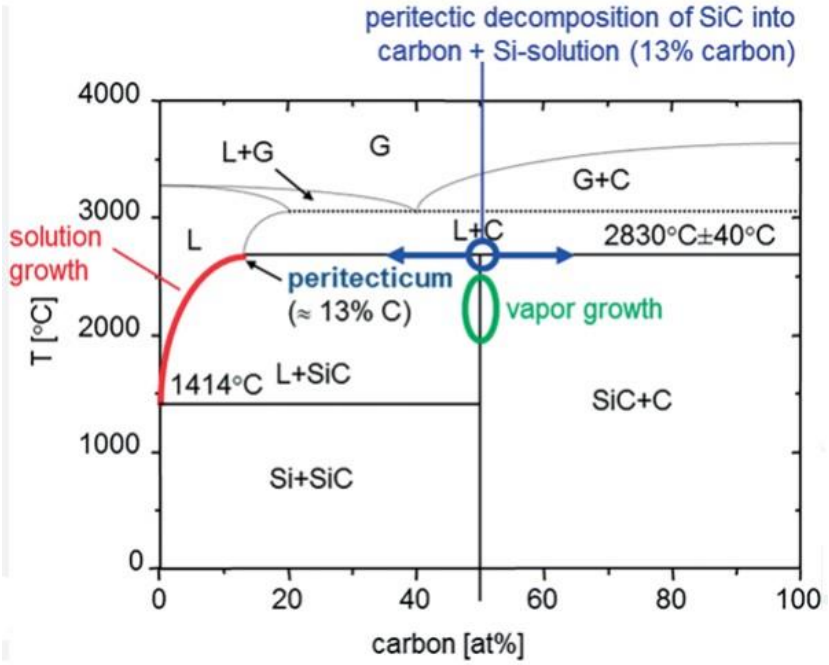


Fig. 5.2 Phase diagram of SiC [178]

Variations on the phase diagram can occur due to severe heat conditions ranging from 2000 °C to 3200 °C. Aside from carbon, no other materials are available as containers under these experimental regimes.

Crystal formation from a stoichiometric "SiC-melt" is not possible due to the phase structure of SiC (fig. 5.2). Sublimation of SiC source material and recrystallization of a SiC single crystal at a slightly lower temperature can be used to perform growth via physical vapor transport in the temperature zone between approximately 1900 °C and 2400 °C.

5.2 Physical vapor transport (PVT) growth

The gas phase is mostly made up of Si, Si_2C . The gas phase contains almost no molecular SiC. The partial pressure difference of the various SiC gas species Si, Si_2C and SiC_2 between the hot SiC source and the somewhat colder SiC seed crystal drives SiC physical vapor transfer (PVT) growth (fig. 5.3).

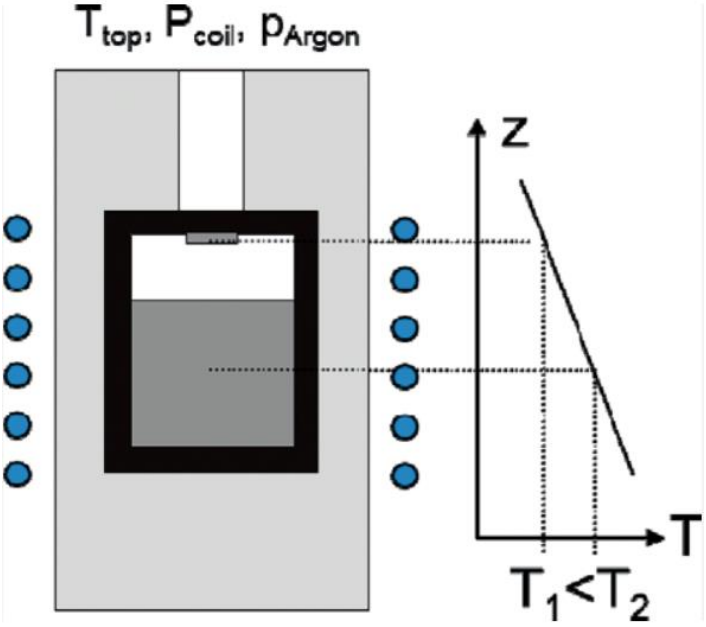


Fig. 5.3 Growth cell for physical vapor transport (PVT) of SiC [178]

In experiments, the rate of formation is significantly affected by the average temperature within the growth cell, the temperature gradient between the SiC source and the SiC seed, and the pressure of the inert gas. This pressure determines the partial pressures of the gases associated with SiC. Because the gas phase is dominated by the species Si, Si_2C and SiC_2, the following heterogeneous chemical processes drive the growth in the chamber:

$$SiC_2(gas) + Si(gas) \leftrightarrow 2SiC(solid)$$

$$SiC_2(gas) \leftrightarrow 2C(solid) + Si(gas)$$

$$SiC_2(gas) + 3Si(gas) \leftrightarrow 2Si_2C(gas) \qquad \text{Eq.5.1}$$

Because the partial pressure of gaseous Si is greatest below 2500 °C (see, for example, Lilov et al. [85]), the molar concentration of the molecule SiC_2 restricts the development rate of solid SiC.

The partial pressures of the different gas species are connected to each other by the following equations according to the law of mass action:

$$p_{SiC_2} p_{Si} = K_1(T)$$

$$p_{SiC_2} = K_2(T)p_{Si}$$

Eq. 5.2

$$p_{SiC_2}p_{Si}^3 = K_3(T)p_{Si_2C}^2$$

The temperature-dependent equilibrium constants K_1, K_2 and K_3 can be determined from the thermodynamic data of the solid and gaseous material components [86].
If there is no considerable graphitization of the SiC source material during sublimation and no incorporation of Si-droplets or C-inclusions during SiC crystallization, both sublimation and crystallization occur at equal Si- and C-fluxes:

$$Condition: J_{Si} + 2J_{Si_2C} + J_{SiC_2} = J_{Si_2C} + 2J_{SiC_2} \quad \text{Eq.5.3}$$

In which J_γ: molar fluxes of the gas species ν

No SiC deposition is detected on the side walls of the gas room due to an axially oriented temperature differential in the PVT growing cell. As a result, total Si species transfer to the graphite side walls is zero:

$$J_{Si} + 2J_{Si_2C} + J_{SiC_2} = 0 \quad \text{Eq. 5.4}$$

Gas species motion from the SiC source to the SiC seed can be controlled using an inert gas such as argon. The partial pressure of the inert gas produces a diffusion limited mass transport regime that allows control of the SiC crystal growth rate by setting a distinct total pressure. According to an electrical circuit in which the electrical current I is determined by the ratio of the electrical potential difference U and the resistance R, the SiC related species transport between SiC source and SiC seed can be calculated from the ratio of the partial pressure differences p (i.e. determined by the temperature difference T = TSource - TCrystal) and the so-called mass transport resistance R_{diff} for species diffusion. If the kinetics of SiC sublimation at the source and SiC crystallization at the seed are not the limiting factors, species motion (diffusion constant D of gas species) through the gas room described by the mass transport resistance R_{diff} may be controlled by the inert gas pressure pInert setting value.

$$R_{diff} = \frac{R\bar{T}d_{SC}}{D_v} \quad with\ D_v \propto \frac{1}{p_{inert}} \rightarrow R_{diff} \propto p_{inert} \quad \text{Eq. 5.5}$$

where R is the real gas constant, and $\overline{T}$ is the average growing temperature.

$$\bar{T} = (T_{source} - T_{crystal})/2$$

A constant growth velocity $v_{crystal}$ is found in the case of a pure diffusion limited growth mode, and the crystal length LCrystal rises linearly with growth time t.

If the heat of crystallization cannot be entirely dissipated through the growing SiC crystal, the temperature of the SiC crystal surface rises and the temperature differential $\bar{T} = T_{source} - T_{crystal}$ (= driving force for mass transport) decreases. As a result, the growth velocity vGrowth decreases.

5.3 Solution growth

To overcome the limited solubility of C in Si at temperatures below 2000 °C, metal additives such as Cr, Ti, and Al to Si, as well as pure metal solvents, have been used since the beginning [87-89].

A tremendous development in the solution growth of bulk SiC has occurred over the previous two decades.

Hofmann and Müller pioneered large-scale growth, which was developed by Epelbaum et al. [90]. The management of the carbon concentration inside the melt and its transfer to the growth interface is still a major difficulty. Graphite is commonly employed as a crucible material, which is largely burned by silicon dissolution. In this case, the wetting behavior of the solution is heavily influenced by the micro-morphology of the graphite. The Czochralski-like growth approach is related to top seeded solution growth (TSSG) [91, 92]. In some circumstances, the accelerated crucible rotation method (ACRT) improves melt mixing. Kusonoki et al. [93] reported the growth of a 75 mm crystal diameter and a growth rate of 200 m/h using Si-Cr and Si-Ti solutions at a growth temperature of up to 1940 °C. For smaller crystal diameters, growth rates of up to 1 mm/h were demonstrated. These rates of increase make solution growth competitive with the cutting-edge PVT approach. Aside from Si melt growth using the Czochralski process, crystal enlargement during SiC solution development appears to be as challenging as it is in PVT growth.

The introduction of metal additions during SiC solution development to promote C-solubility in the melt results in the integration of these unintended dopants into the SiC

crystal up to their solubility limit, which can lead to an alteration the electronic properties of the semiconductor substrate.

The vapor-liquidsolid (VLS) mechanism has been examined for foundational studies of solution-based growth kinetics, which demonstrated an improved supply of C-species at the growth interface compared to typical top seeded solution growth [94-96]. Solution growth, like PVT growth, occurs near thermodynamic equilibrium and so results in a decreased defect density.

Aside from SiC's superior structural quality (97), the closure of so-called micropipes (i.e. open hollow core screw dislocations, see section 4.2) has been proven (98, 99).

5.4 Chemical Vapor Deposition (CVD) growth

Chemical vapor deposition (CVD) is the most often used epitaxial growth technology for SiC because it allows for precise control of epitaxial layer thickness and impurity doping while maintaining a tolerable growth rate and good surface morphology. For common SiC CVD techniques, growth temperatures range from 1200 to 1800 °C, while growth pressures range from several tens of Torr to air pressure.

Typical CVD approaches for SiC epitaxial layer formation use distinct Si and C sources. Silane is the most often utilized silicon source, and other hydrocarbons have been used as carbon sources. Both are fed into the reactor via a high-purity H_2 carrier gas. Propane has been the most widely utilized hydrocarbon, owing to its relationship with the first successful demonstration of large-area epitaxial SiC on Si substrates [100], but methane, ethylene, and acetylene have been employed less frequently.

Methane is of interest due to the higher purity available from commercial sources when compared to propane, albeit the higher thermal stability results in a lower C source cracking efficiency [101]. Chlorine-based silicon sources, such as SiH_2Cl_2 and Si_2Cl_6, have been used to grow 3C-SiC on Si [102, 103]; one advantage is that Cl is to reduce silicon codeposition.

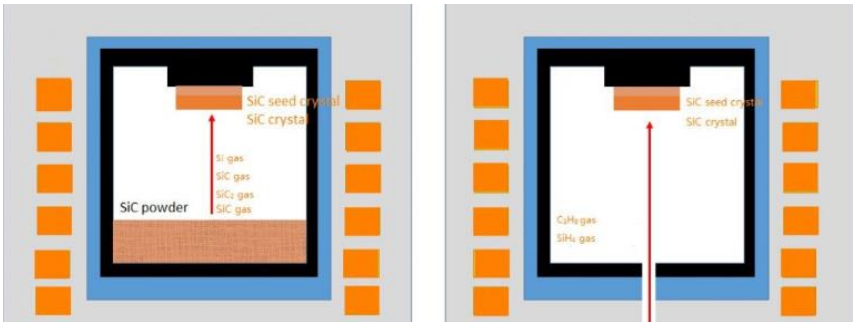


Fig. 5.4 CVD reactor and growth cell

5.5 CVD reactor set-up

The quartz horizontal reactor running at air or low pressure has been the most often utilized simple reactor structure for SiC CVD (Fig. 5.5), and it can be water-cooled or warm-walled.

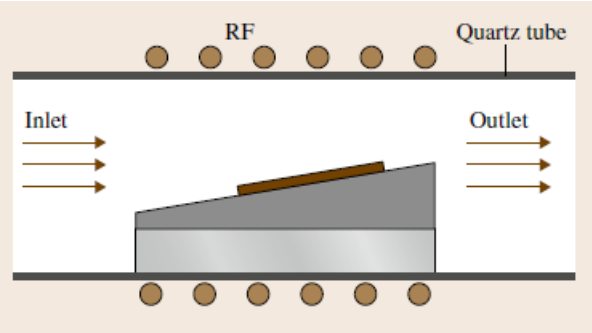


Fig. 5.5 horizontal water-cooled cold-wall reactor

The gases used include silane (SiH_4) and propane (C_3H_8), along with a significant amount of H_2. The flow rate of silane gas determines the growth rate, however the layer quality and density of defects such as cubic SiC inclusions, dopant incorporations, and so on are heavily reliant on the growth temperature and flow rate of propane at a given growth rate. When the silane flow is increased above a specific threshold, the morphology of the formed layer rapidly deteriorates. This type of technology has been used to achieve growth rates of a few um/h. Increasing the carrier gas flow (decreasing the residence time of the precursor), lowering the deposition pressure, and tilting the susceptor with regard to the gas flow are all methods for minimizing doping and thickness nonuniformities. More importantly, the slow growth rate and parasitic deposits falling from the reactor wall make thick (> 50 um) SiC epilayers with good surface shape difficult to form. Vertical cold-wall reactors have also been developed and employed to grow high purity and crystal quality SiC [104-106]. Precursor gases were introduced from the reactor's top, and particles dropping from the ceiling were prevented in the horizontal cold-wall reactor. The attached sample were rotated at speeds of up to 1500 rpm to improve homogeneity and prevent gas recirculation in the chamber. This rapid rotation acts as a pump for the gas flow. With a growth rate of 5-6 um/h, a background impurity level of less than $10^{14} cm^{-3}$ can be usually obtained.

Despite the vertical reactor produced a similar growth rate to the horizontal cold-wall reactor, longer growth durations could be utilized. Using this type of reactor, thick epilayers as thick as 50 um have been created. It was [107] propose horizontal hot-wall

reactors to manufacture thick, high-quality epilayers for power device applications in a reproducible manner.

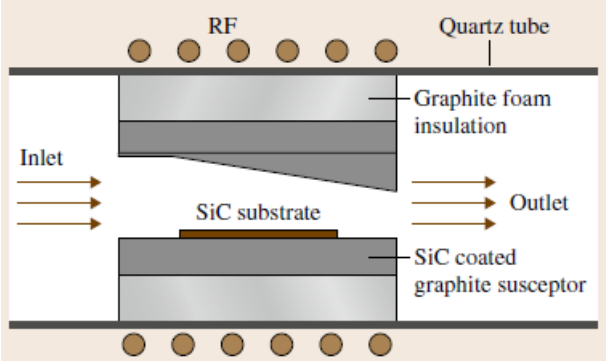


Fig. 5.6 Typical horizontal hotwall SiC CVD reactor [179]

The hot wall reactor was designed to achieve very high heating efficiency as well as high cracking efficiency of the precursors because gases could be heated considerably more efficiently in a hot-wall reactor. Furthermore, because the solution is heated more evenly, Si droplet production just above the sample surface may be prevented, allowing for a significantly higher silane flow to be used for SiC growth. Because the reactor walls are all heated (Fig. 5.6), the parasitic deposits on the reactor walls are polycrystalline SiC, which adheres to the wall more strongly than amorphous SiC or byproducts do in cold-wall reactors. Because of these factors, it is possible to grow SiC at a considerably faster rate and over a longer period of time in a hot-wall reactor without causing the dusting and surface morphological degradation that occurs in cold-wall reactors. Kimoto et al. [109], for example, have improved on this approach and demonstrated very high-purity SiC growth employing this style of reactor. At 1550 °C and 80 Torr, reproducible epilayers with 50 um thickness and n-type background doping in the low $10^{-13}cm^3$ range were produced. Excellent thickness uniformity (1% standard deviation over mean value) and doping uniformity (6% standard deviation over mean value) have been achieved on 2 inch wafers utilizing a horizontal hot-wall reactor [109] with extra mechanical rotation.

5.6 Doping Incorporation strategy

Well-controlled dopant inclusion is required to achieve consistent and dependable SiC semiconductor device properties. Due to the low diffusion coefficient of SiC, unlike the doping technology often employed in the silicon semiconductor industry, it cannot be efficiently doped by diffusion at SiC growth temperature. Doping of a device structure's

SiC epitaxial layers is performed by either pouring a dopant source into the reactor during growth or by implanting the dopant atoms. The most prevalent n-type source for in situ doping is nitrogen. Because nitrogen's atomic size (0.74 Å) is closer to that of carbon (0.77 Å), nitrogen prefers to replace at C sites to a first approximation, which is compatible with the published experimental results [110]. As previously discussed, the bonding between Si and C atoms in neighboring bilayer planes can be either zincblende (cubic) or wurtzite (hexagonal). Because each form of bond creates a slightly different atomic environment, some lattice positions in polytypes are inequivalent. In 6H-SiC, three inequivalent sites are available (two cubic sites and one hexagonal site), whereas 4H-SiC has two inequivalent sites (one cubic site and one hexagonal site). When a dopant is integrated into distinct inequivalent sites, the ionization energy changes. In general, larger donor concentration epitaxial layers produce lower ionization energy due to Coulombic interactions with surrounding impurities [111]. Furthermore, it was discovered experimentally that the ionization energies of nitrogen in 4H-SiC are shallower than the comparable values in 6H-SiC. In situ nitrogen doping can be accomplished by injecting nitrogen or ammonia into the reactor during the growth process. Controlling net dopant incorporation by simply raising or reducing the flow of the dopant source, on the other hand, has limitations in terms of repeatability and doping range. For a nitrogen-doped n-type layer, this doping range is typically confined to $2 \times 10^{16} - 5 \times 10^{18}\ cm^{-3}$. If the nitrogen supply is increased further, either the growth rate or the surface morphology is found to decrease dramatically [112]. That lead to another method, called termed *site-competition growth*, which it's used to increase the doping concentration [113]. Nitrogen and carbon occupy the same sites in SiC, reducing C/Si produces more C vacancies in SiC, which increases nitrogen incorporation.

Another n-type dopant in SiC is phosphorus. However, phosphorous appears to have limited potential as a nitrogen substitute, given its bigger atomic size and similar ionization energy to the nitrogen donor [113]. The position of phosphorous in the SiC lattice as an independent impurity, phosphorous-related complexes, and corresponding electronic levels are still poorly understood. Hall measurements on phosphorous-implanted SiC epilayers revealed two ionization energies: $80 \pm 5\ meV$ and $110 \pm 5\ meV$ for 6H-SiC [114] and 53 and 93 meV for 4H-SiC [115], which were assigned to silicon's hexagonal and quasicubic sites, respectively.

Otherwise, aluminum is more used as a shallow acceptor dopant in SiC and can be insert during growth, or by implantation. Differently to nitrogen, the aluminum acceptor resides at the Si lattice sites. Boron is another acceptor dopant in SiC. During

epitaxial growth, a considerable amount of holepassivating hydrogen is simultaneously incorporated into the growing B-doped CVD epilayer. Postannealing at 1700 ◦C in Ar is usually used to dissociate B–H and better activate the B acceptors [113]. However, this does not mean that boron only substitutes at Si sites. Experiments have revealed that a trace quantity of boron can occupy C sites and form an energetically deep complex known as a D-center. The boron energy level at the Si site is around 300 meV, measured from the top of the valence band. The deeper core is roughly 600-700 meV above the valence band and manifests optically at low temperatures by forming donor-acceptor pair spectra [116].

5.7 Defects in bulk SiC

The following overview focuses on defects important to SiC bulk crystal formation and SiC wafer applications.

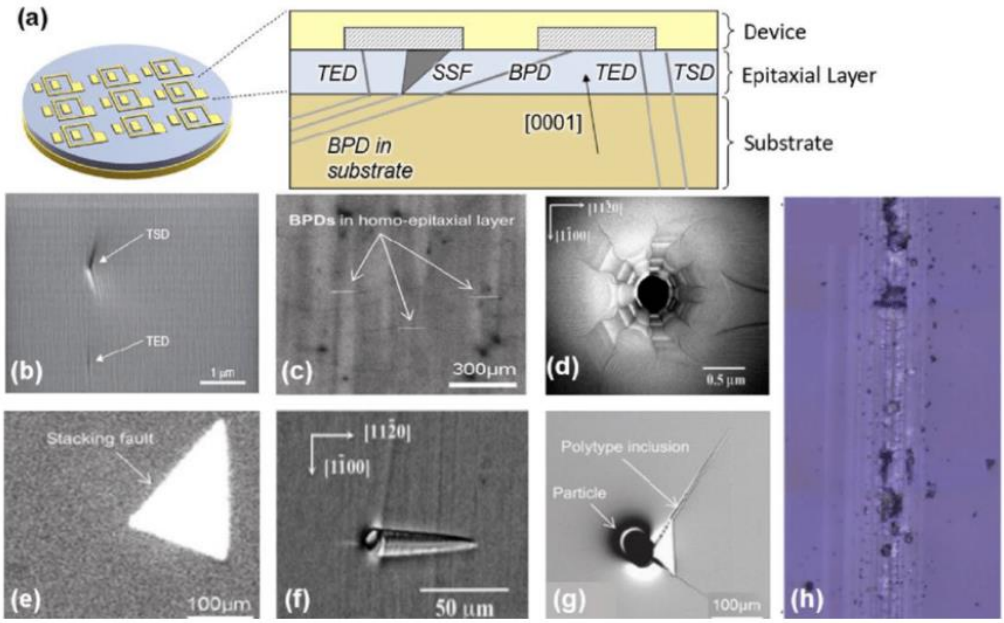


Fig. 5.7 a) device defectivity scheme b) TSD7TED c) BPDs d) dot e)Stacking fault f) comet g) particle contamination h) dislocations [180].

5.7.1 0D – point defects.

Carbon and silicon vacancies, interstitials, antisite defects, and defect complexes are examples of intrinsic point defects. Vacancies play a role in dislocation rise in the crystal during bulk development. Although controls over dislocation production and propagation are critical for SiC bulk development, little effort has been done to incorporate vacancies for fundamental knowledge of SiC dislocation dynamics.

However, in the case of the so-called HPSI material for radio frequency (RF) applications, native point defects play an essential role. It is thought that vacancy-related defects and defect complexes generate deep acceptor and donor levels, compensating for the residual, shallow dopants.

Unintentional doping by nitrogen (shallow donor), boron (shallow acceptor), and aluminum (shallow acceptor) as well as transition metals (typically deep electronic levels) alters the electronic characteristics of the semiconductor SiC in the event of extrinsic point defects. These contaminations are often caused by SiC source materials and graphite crucible components.

5.7.2 1D line defects

Dislocations in SiC are the primary cause of electronic device deterioration and failure. The threading edge (TED) and threading screw (TSD) dislocation lines in hexagonal SiC primarily proceed in the <0001> direction and cut the horizontal device structures vertically. Several authors have demonstrated that large densities of TSDs and TEDs change the device operation of Schottky-Diodes and Metal-Oxide-Field-Effect-Transistors (see, for example, reviews in (117) and (118)). Such phenomenon is common in device processing for any type of semiconductor material. Basal plane dislocations (BPD) are dislocation lines in the < 0001> plane showing a very specifically device failure mechanism in SiC. BPDs from the grown crystal should not normally be found in epitaxial layers grown on a <0001> 4H-SiC wafer. A number of BPDs from the SiC substrate penetrate into the thin film deposited on top due to the modest off-axis orientation of the substrates in the region of 4° up 8° in the <11-20> direction, which favors step flow growth during epitaxial growth. It was proven (119, 120) that BPDs cause quick bipolar device deterioration. The recombination energy created by a pn-junction during forward voltage operation may induce basal plane dislocations to divide into partial dislocations, forming a stacking fault in between. The latter is a source of heightened charge carrier recombination, which increases the device failure rate dramatically. Although basal plane dislocations can be transformed into other dislocation types throughout the epitaxial process, greatly reducing their density during bulk crystal formation is the optimum preparation.

KOH defect etching (121, 122) can be used to visualize dislocations by determining their density and lateral distribution in the SiC sample under examination (figure 5.8 a). The more complex X-ray topography characterization method can be used to analyze the nature of the propagation through the crystal.

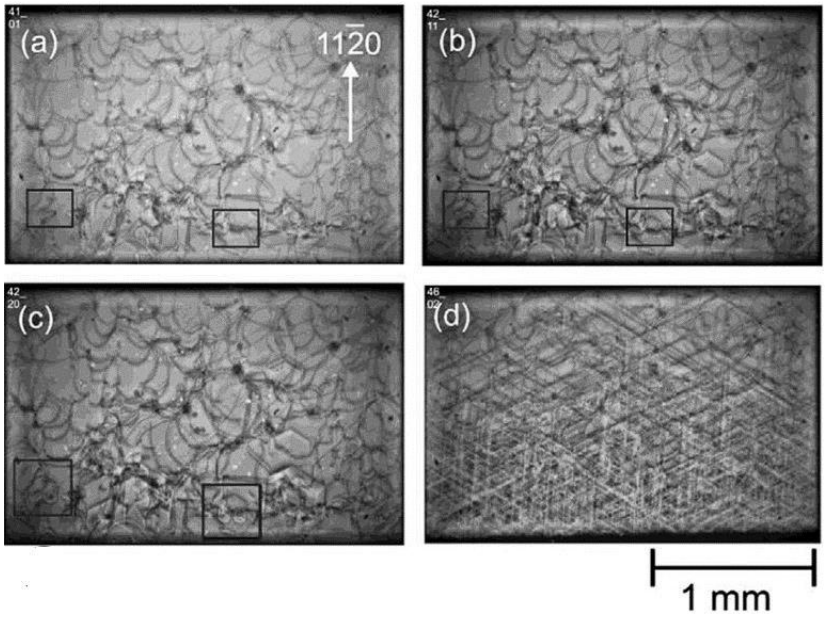


Fig. 5.8 Examples of SiC dislocations [181].

Thermo-elastic stress in the growing crystal as well as during the subsequent cooling down process has been identified as a major source of dislocation generation. As a result, it is critical to reduce the radial temperature gradient in the growth cell always maintaining a convex growth interface. Another kinetically driven issue is the relationship between growth rate and growth temperature. Dorozhkin et al. [123], for example, has reported that a high growth rate in the region of 500 μm to 1000 μm triggers dislocation development.

The most well-known SiC dislocation is the hollow core type known as micropipe (124), which has a huge burgers vector with a multitude of 3 to about 10 of the c-lattice parameters. Micropipes are screw dislocations that propagate primarily towards the <0001> direction; a minor deviation from the <0001> direction shows the nature of a mixed type of dislocation. Micropipes are either extensions of the SiC seed (figure 5.7(c)) or they begin as macroscopic defects such as polytype shifts, carbon inclusions (figure 5.7 (d)), silicon droplets (figure 5.7(e)), or they occur in association with voids (figure 5.7 (f)).

Most reports in literature agree that the elimination of unintentional polytype switches during seeding and throughout the growth process is the major effort to reach a zero micropipe density in the SiC boules by reduction of polytype switches during seeding & throughout the growth [125]. Near equilibrium growth during seeding is favorable for reduction of the micropipe density [171]. Using sublimation epitaxy, even micropipe

filling has been observed [126]. Micropipes that propagate into c-direction occur during growth on the c-plane. Hence, growth on surfaces tilted or even perpendicular to the c-plane is another option to diminish micropipes [127-129].

5.7.3 2D planar defects

Stacking faults (SFs) are the most visible two-dimensional flaws in SiC. Several causes of stacking faults during PVT development have been identified. Shockley stacking faults are formed when a full basal plane dislocation dissolves into partial dislocations [130]. A high nitrogen doping level above $10^{-19}cm^3$ causes ingrown stacking defects in the SiC boule [131] during crystal development. Their origin may be related to the Shockley fault generation mechanism, or they may simply emerge as a form of thin polytype instability on a terrace of the growth surface due to the low stacking fault energy in SiC. Frank type defects have also been observed in CVD, most likely as a result of overgrowth from threading screw dislocations whose spiral steps were divided on the surface into parts smaller than the unit cell in the c-direction [132]. Several studies have reported dislocation transformation at the growth interface in epitaxial growth. The line energy in newly developed crystal layers acts as a kind of selection rule for which direction a dislocation line will propagate further (for a foundational survey, see [133]).

5.7.4 3D volume defects

The finding of unintended polytype switches during PVT development on <0001> and slightly off-axis tilted seeds is closely related to the production and occurrence of stacking faults in SiC polytype switches. Polytype alterations in nitrogen doped SiC are defined by differences in visible light absorption. In the longitudinal cut (figure 5.7 (b)) made perpendicular to the <0001> seed orientation, 4H-SiC appears brownish, while green and yellow colors represent 6H-SiC and 15R-SiC polytype inclusions, respectively. The low stacking fault energy in SiC [135] is commonly referred to as the physical origin of polytype switching. Polytype variations during PVT development of SiC at extreme temperatures are technologically related to unstable or incorrectly designed growth conditions. The most important parameters are the gas phase composition (high C/Si rate favors 4H-SiC), the temperature, specifically the temperature gradient and related supersaturation (higher supersaturation favors 4H-SiC versus 6H-SiC), the type of doping (nitrogen stabilizes 4H-SiC), and the seed polarity (4H grows primarily on the <0001> surface). To put it another way, polytype flips frequently initiate at the edge of a <0001> growth facet. A smooth step flow development mode outside the facetted area or a spiral

growth mode inside the facetted area, in general, likely to reduce inadvertent polytype switching. Large growth terraces are problematic because they accumulate in the case of strong step bunching. The transition zone from the facet to the slanted growth interface outside of the terrace is a crucial region for increased step bunching and, as a result, unintended polytype flips.

Carbon inclusions (figure 5.6 (d)) have already been observed in numerous SiC growth labs. Carbon particles originating from the SiC source/powder and released due to the Si-rich gas phase composition are two significant sources. The particles are transported to the growth interface by an upstream flow in the PVT cell's gas room. [136] confirmed this model by using the M-PVT growth method, in which the gas feeding stream pushed out C-dust from the center crystal area. In contrast, Rost [137] linked the genesis of the carbon particles to a significant local increase in carbon content in the gas room, which may be induced, for example, by silicon loss.

Several papers have previously detailed the finding of Si inclusions (droplets) (figure 5.7 (e)) in SiC. In addition of the carbon inclusion, the Si droplet forms at the growth contact. Its cause is a low C/Si ratio in the gas phase. When a dense graphite material is utilized as the crucible material, a Si-rich gas phase may form primarily if a non-stoichiometric, i.e., Si-rich SiC source material is used.

Poor seed mounting results in the creation and migration of a void several micrometers in size through the SiC seed and farther into the growing SiC boule. The temperature gradient caused by a local sublimation-recrystallization process inside the hollow core directs its movement.

5.7.5 Dislocations in the crystal

The critical resolved shear stress σ_{CRS} in SiC is around 1 MPa [138], although normal resolved shear stress values in the growth cell readily surpass 10 MPa. As a result, thermally induced stress is regarded as the primary source of dislocation production during SiC PVT development.

The basal plane is frequently believed to be the principal slip plane when estimating the produced dislocation density. The shear stress component rz is causing dislocation motion in this situation. The density of dislocations in the crystal is proportional to the value |rz - CRS| [139]. The so-called van Mises stress, which also takes non-basal-plane components into account, is another signal for the effect of thermally induced strain on the ensuing dislocation density:

Eq.5.7

$$\sigma_m = \sqrt{0.5}\left[(\sigma_{zz} - \sigma_\pi)^2 + \left(\sigma_{zz} - \sigma_{\varphi\varphi}\right)^2 + (\sigma_\pi - \sigma_\pi)^2 + 12\sigma_{rz}^2\right]^{1/2}$$

Gao et al. [122], who used the Alexander-Haasen theory, took a more sophisticated way to determining dislocation density using thermos-elastic stress data. Gao et al. [140] continue to emphasize the basal plane as the primary slip plane in hexagonal SiC. Guo et al. [141] have highlighted the importance of prismatic planes for dislocation gliding in hexagonal SiC, emphasizing the need to take non-basal planes into account.

5.6 Wafer level annealing

To produce a device semiconductor, it needs to grow a 4H-SiC epitaxial layer (of certain thickness and doping) on a degenerate doped 4H-SiC substrate. The epitaxial growth requires high temperature treatments. Furthermore, for some applications the devices could be exposed to high temperature processes. In this context the thermal stability of 4H-SiC is a critical aspect. In the past it has been observed that treatments at temperature of about 2000°C induce the sublimation of Si and the growth of graphene layer on top of SiC in different atmospheres or in vacuum [142-144]. This proves the vulnerability of the material.

So, process optimization mainly sees two problems in WLA: crystallographic defects and the generation of graphite/graphene layers between the substrate and epitaxy.

The WLA technique is absolutely effective in reducing crystallographic defects, but on the other hand it generates an unwanted process consisting of a random graphitization on the surface of the substrate. This causes anomaly in terms of both doping and thickness of the subsequent layer and clearly an epitaxy with out-of-control parameters. In addition to the in-situ verification and successive results, which will be given later, it has emerged from the history of art that a method has recently been proposed that allows the growth of graphene on silicon carbide substrates with a high level of purity. We are therefore in a situation where the WLA technique undoubtedly has advantages but is also part of a process that can be and is used to produce graphene-based devices.

A commercial SiC wafer is annealed at high temperatures (at least 1200 °C, but frequently higher) in this procedure. At these temperatures, the Si atoms preferentially evaporate away from the substrate, leaving a C-rich surface behind. At high temperatures, this C-

rich surface can rebuild to create a sp2-bonded epitaxial graphene layer. Imperfections and flaws on the substrate surface, such as polishing scratches and screw dislocations, can cause an increase in silicon evaporation rate during an annealing process, resulting in uneven graphene development. It was shown that annealing at temperatures below the graphitization temperature in argon atmospheres can yield an atomically terraced silicon carbide surface free of polishing scratches and dislocations. These substrates can be graphitized simply by raising the annealing temperature above the point at which graphitization begins.

The implementation of this process after substrate growth take place in similar conditions. Aiming to clarify the critical features of thermal treatments for applications in this work we have evaluated the stability of 4H-SiC in a low temperature range below 2000°C monitoring the wafer surface homogeneity by micro-Raman spectroscopy, Atomic Force Microscopy (AFM) and Electrostatic Force Microscopy (EFM).

5.6.1 Qualification process flow and results

The implementation of the Wafer Level Annealing (WLA) technique initially took place at an elevated temperature of 1600 degrees Celsius. This high-temperature annealing process served a crucial purpose in reducing basal plane dislocations, a critical step in semiconductor manufacturing. With WLA, basal plane dislocations can be "transform" into defects with a "*low killer rate*", meaning they have the potential to less impact device performance and higher yield.

By subjecting wafers to the rigorous annealing process at 1600 degrees Celsius, the semiconductor industry effectively mitigated the formation of basal plane dislocations, thereby enhancing the overall quality and reliability of the final semiconductor devices. This temperature was carefully chosen for its ability to optimize the reduction of dislocations while considering the material properties and constraints.

However, it's important to note that, despite the benefits of the annealing process, certain challenges persisted. One of these challenges relates to the observation of electric anomalies located near to the active area of devices, such as diodes and MOSFETs. These

anomalies prompted further investigation and optimization efforts to ensure consistent device performance and reliability.

Reducing the temperature from its original value of 1600 degrees Celsius down to a significantly lower temperature of 1150 degrees Celsius. Tests were also carried out on the reduction from 1600 C to 1350 C, but the results obtained highlight anomalies in terms of doping hence the pristine lower temperature of 1150°C seems more suitable. This adjustment is implemented with the explicit objective of enhancing the robustness of each individual step involved, thereby extending the overall process qualification to encompass all equipment components operating within the production line. The significance of this temperature reduction becomes even more apparent when we consider that it falls below the fusion temperature of silicon.

One of the primary advantages of operating at this reduced temperature is the mitigation of potential surface damage arising from the presence of oxygen (O_2) and water vapor (H_2O). Silicon is inherently susceptible to oxidation when exposed to oxygen and moisture at elevated temperatures. By maintaining the process at 1150 degrees Celsius, we effectively create an environment that minimizes the risk of surface damage, thus preserving the integrity of the materials and equipment involved.

Furthermore, this carefully controlled reduction in temperature has a notable impact on the distribution of resistivity within the wafer during the growth of the EPI (epitaxial) layer. The result is a more tightly constrained and uniform distribution of resistivity throughout the wafer. This improved uniformity translates into a tangible reduction in defectivity, a critical metric in semiconductor manufacturing. The enhancement in defectivity is not only advantageous from a quality control perspective but also offers potential cost savings by minimizing the need for rework and reducing the yield loss associated with defective wafers.

An additional noteworthy effect of this temperature adjustment is its ability to curtail the phenomenon of surface graphitization. Surface graphitization involves the transformation of silicon into graphite or graphene-like structures when subjected to high temperatures. By maintaining a lower temperature throughout the process, the likelihood of surface graphitization is substantially diminished. This, in turn, contributes to the preservation of the intended properties and characteristics of the semiconductor materials.

So, the decision to reduce the operating temperature from 1600 degrees Celsius to the more manageable 1150 degrees Celsius holds a multitude of benefits for the semiconductor production process. It not only safeguards against surface damage induced by oxygen and moisture but also optimizes the resistivity distribution within the wafer, leading to a reduction in defectivity. Additionally, it plays a crucial role in preventing surface graphitization, ensuring the integrity of the materials utilized in semiconductor manufacturing. Through this strategic temperature adjustment, the production line achieves greater robustness and enhanced process qualification, ultimately contributing to the production of high-quality semiconductor devices.

Summarizing:

- relieves stress caused by the aggressive mechanical process steps.
- converts up to 70% of the BPD's to device-benign TED's and reduces the overall defect density of the wafer

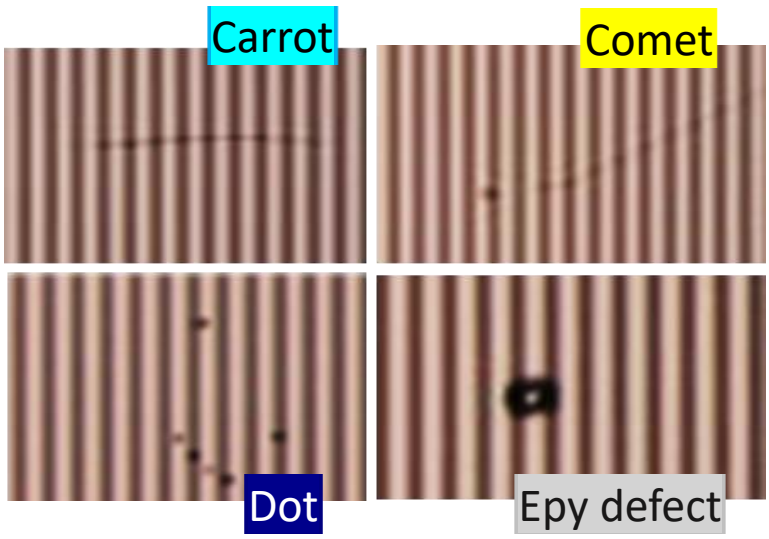


Fig.5.9Inspection at substrate/epitaxy level with CANDELA 8520 by KLA-Tencorscan which allowed to detect surface defects such as droplet, carrots, triangles, micropits, etc.) and doping profile of trial wafers.

CANDELA is an instrument based on photoluminescence (PL), which is one of the most common techniques for characterizing materials. The incident photons are absorbed by the sample which will subsequently release others at characteristic energies of the material studied according to the selection rules dictated by quantum mechanics. The

lifetime of excited electrons depends on the quality of the material, and time-resolved PL allows the study of radiative and non-radiative recombination processes. Typical information extracted from PL is gap energy, quantum confinement and crystal purity. CANDELA analysis was evaluated for wafers with and without WLA process and before and after epitaxy.

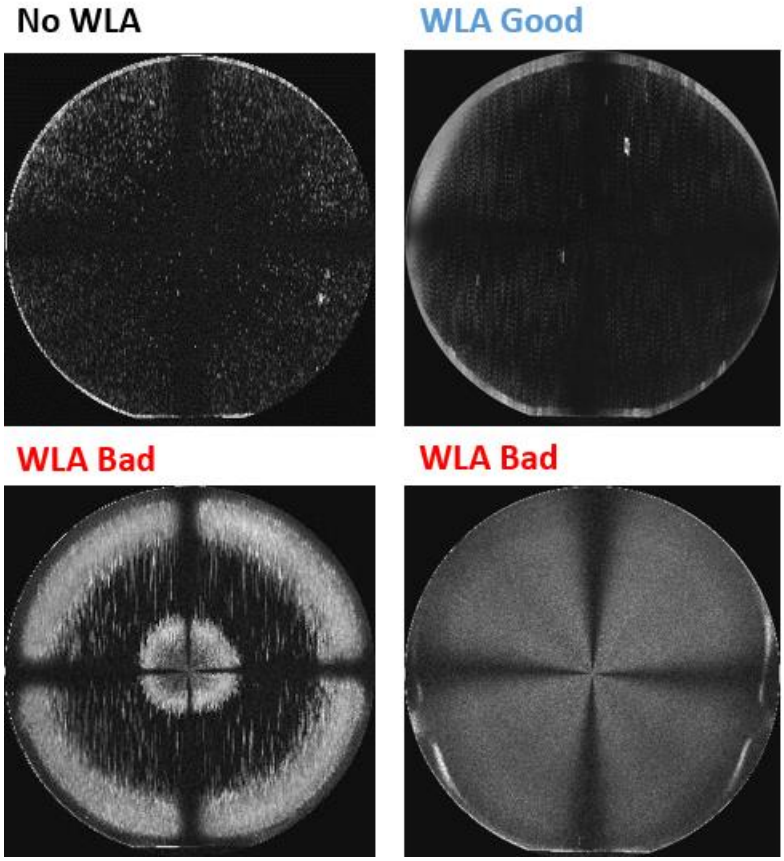


Fig. 5.10 CANDELA (photoluminescence) measurement on wafers processed with and without WLA

Doping profile is correlated to the surface roughness and it's quite difficult be controlled. The machine parameters also highlight a doping distribution which is altered when the surface is anomalous. For this reason, the problem was investigated using AFM and Raman techniques.

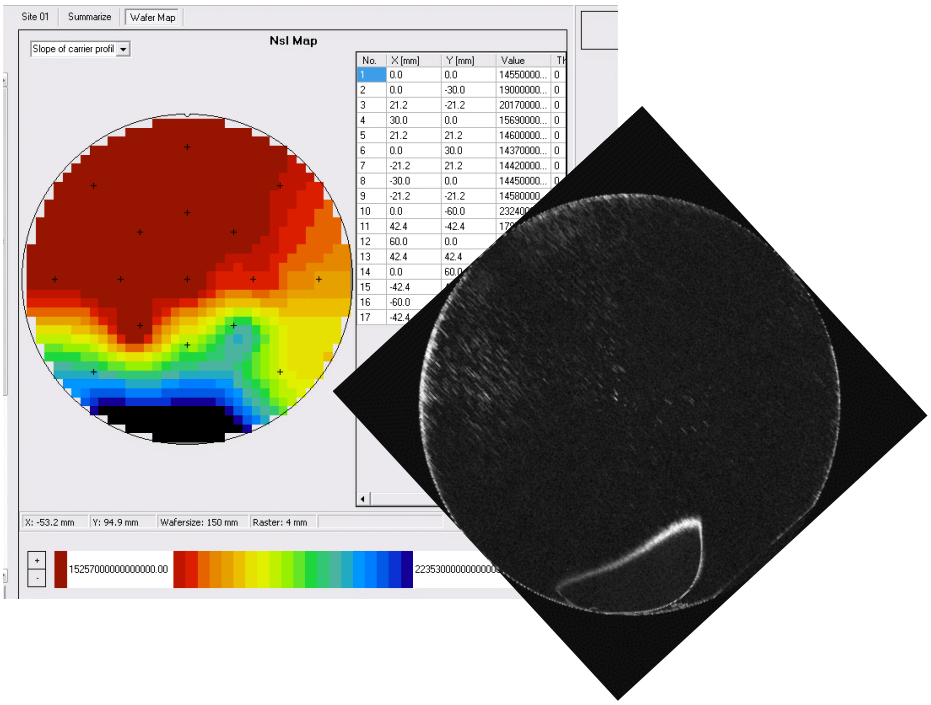


Fig. 5.11 Doping profile compared to Candela map

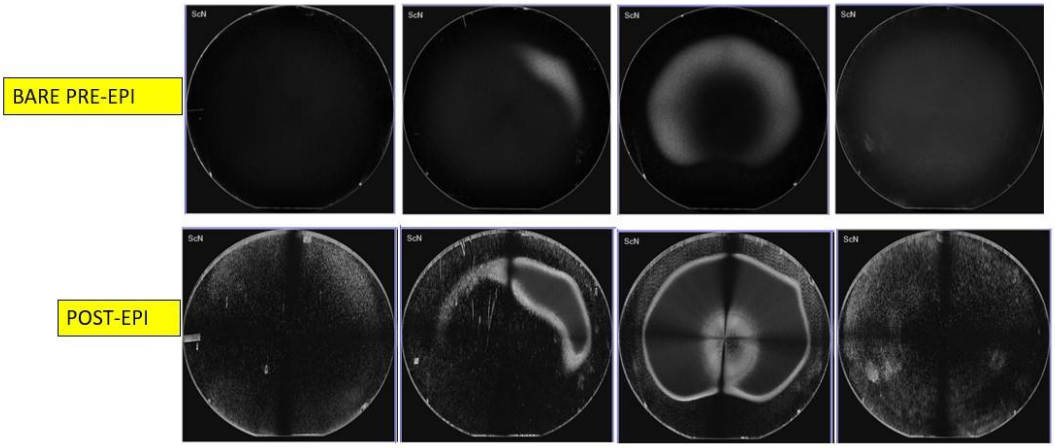


Fig. 5.12 Wafer shape after epi growth due to anomalus doping

The AFM analysis was performed on the wafers most populated by defects. The results highlight a surface populated by unusual terraces compared to the normal SiC surface: the surface, following random graphitization, generates a non-homogeneous and contaminated surface.

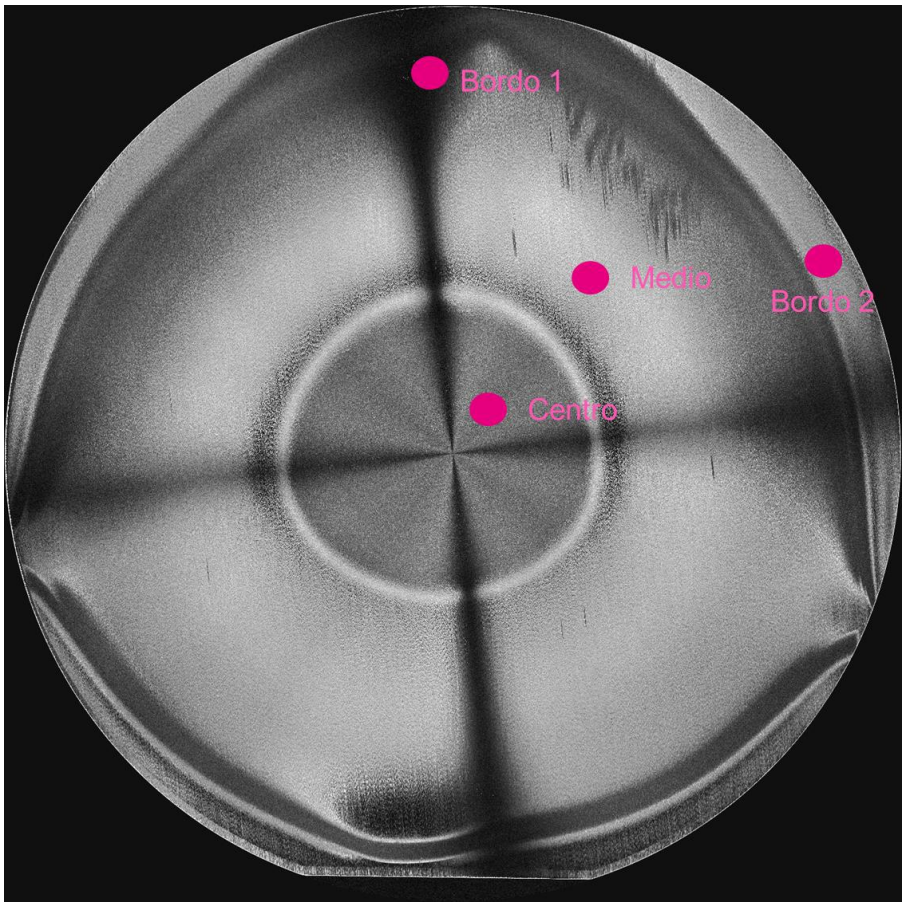


Fig. 5.13 Wafer with anomalous doping profile in which we perform AFM (measures in pink points)

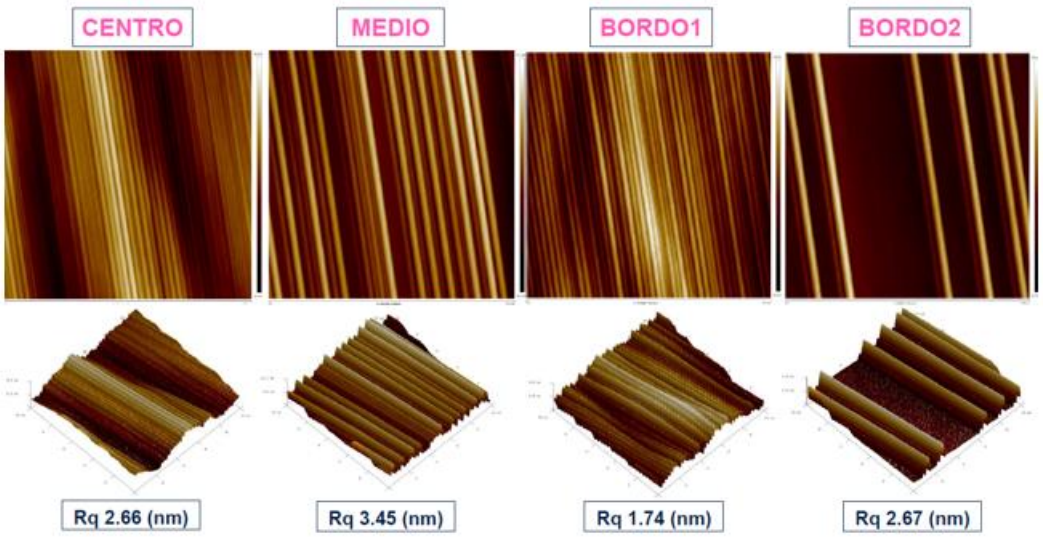
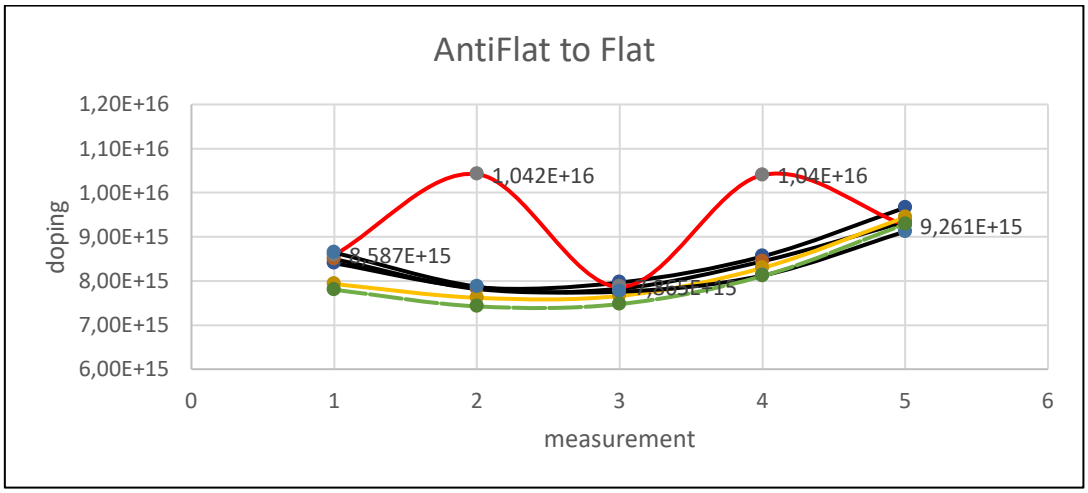


Fig. 5.14 AFM on points in Fig. 5.11

The outlayer points in fig. 5.15, are the ones in which grafitization growth are absoluty out of specific.



Slot	1	2	3	4	5	Mean	Max	Min	Delta
1	8.40E+15	7.85E+15	7.96E+15	8.56E+15	9.66E+15	8.487E+15	9.66E+15	7.85E+15	21.4%
2	8.50E+15	7.82E+15	7.83E+15	8.45E+15	9.34E+15	8.385E+15	9.34E+15	7.82E+15	18.2%
3	8.59E+15	1.04E+16	7.87E+15	1.04E+16	9.26E+15	9.307E+15	1.04E+16	7.87E+15	27.5%
4	7.93E+15	7.62E+15	7.66E+15	8.30E+15	9.44E+15	8.190E+15	9.44E+15	7.62E+15	22.3%
5	8.64E+15	7.87E+15	7.76E+15	8.12E+15	9.12E+15	8.302E+15	9.12E+15	7.76E+15	16.4%
19	7.80E+15	7.42E+15	7.48E+15	8.11E+15	9.29E+15	8.020E+15	9.29E+15	7.42E+15	23.3%

Fig. 5.15 Doping vs measurement – Out of spec points in halo in Fig. 5.13

Following this evidence, we proceeded by characterizing the surface of the wafers using micro-Raman spectroscopy and EFM (Electrostatic Force Microscopy). Micro-Raman spectroscopy measurements were conducted all over the wafers surface to get information about the crystal structure and the electronic features. We used a Horiba HR-Evolution Micro-Raman system with a confocal microscope (100x) and a laser excitation wavelength of 633 nm. The laser power was filtered with a neutral density (ND) filter at 50%. A grating of 600 lines/mm was used to acquire Raman spectra. All the spectra were calibrated with respect to the Si peak at 520.7 cm^{-1}. AFM and EFM measurements were performed using a NT-MDT stand alone SMENA Scanning Probe Microscope working in semi contact mode and equipped with a platinum coated probe.

In Fig. 5.17 micro-Raman spectra acquired in different radial positions of the wafer A after the thermal treatment at the highest temperature are reported. Going from the center to the edge of the wafer the corresponding spectrum is reported in green, black, pink and red color. The spectra evidence the typical bands of 4H-SiC together with specific shape changes going from the center to the edges of the wafer. It is evident that the wafer A surface is not homogeneous, conversely the surface of wafer B is homogeneous. To

highlight the differences of the spectra, Fig. 18 reports the same spectra of the wafer A already shown in Fig.1, after the subtraction of the reference Raman spectrum of the same kind of substrate of 4H-SiC not treated. In particular, the green spectrum is collected in the center of the wafer A, the absence of signals indicates that this area is made of high quality not modified 4H-SiC. The black color spectrum is the most common all over the wafer surface. In this case, a broad band is clearly detected around 1300 cm^{-1} as well as another band near 1580 cm^{-1}. The pink color spectrum is always recorded at 1 cm from the edges of the wafer. In this region it is evident a shift of the bands toward higher Raman shifts values with respect to the most common spectrum (black line). Another band around 2700 cm^{-1} is hardly detected in this sample's region for magnification motifs. Lastly, the red color spectrum is collected along the edges of the wafer. In this case the band around 2700 cm^{-1} is quite evident. Furthermore, the high intensity and sharp bands at lower Raman shift are at 1350 cm^{-1} and 1600 cm^{-1}. It is interesting to note that the red spectra match with the Raman spectra of damaged graphene whereas the other spectra resemble those of amorphous carbon [5-6].

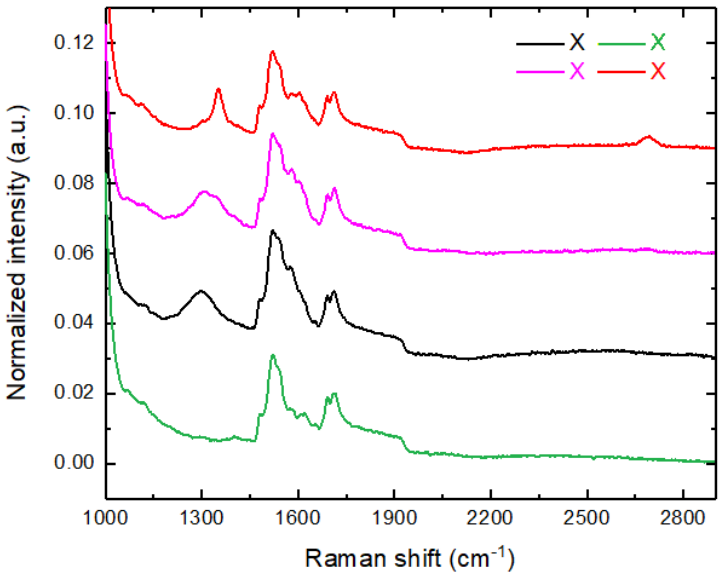


Fig. 5.17 Raman spectra of Wafer A in different radial positions after thermal treatment at the highest temperature.

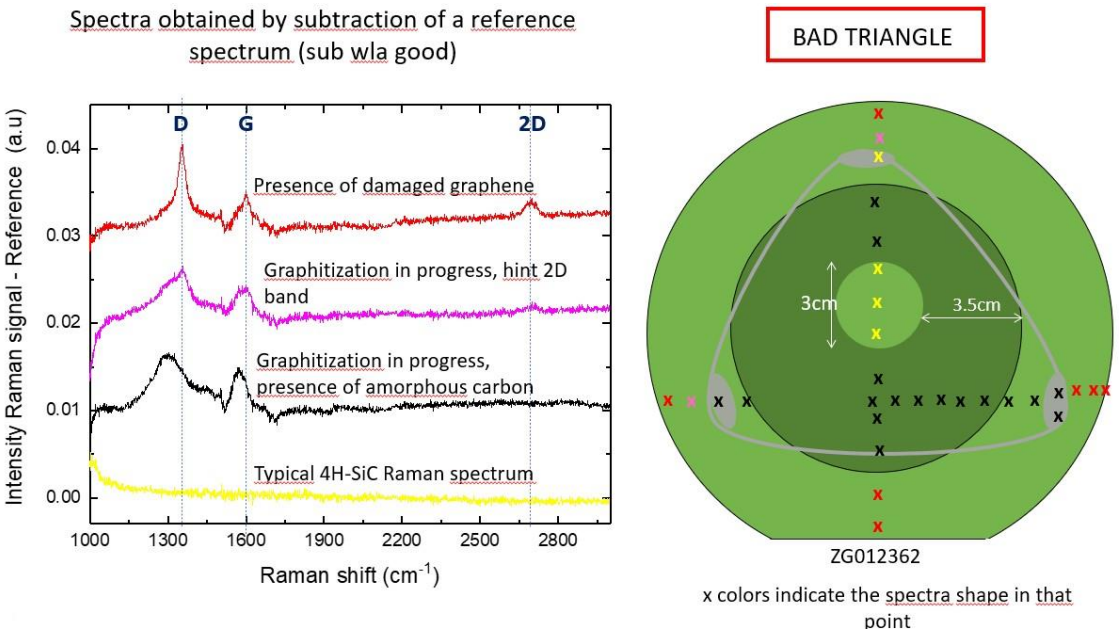


Fig. 5.18 Raman spectra after the subtraction of the reference spectrum of 4H-SiC.

In order to confirm the graphitization, more accurate Raman measurements were performed on wafers coming from WLA process at different temperature (1600°C, 1350°C, 1150 °C) and processed on different equipments (just the results about 1150 °C are reported, which is the qualified process).

The wafer were cut in 2 cm^2 pieces by using a diamond pen and for each piece 3 Raman measurement were performed. Each measure was performed using two wavelengths in order to evaluate all the spectra, since graphite and graphene has Raman peaks at about 1300 cm^{-1} and 2700cm^{-1}, as previous said.

Right after the Raman set-up configuration:

- Laser wavelenght: 532 nm
- Exposure time: 180 s
- $\lambda = 580\ nm\ - 615\ nm$

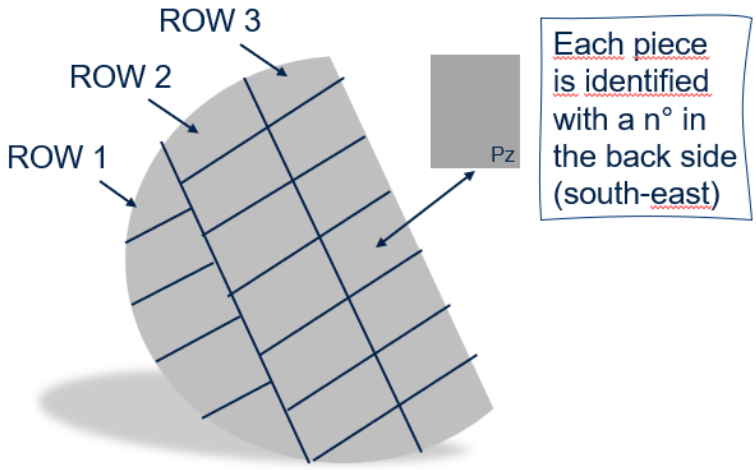


Fig. 5.19 Wafer cutted in order to perform Raman measurements

Since the number of SiC wafer pieces are quite large, just some 1150 °C of the Raman spectra are reported.

For the first equipment:

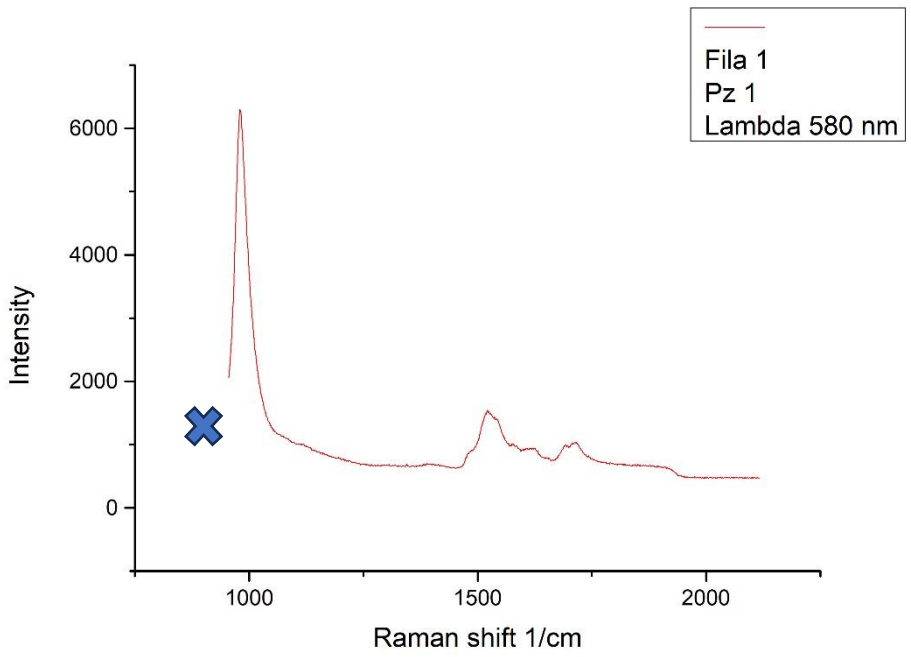


Fig. 5.20 No graphitization at 1300 cm^{-1}

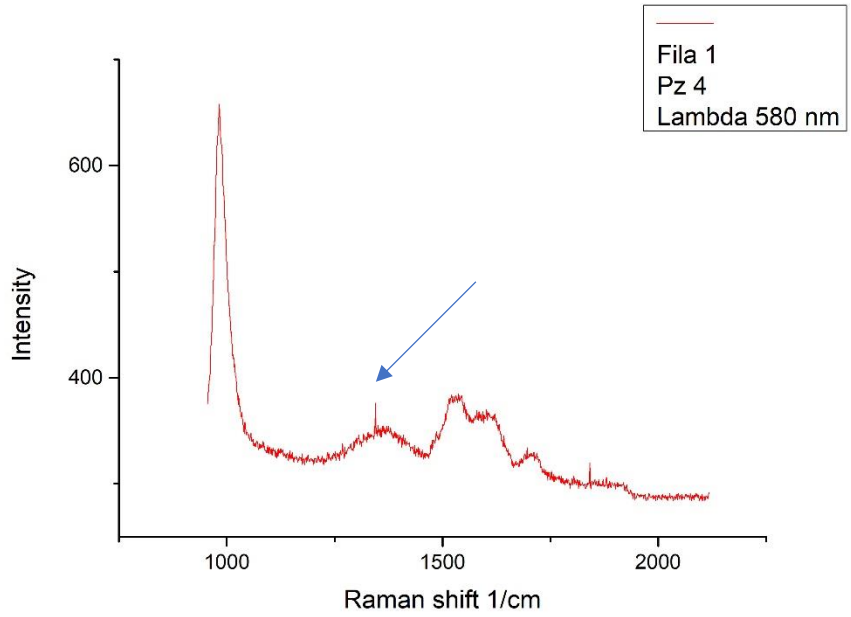


Fig. 5.21 Presence of graphitization at 1300 cm^{-1}

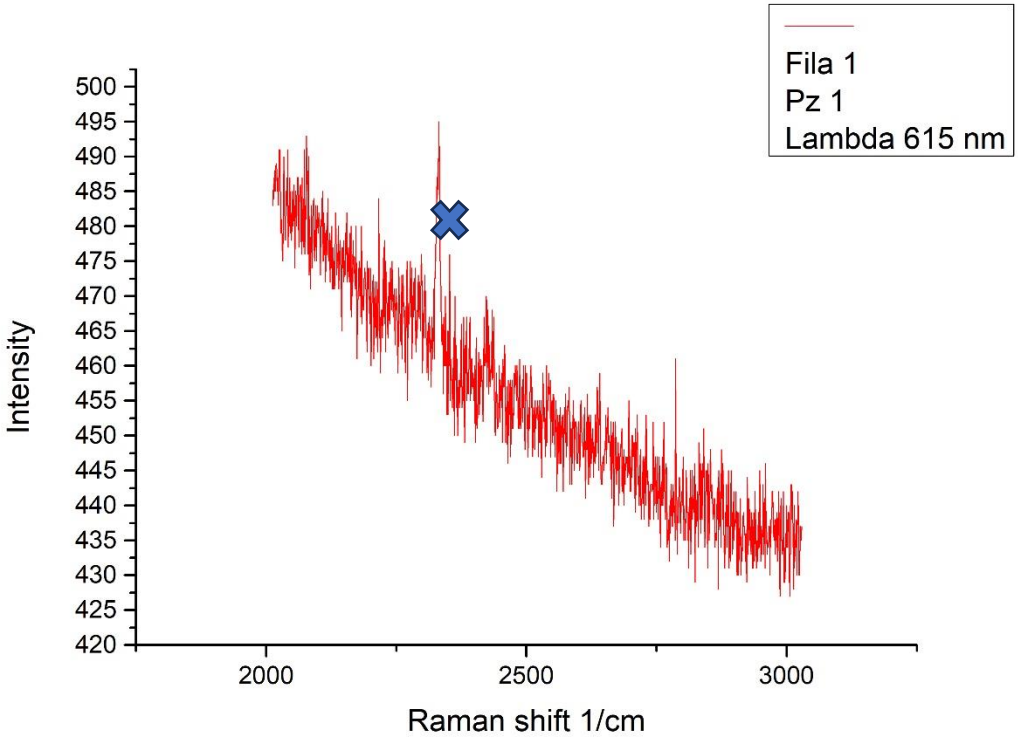


Fig. 5.22 No graphitization at 2700 cm^{-1}

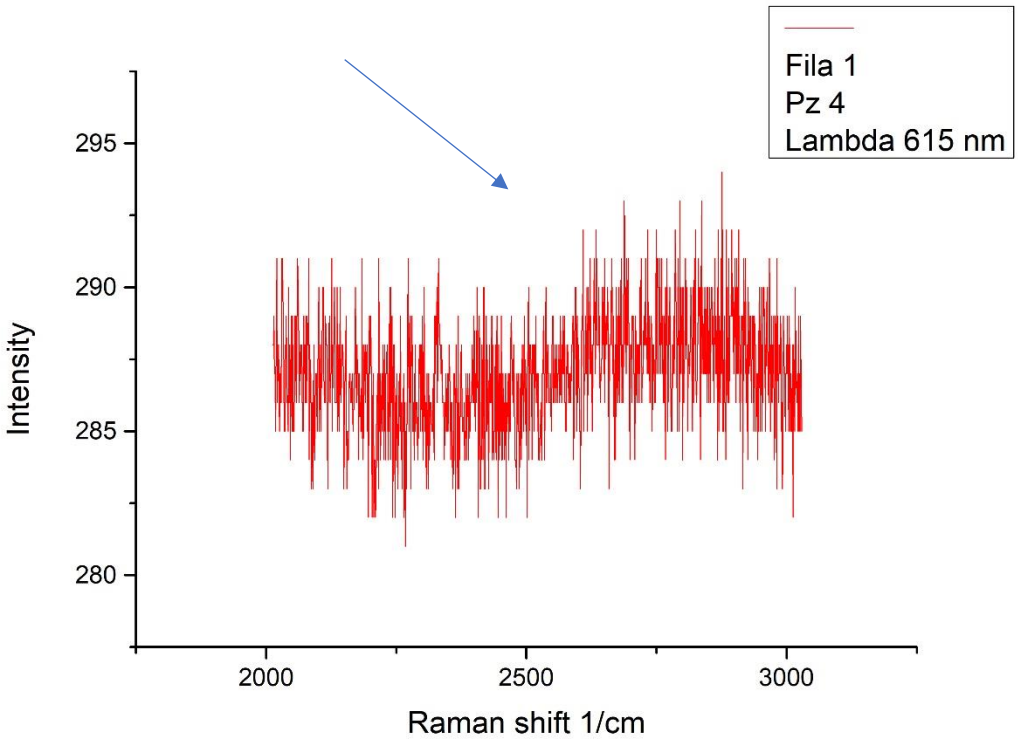


Fig. 5.23 Presence of graphitization at 2700 cm^{-1}

For the other equipment:

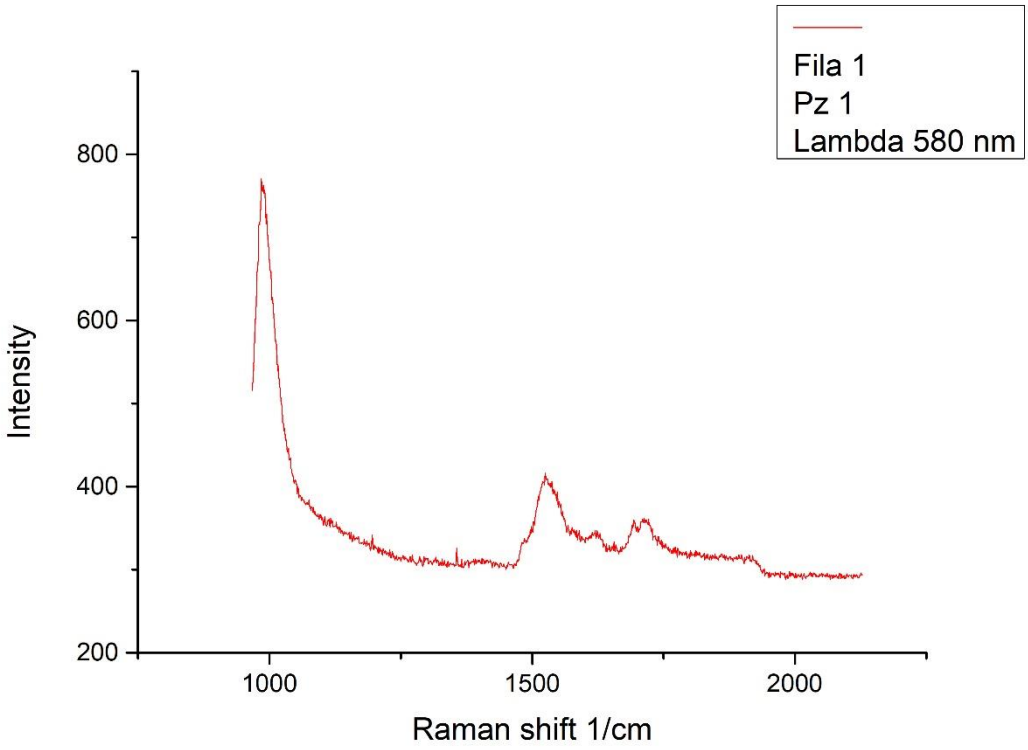


Fig. 5.24 No graphitization at 1300 cm^{-1}

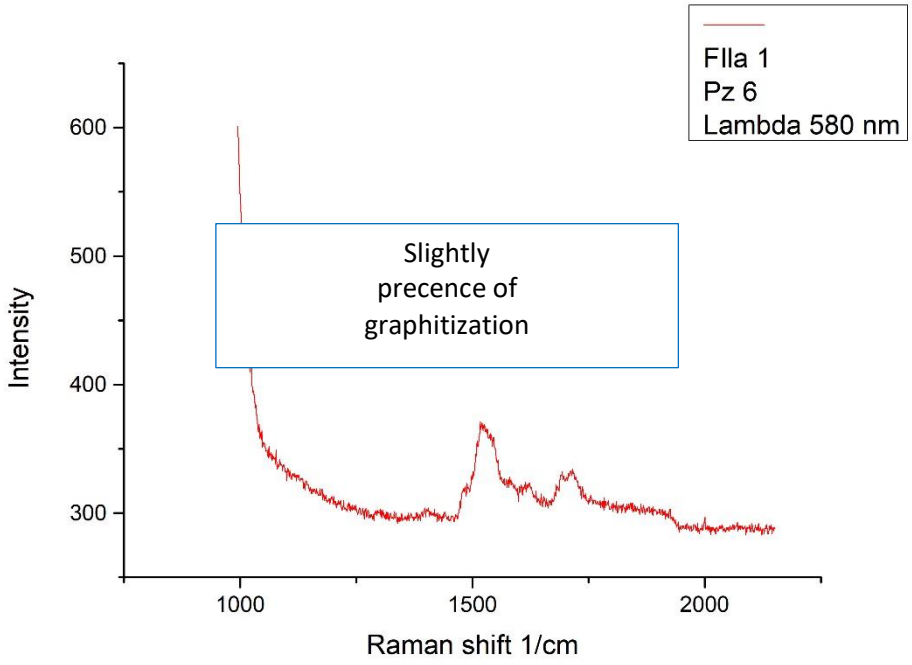


Fig. 5.25 No graphitization at 1300 cm^{-1}

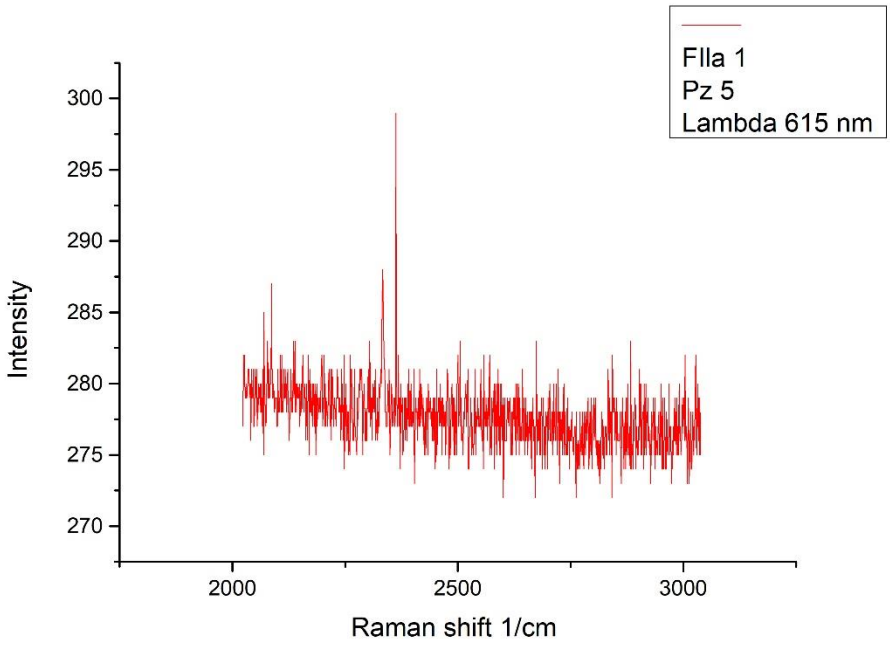


Fig. 5.26 No graphitization at 2800 cm^{-1}

The wafers processed on equipment 1 shows traces of graphitization across the entire wafer, especially at the wafer edge. No trace in the two wafers processed on equipment 2.

Wafers processed at temperatures of 1600 °C and 1350 °C exhibit greater graphitization compared to the process at 1150 °C (qualified process). It is clear that small differences inside the oven can modify the surface of the slice, generating graphitization. The two equipments are twins tool but it is clear that the graphitization depends not only on the process but also on any C contaminants inside the chamber (whose walls are made of SiC, and the thermal processes can lead to a splitting of the covalent bonds of the SiC , contaminating the slices with carbon). So, it's absolutely necessary to increase maintenance and add a cleaning at least every two day.

5.7 Conclusions

In this work we have studied the thermal stability at low temperature of 4H-SiC substrates. We detected effects of graphitization on two substrates of 4H-SiC after a thermal treatment in Ar atmosphere at temperature lower than 2000°C by micro-Raman spectroscopy. Traces of damaged graphene have been evidenced on the edges of one of the wafers featuring graphitization and large radial inhomogeneity. In conclusion we can highlight two points:

1. WLA must be used with temperature lower than 1200 °C or the covalent bond in SiC can be broken; the Si particles evaporate and C particles generate graphitization .

   Twin equipments show different results. This means that graphitization is random at temperature below 1200 °C and possible C contamination due the equipment must be avoid raising the number of maintenance interventions.

Chapter 6

Thermal behavior of a 7kW interleaved module for automobile fast charging

The pursuit of electrification in the automotive market is becoming increasingly important to address stricter limits on CO_2 emissions and the growing energy consumption.

New power semiconductor devices based on Si and SiC allow a higher amount of power flow, necessitating proper thermal dissipation techniques. Using the finite-element-based COMSOL Multiphysics, we developed a thermal simulation of a revolutionary scalable On-Board Charger (OBC) capable of performing a power flow of 7 kW.

The study describes in full the OBC modular approach, as well as the simulated active devices, which are Si- and SiC-based MOSFETs, SiC Schottky diodes, and thyristors. Appropriate power losses for the semiconductor devices used in the OBC are determined and used in simulation setup to evaluate the realistic maximum temperature at full load during operative state. In addition, a parametric investigation is performed in the simulation by sweeping over the convective heat transfer coefficient values. The implementation of numerical analysis is well discussed. The maximum device temperature of the OBC module during application conditions is estimated in this study.

6.1 Introduction

As a result of environmental concerns, electric vehicles (EVs) have grown in appeal in recent years. Power electronics-related systems are a crucial subject in the automotive framework, particularly for plug-in full and hybrid vehicles, in terms of power converters and power semiconductor devices contained within them, as well as traction, charging, and auxiliary designs inside the car [145-147].

This rapid expansion is undoubtedly owing to new power semiconductor technologies that make use of wide band-gap materials like silicon carbide (SiC) and gallium nitride (GaN). They can enable greater efficiency and power density from both the device and

topology perspectives [148-149]. There are also innovative silicon (Si)-based devices for both high voltage and low voltage frameworks that can be employed in automobile applications. For example, Si MOSFETs are frequently employed in resonant converters [150].

Traditionally, the automobile industry classifies electric vehicles based on their electrical power consumption. MHEVs (Mild Hybrid Electric Vehicles) have a traditional internal combustion engine (ICE) with a parallel generator that takes over while the vehicle is in neutral, coasting, or braking. Hybrid electric vehicles (HEVs) are already relatively prevalent and drive the automobile using an inverter powered by a battery pack.

When the ICE is triggered, the battery is charged using a particular approach such as the Kinetic Energy Recovery System (KERS). PHEVs (Plug-in Hybrid electric vehicles) are similar to HEVs in that the battery can be charged directly by connecting to the electrical grid. The power transmission between the battery and the grid was handled by the on-board charger. Battery electric vehicles (BEVs) do not have a combustion engine [151-152].

Battery reliability and charging are two of the most critical topics in plug-in EVs, both for the car and for the integrated grid infrastructure that will be required to meet the needs of all vehicles once they are widely distributed. The key problems in this study area will be integration with the smart grid, distributed generation, including renewable energy sources such as photovoltaics, wind, and storage systems [7]. Charging can take place both on and off-board. Table 6.1 lists the advantages and issues of both solutions. Furthermore, so-called “integrated on-board chargers” are being developed, which take into account the existing motors or converters within the electric vehicle, although they appear not to be sufficiently technologically robust compared to other options [153]

Chargers	Advantages and key challanges
On board charger	*Size and weight restrictions caused by EVs design*
	Less energy transfer
	Charge at low-power levels
	Recharge at any electrical outlet
	On board rectification is needed to manage BMS
Off Board charger	*Less weight*
	Fast charging
	Higher energy transfer
	Recharge only in wall box
	Power output limitations
	Better and less complex BMS systems
	Improvement of contractual chances for companies
	No identification of malfunctioning of battery pack cells

TABLE. 6.1 Differences between ON and OFF Board Chargers

Innovative battery technologies, particularly lithium-ion-based ones, are encouraging the development of innovative automobile solutions. Although there are many different types of batteries available today, and they all need to be improved, the type mentioned above is now the most commonly used in EVs [145].

On-board chargers (OBCs) can be unidirectional or bidirectional, with the latter allowing for power exchange from vehicle to grid [155]. There are many modulation schemes and control modes for OBCs, all with the same goal in mind: to increase converter efficiency. DC fast charging facilities are available as off-board solutions [154]. The converter for charging the batteries is located off-board and at the stations in this structure. There are various AC and DC charging modes [145-156]. Wireless power transmission based on induction law is another charging technology under development [157]. It would reduce the amount of time required to charge the battery and increase the system's safety and reliability; nevertheless, in comparison to wired modes, this option is still in its infancy.

In relation to this power transfer mechanism, vehicle–to–vehicle recharging has been proposed, in which two cars can swap power, one from the other, during a journey. Fast charging can be obtained also with AC–based OBC topologies. The considered architectures can be either single–phase or three–phase. Among the possible converter types, there are: conventional, interleaved, or phase shifted semi–bridgeless boosts, but also bridgeless interleaved topologies, also in resonant version.

[158] and [159] provide a complete analysis of the different topologies for off-, on-board, and integrated chargers using Si, SiC, or GaN devices. To prevent electromagnetic interference, a filter is typically installed in the system before to the power factor corrector (PFC) stage. The topology of all the system that has an AC input require an AC-DC converter. The converter under consideration in this work, which will be briefly detailed below. It has a very flexible input voltage amplitude that ranges between 85-265 V and a voltage frequency of 45-65 Hz.

The OBC first stage is a PFC interleaved totem pole, made up with SiC power semiconductor devices in the power stage. The high–voltage SiC devices are housed in a surface–mounted package (STM). Switching frequency is set to 70 kHz. Synchronous rectification is employed to improve the power efficiency, enabled according to load conditions. The other stage, downstream from the PFC, is the DC–DC converter. Usually, it is an LLC converter with a resonant tank, when on the primary side power semiconductor devices are employed. In this work, the placed devices are silicon–based, in MDmesh technology.

The LLC is a full-bridge interleaved with a configurable switching frequency ranging from 80 to 310 kHz. For a 375 V-rated primary battery, the DC voltage amplitude is in the 250-450 V range. Furthermore, a battery management system is typically installed in order to assess the system's proper operation. Finally, the traction inverter feeds the electrical motor, which is typically a permanent magnet synchronous one [145]. The total power delivered by the simulated system in this article is 7 kW.

Thermal control of power devices in these high-performance converters is inextricably linked to device longevity. Following the well-known Coffin-Manson law, the device's junction temperature must remain below a particular threshold in order to meet reliability standards and avoid premature failures [160-162]. A finite-element based thermal simulation of an OBC has been undertaken with the goal of analyzing temperature values in a typical operation condition by studying heat propagation in the converter structure.

6.2 Thermal Management and Losses Computation

Thermal management is a critical issue in building a proper reliability model in power converters. Extraction of heat from (SMT, Surface-Mounted Technology) power devices in power converters is one of the most difficult issues. SMT are ideal for usage in power conversion products since they simplify the manufacturing process. Some considerations must be made in this framework because thermal concerns can be improved with new

packages, improved geometry design, and the usage of correct thermal vias beneath the footprint area. Another significant aspect of SMT devices is the attachment to the Printed Circuit Board (PCB), which is utilized to connect all of the components (both active and passive). PCB is the system's thermal bottleneck since it can withstand lower temperatures than power devices. Heat sinks or baseplates placed to the other side of the PCB dissipate the heat [163-164].

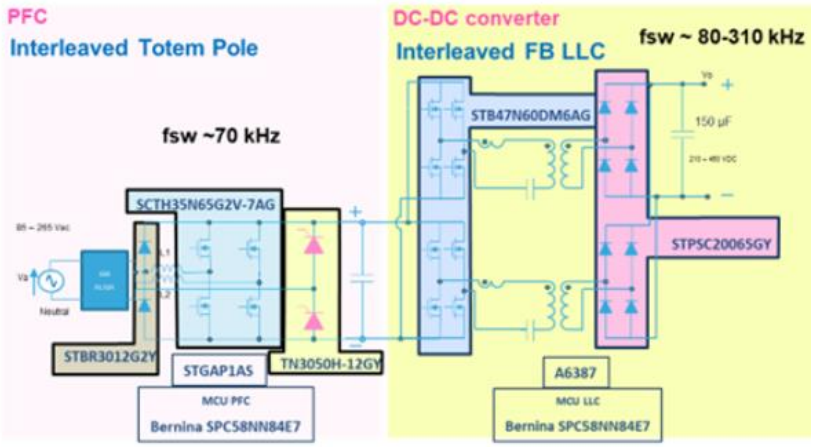


Fig. 6.1 Schematic diagram of the power converters

STDES-7kWOBC is the investigated OBC reference design (shown in Fig.6.1) that allows EV batteries to be charged either a household AC mains connection or a private/public outlet (AC charging station, levels 1 and 2). By utilizing forced air or liquid cooling, the underlying insulated metal substrate (IMS) on aluminum base plate offers very good heat dissipation. Of course, a converter has a large number of devices (diodes, thyristors, and MOSFETs), each of which creates a different power loss that must be evaluated using the right formulas before being put to the simulation as value in the heat source dies.

The power loss analysis excludes the two diodes STBR3012G2Y because they are inactive during normal operation as they are blocked when the voltage in the boost converter exceeds the bus voltage, resulting in no relevant power being dissipated; these are bypass diodes with an ultra-low power loss and can thus be ignored. The four SCTH35N65G2V-7AG silicon carbide Power MOSFETs are placed in an H2PAK-7 package and form the core of the interleaved totem pole; its low turn-on resistance (55 um) much help to reduce the conduction losses.

Switching, conduction, and driver losses all contribute to power loss. [165] publishes some estimates for the boost PFC converter architecture, which differs from the totem pole PFC discussed in this thesis.

In our case, a MOSFET replaces the diode, which functions as a rectifier for half a time. As a result, the conduction losses must be divided into two components:

$$P_{cond} = I_{DS(RMS)}^2 \cdot \left(R_{DS(on)} \cdot \alpha\right) + I_{RMS\_rect}^2 \cdot \left(R_{DS(on)} \cdot \alpha\right) \quad \text{Eq.6.1}$$

where the currents can be expresses as:

$$I_{RMS} = \frac{P_{OUT}}{2 \cdot V_{IN}} \cdot \sqrt{1 - \frac{8 \cdot \sqrt{2} \cdot V_{IN}}{3 \cdot \pi \cdot V_{OUT}}}$$

$$I_{RMS\_rect} = \frac{P_{OUT}}{2 \cdot V_{IN}} \cdot \sqrt{\frac{8 \cdot \sqrt{2} \cdot V_{IN}}{3 \cdot \pi \cdot V_{OUT}}} \quad \text{Eq.6.2}$$

Similarly, to adapt the model to the simulated topology, the switching and body diode losses must be slightly adjusted:

$$P_{SW} = V_{DS} \frac{f_{sw}}{2} \cdot t_{rise} \cdot \left(I_{DS(min)} + I_{QRR}\right)$$

$$P_{body\_diode} = 2V_{FD} \cdot f_{sw} \cdot t_{dead\_time} \cdot I_{Lavg} \quad \text{Eq.6.3}$$

Neglecting the driver contribution, which can be considered largely negligible, considering only one leg, and assuming P_{OUT}*=3680 W*, V_{IN}*=240 V*, V_{OUT}*=400 V*, the calculated $P_{MOSFET} \simeq$*14 W*.

The power losses values for each Silicon Controlled Rectifier (SCR) are calculated take advantage from the following formula:

$$P_{d_{SCR}} = \frac{V_{TO} I_{LINE(RMS)} \sqrt{2}}{\pi} + R_d \frac{I^2_{LINE(RMS)}}{2} \quad \text{Eq.6.4}$$

where I_{LINE}=32 A, V_{TO}=1.65 V, R_d=0.014 Ω; the power dissipated by the two TN3050H-12GY-TR will be P_{dSCR}=26.5 W.

To a first approximation, the only substantial power losses in the LLC section [166], which functions in soft-switching and at zero-voltage switching during the turn-on stage, are conduction losses. This statement may be reasonable because we are analyzing the converter at full load. In fact, with low current peak and frequency values, we are close to the resonance frequency in this case. As a result, switching losses are kept to a minimum. A Power MOSFET's RMS current can be written as:

$$I_{RMS\_MOS} = \frac{P_{IN} \cdot \pi}{V_{IN} \cdot 2\sqrt{2}} \quad \text{Eq. 6.5}$$

And the conduction losses are represented as:

$$P_{cond} = I^2_{RMS} \cdot R_{DS(on)} \cdot \alpha \quad \text{Eq. 6.6}$$

where the parameter α is set to 1.5. The calculated power loss for each STB47N60DM6AG is around 14 W.

The ultimate goal of the present study is to thermally replicate the global behavior of a car charger's active stages with an adequate heat sink capable of preventing problems and substantially reducing lifetime. There are two ways for running simulations like the one in this paper, which use two different types of approximations:

1. *A fixed-temperature heatsink:* The main boundary condition is that a fixed temperature is used for the layer all the way down the baseplate. This solution reflects an ideal scenario, which means that all the heat generated by the active components is drained practically instantly by an infinite heatsink, resulting in a negligible temperature rise. Because it is easy, this type of thermal simulation is one of the most commonly used [167]. Because it may simulate this state, i.e., a very favorable path for the heat created in the die, this technology is well-suited for cooling systems with very high heat exchange capacity.

2. *Heatsink with finite cooling system:* Different numerical methodologies can be used to indicate the fluid cooling system's capabilities. By specifying the heat exchange area, the equivalent heat transfer coefficient (htc) of the cooling system can be examined in a simulation. It is the face beneath the baseplate of the considered board in the simulated OBC. [168] retrieves the parameter htc, which is defined as the amount of heat carried by convection between a solid and a fluid.

$$Q_0 = h \cdot (T_{ext} - T) \qquad \text{Eq. 6.7}$$

Where Q_0 represent the transferred heat between fluid and solid, T_{ext} is the external temperature and T the one in the active site. It means that when the temperature rises steadily, with more heat convection between the module and the cooling system, the heat flux is concentrated beneath the active components and heat spreading is reduced. This action reduces the broad baseplate surface's benefit in spreading heat dissipation and raises the temperature between the junction and the casing. Depending on the technology used, the coefficient htc ranges from 10 W/m^2K for natural convection systems to around 10000 W/m^2K or more for liquid cooling systems [169].

6.3 Modular solution description

This Section describes the OBC structure that was mentioned in the introduction. The 7 kW AC-DC power converter module takes advantage of innovative SiC devices and enables for the parallelization of more MOSFETs in an interleaved stacked system capable of reaching up to 21 kW and being configured for mono and three phase inputs, as shown in Fig. 6.2.

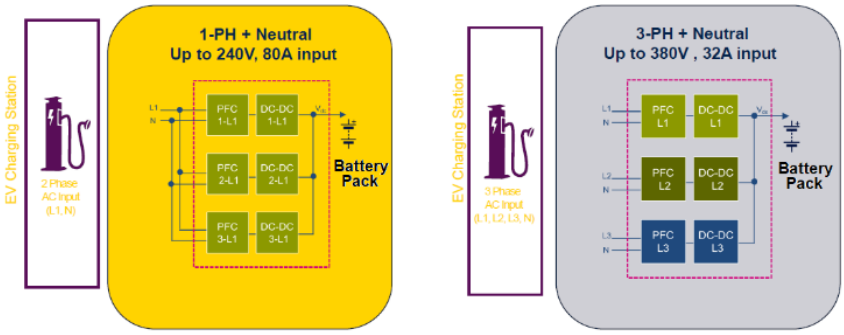


Fig. 6.2 Single and three phase configuration schemes

The proposed method aims to provide an AC-DC power converter that can be included into an electric car's OBC as well as a DC wall-box. In comparison to normal AC wall-boxes, the last alternative would be seen as a novel method for drastically lowering charging time.

As shown in Fig. 3, the reference design has two sections: an interleaved totem pole PFC with SiC MOSFETs and a dual galvanic isolated full bridge LLC DC-DC ZVS resonant converter based on MDmesh DM6 super-junction power MOSFETs.

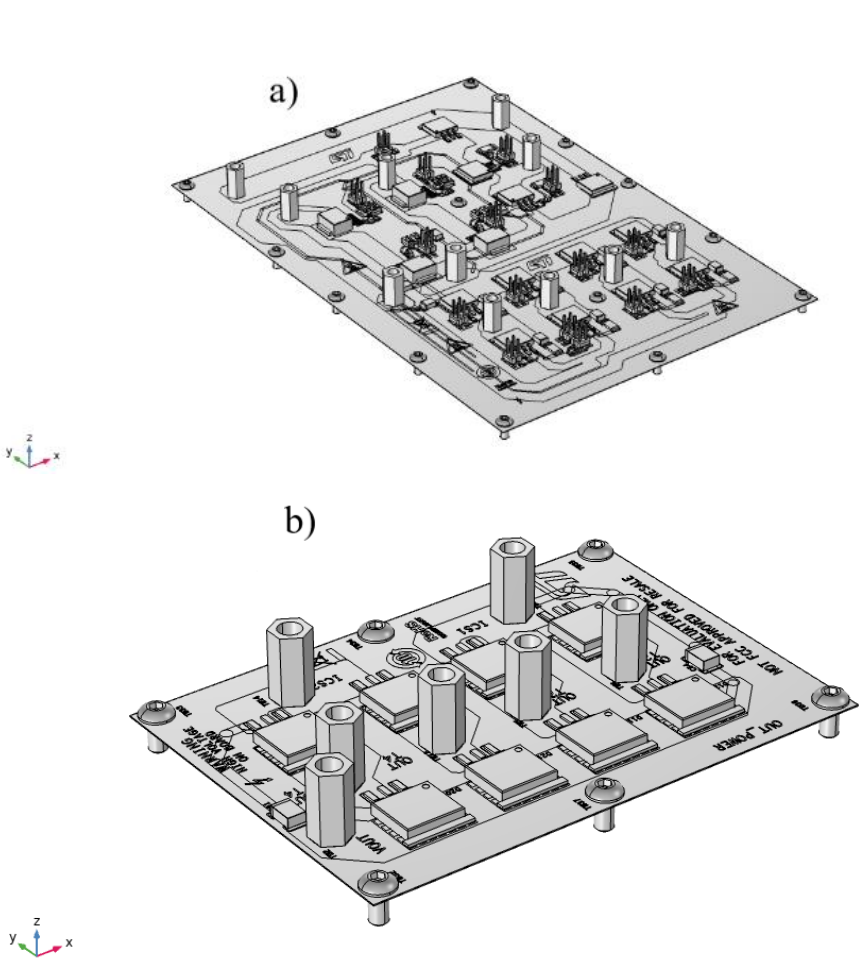


Fig. 6.3 Global geometry of a) PFC and LLC stages and b) output stage

The PFC section employs a number of signals, including sinusoidal mains voltage zero crossing signals, mains signals, current sensors for the first and second totem pole inductors, maximum current limit comparators, SiC driver signals, SCR driver signals, bus voltage, and PFC temperature sensing signals. In the DC-DC converter dual full bridge LLC section, the bus voltage galvanically isolated sensing signal, resonant current

of the resonant cells, output current and output voltage, LLC temperature, and MOSFET driving signals for the two full bridge LLCs are all employed.

The PFC section is an interleaved totem pole that uses 2 x 510 μH inductors and 2240 μF bulk capacitors. The switching frequency is 70 kHz. The high frequency legs use SiC MOSFETs (STB47N60DM6AG) and the low frequency leg is SCR–based (TN3050H-12GY-TR).

To prevent current spikes, this PFC is designed to run in continuous conduction mode (CCM), with two distinct current loops (type II or PID controllers), mains voltage feedforward, and PWM initiation at zero crossover. The switching frequency of the interleaved totem pole PFC is 70 kHz, but the switching frequency of the dual DC-DC LLC resonant converter ranges from 80 kHz to 310 kHz.

The output current balance management on the DC-DC LLC is different from the inductor current balance control on the interleaved totem pole. These procedures ensure that the current in the parallel connection stages is balanced.

The AC–DC totem pole PFC section converts an input voltage of 85 VAC to 265 VAC into 400 V. The maximum input current is 32 A at 50 Hz or 60 Hz.

The PFC works in CCM. With a dynamic resistance of 14 mΩ, the TN3050H-12GY-TR SCR thyristors implement inrush current. Two independent current loop regulators are used by PID or 2p2 controllers to regulate current. The SPC58NN84E7 MCU controller is used to implement these controls.

The second converter is the dual resonant DC–DC LLC based on super junction MOSFETs.

The output DC–DC voltage is in the range of 250 V_{DC} to 450 V_{DC}. Two independent constant current loops (CC) and one constant voltage loop (CV) plus current balancing are implemented on a second SPC58NN84E7 MCU controller.

The 7 kW AC–DC power module consists of the following blocks, that are showed in Fig.6.4:

- EMI Filter/front end rectifier.
- SiC interleaved totem pole PFC stage to ensure the optimal interfacing with the mains [19];
- DC\DC converter based on interleaved Full Bridge (FB)-LLC with SiC synchronous rectifier–box [20].

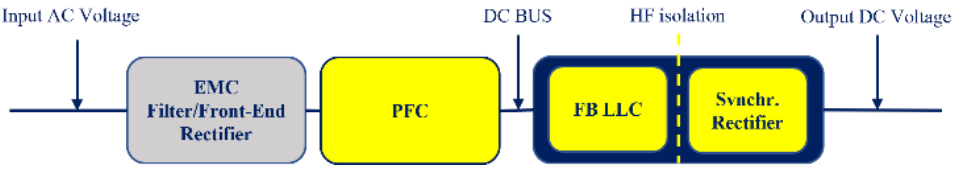


Fig. 6.4 block diagram of the DC–DC converter

The goal is to use interleaved solutions for the SiC PFC stage (totem pole) and the high voltage side of the DC-DC converter (FB LLC) to achieve the configuration flexibility required to provide the required power size (up to 21 kW by stacking three modules) and the AC mains interfacing via a 7 kW module, used alone or in parallel, to match mono phase (1 Phase+ N) and three phase (3 Phases + N) assembly modes. Figures 6.5 and 6.6 show the top and exploded views of the OBC, respectively.

Fig. 6.5 Top view of the OBC structure

6.4 Thermal simulation setup and results

It was run thermal simulations to predict the temperature inside the devices, with the goal of defining an appropriate thermal margin during operation and, eventually, building a proper lifetime reliability model to learn about the system's behavior and reliability under normal operating conditions. COMSOL Multiphysics, a cross-platform finite element method (FEM) analysis software that supports standard physics-based user interfaces and coupled systems of partial differential equations (PDEs), is used to run the simulations. PDEs can be translated into algebraic equations using the FEM approach, which the simulator can manage more easily.

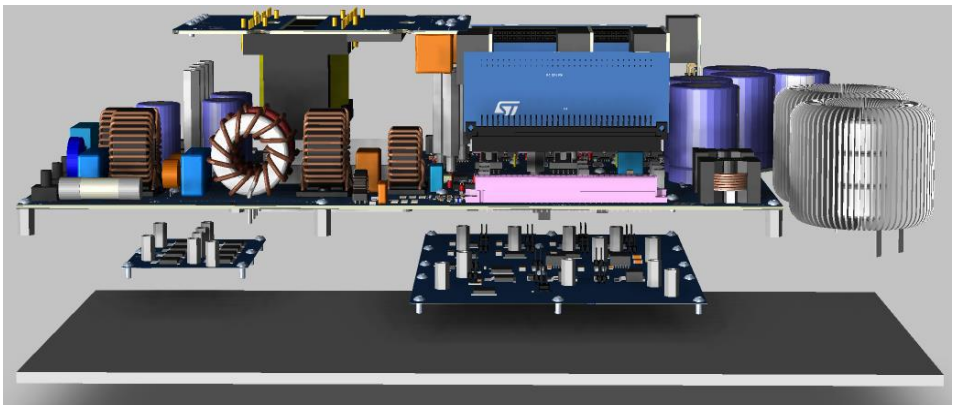


Fig. 6.6 Exploded view of the OBC structure

The overall system must be assessed, but in our simulation, the focus was on the thermal behavior of the PFC and DC-DC converters, which are without a doubt the most critical components. This module has a significant impact on the overall system's efficiency and longevity. Figure 7 depicts the investigated vehicle on-board charger, with the simulated elements highlighted.

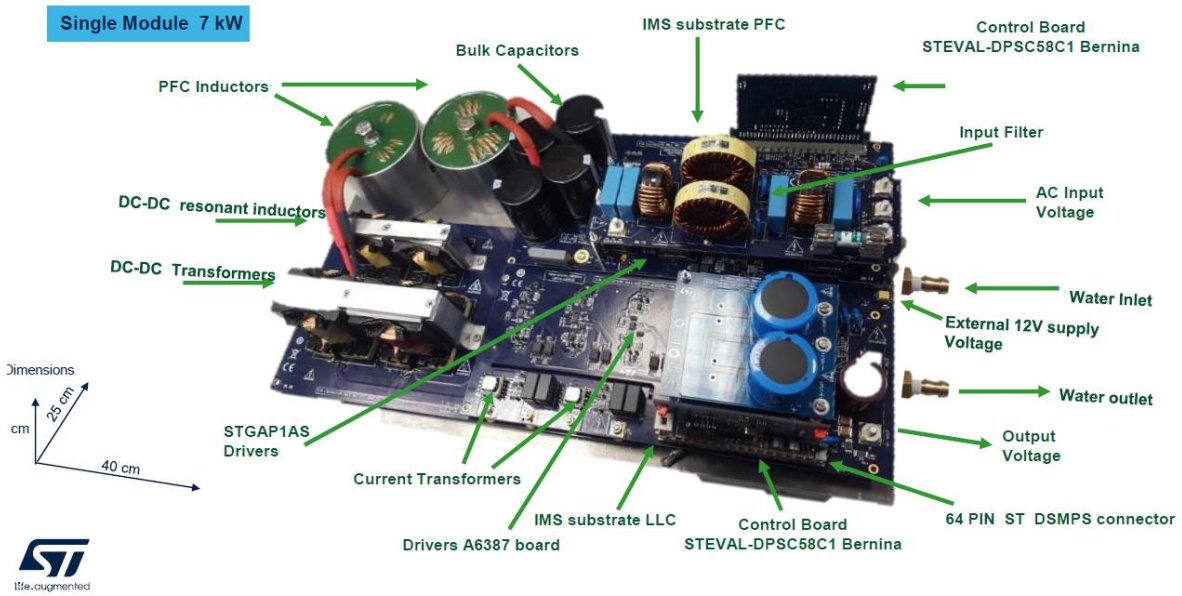


Fig. 6.7 Picture of the on–board charger. The red ellipses highlight the parts we focused for the thermal simulation (LLC and PFC stages).

The complex multilayered mechanical structure is updated as follow:

- An aluminum baseplate, which is connected to the external cooling system (420x200x6 mm);

- A thermal grease thin layer with the same area having a thickness of 180 μm, useful to improve thermal conductivity.
- Right up two IMSs, one for the PFC stage (203x139x1.5 mm) and the other for the LLC stage (91x65x1.5 mm), at a distance of 105 *mm* from each other.
- Both stages have on top a copper layer of 105 μm, which hosts all the active components (diodes, thyristors, and transistors), all dies have the real size, those are undisclosed information.
- The entire structure is incapsulated in the epoxy resin.
- The copper and epoxy resin of each device as the size of the package of the component.

An important job during the simulations is to provide a model in which the trade-off between approximations and computing times is acceptable. Three boundary conditions were used in this work: all active component dies function as heat sources. This condition was precisely applied by resizing the die dimensions and employing the complementary COMSOL functionalities "work plane" and "partition objects"; this procedure ensures the resolution of some mesh problems (which the reader can check immediately after) and the reduction of computation time.

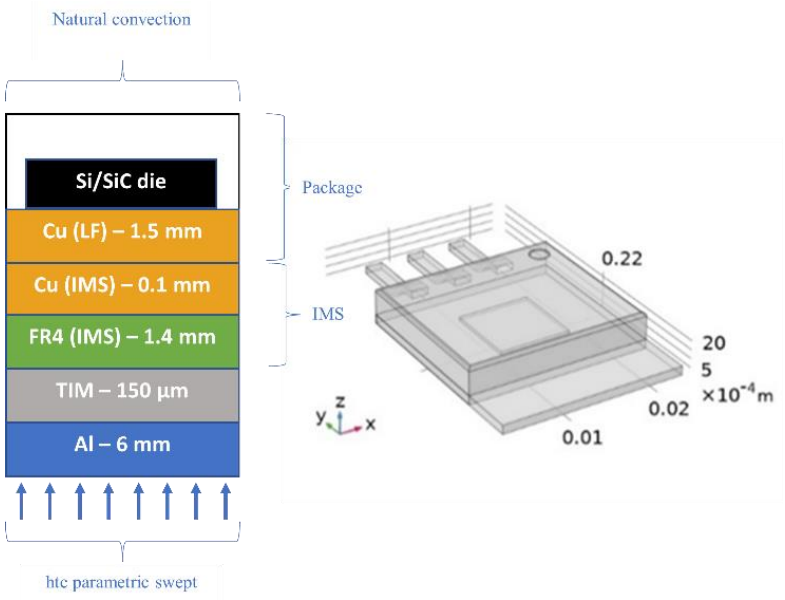


Fig. 6.8 (a) Details of the layers used to simulate the structure; (b) the model used to simulate the system (on the left) and a power device structure (on the right).

The second condition concerns the cooling system simulation. The bottom layer of the aluminum baseplate is used as a convective heat flux for this purpose; for the desired value, a parametric sweep is done according to (9), which gives us specifics about the appropriate heatsink to install. The final boundary condition is the heat flow in the

external package contour, which is useful to ensure the natural convective flux that each device must bear during normal operation (set at $htc=4\ W/m^2\ K$).

The realistic evaluation of power dissipated by the active component is a challenge, and constructing a complete model to analyze the losses is not the goal of this work. According to [23], the conductivity of various materials depends on the temperature. Silicon and copper have a significantly high thermal conductivity at higher temperatures, making them more susceptible to boundary conditions.

The mesh employed is a tricky issue due to the intricate geometry and varying thicknesses of the layers that range between hundreds of μm and hundreds of mm. This is undoubtedly one of the most significant issues that occurs when a FEM is employed to do this type of research. To address such challenges, an ad hoc technique is required: as previously stated, for each side of the die of each active component, a "work plane" was assigned, which, in addition to the COMSOL functionality "partition objects," allows for the division of each device into smaller domains. Every device's divided surface is meshed with "mapped" capability (and therefore further divided) with a one-millimeter maximum dimension of the elements. Each device can now be swept from top to bottom. This procedure must be repeated for each different component. The IMS layers and corresponding copper films were then covered with a "non-structured quadrilateral" mesh. Following that, a swept is executed from top to bottom, till the rear side of the baseplate is reached. It is now feasible to connect the baseplate, thermal grease, and IMS layers, sweating from top to bottom.

As mentioned before, a parametric swept for various htc values was performed.

It's obvious that the thermal jump is more evident for lower values of htc, while starting from $htc=1000\ W/m^2\ K$ the resulting thermal gradient ($\Delta T = 20{,}44\ K$) start converging to a constant value, in fact for $htc=10000\ W/m^2\ K$ and $htc=100000\ W/m^2\ K$ the thermal jump is respectively of 18,46 K and 18,33 K. For simplicity just the image relative to the case with $htc=10000\ W/m^2\ K$ is reported (Fig.9.).

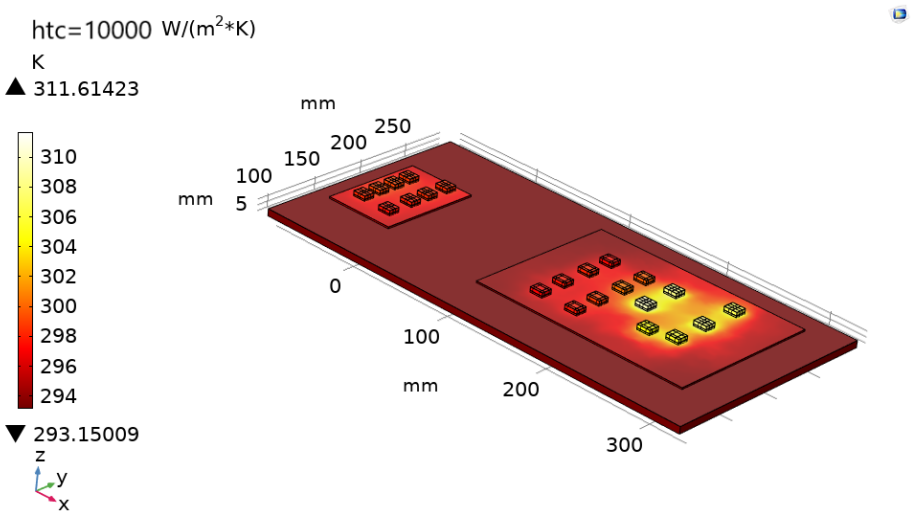


Fig. 6.9 The obtained thermal jump for *htc=10000 W/m² K* parametric swept, in which the maximum is located on the SiC Power MOSFETs.

The little temperature difference in comparison to the large htc difference suggests that the PFC and LLC stages under consideration have optimal thermal performance. The thermal gradient is evaluated for htc values of 1, 2, 3, 4, 5, 6, 7, 8, 9, 10, 100, 1000, 10000, and 100000 $W/m^2 \cdot K$. To better clarify the curve of the Tmax-Text as a function of the heat transfer coefficient (as shown in Fig.11), we felt it acceptable to investigate in greater depth the range from *htc=1 W/m² K* to *htc=10 W/m² K*, and therefore we opted to proceed in unit steps in this range.

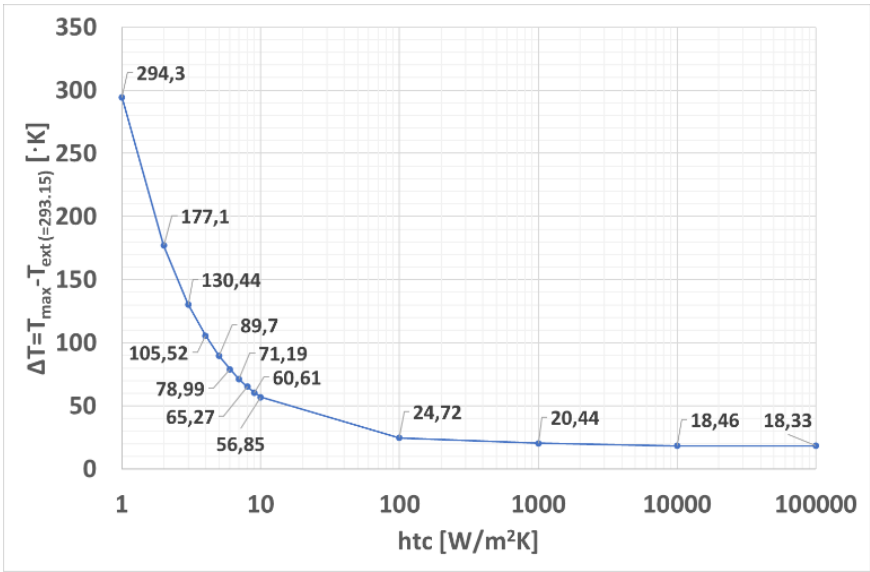


Fig. 6.10 Curve of the T_{max}–T_{ext} as a function of the heat transfer coefficient, in which a logarithmic scale for x-axes is used in order to get a better detailed curve.

The parametrization computation time is 1 hour, 11 minutes, and 10 seconds to solve 1382337 degrees of freedom (df), with 305 s spent for each simulation for the provided values.

The curve describing the baseplate thermal jump versus the htc coefficient allows to find a cooling strategy suitable for different scenarios and to design the cooling system focusing on the maximum allowed temperature of the baseplate which in turn defines the lifetime and the reliability of the converter at least from the thermal point of view.

In this frame, it can be observed that even with passive dissipation systems, i.e. HTC ranging between 100 and 1000W/m^{2}K, the thermal jump on the power devices package at full power is about 25°C. This means that the power dissipated by the devices is extremely low, resulting in particularly high conversion efficiency. Furthermore, this represents a useful aspect from an application standpoint because the heat sink was not equipped with forced heat dissipation systems: the absence of moving mechanical parts, such as fans or hydraulic cooling circuits, greatly simplifies the integration of the inverter into more complex systems and ensures its reliability.

Conclusions

The analysis shows that for low htc values, the temperature rises very quickly, but values over 1000W/m^{2}K, result in the temperature convergence to an essentially constant value, suggesting that the assembly has optimal thermal performance, ensuring good reliability and scalability. Furthermore, it is fully compatible with automotive technology and may be installed on board. The proposed solution only applies to the active components of the system; of course, the thermal contribution of the passive components should be investigated afterwards, with special emphasis paid to the inductors, which are, without a doubt, another key component of the system. The deployment of those passive components, as well as experimental research to validate the suggested thermal model, are future development goals.

Conclusions

Nowadays wide bandgap semiconductor takes a crucial role in power and high frequency electronic technology hence it is of paramount importance to solve the several issues that reduce yield products and reliability.

The work thesis focuses on two of the main aspects of SiC power devices:

- The reduction of substrate defectivity, which has a high killer rate. Screening inspections after substrate and epitaxy growth is good enough to detect all the kind of defectivity but the real screening take place at the end of the active area process flow. At these points it's possible to have evidence of reject dice due to current leakage, shorts, anomalous BV_{DSS}
- Thermal management reliability: This study took place once the devices (in the present work an inverter was studied) is packed. Of course, it's an industry priority assure high performances and lifetime in harsh environment with high thermal excursions.

About the first point, it's not possible avoid substrate defectivity, so it was proposed a technique able to reduce it: Wafer Level Annealing (WLA). This process results quite effective and able to help recombination after the crystal growth, more specifically can "transform" BPD in a kind of defectivity which is not killer. As you can see in Fig. 7.1, after the WLA implementation on process flow, show a drastic reduce of defectivity and give a huge improvement in terms of yield.

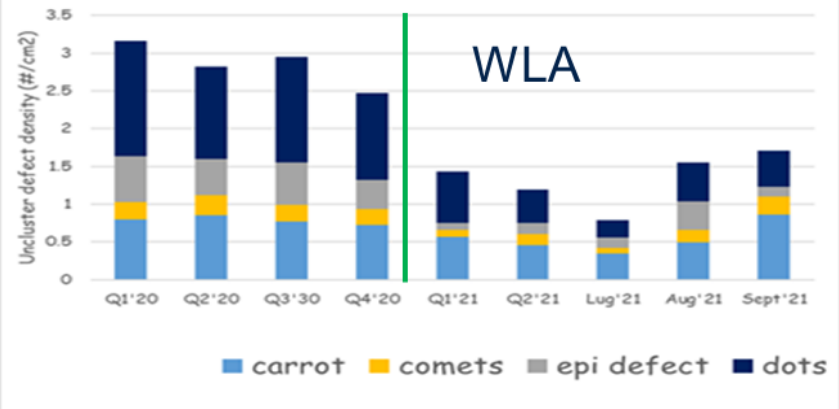


Fig. 7.1 Defectivity improvement after WLA implementation in process flow

However, it has a problem to face: during the WLA high temperature are reached (1150 °C is the qualified process, the study started at 1600 °C). In this framework, covalent bond can be broken, and evaporation of silicon give the possibility to carbon particles to graphitized. This issue was studied using AFM, RAMAN and photoluminescence. The study led to an optimized process at 1150 °C and highlight that carbon contamination can be introduced by the equipment tool.

About the second point, it was evaluated the thermal behavior of the PFC and LLC stages of a unique on-board charger for automotive applications, which were mounted on an IMS board. A FEM simulation was used to achieve this goal. First, the innovative converter has been described in detail, with the main components thoroughly explained. The simulation includes Si and SiC MOSFETs, SiC Shottky diodes, and thyristors as active components. The simulation setup and methodology are also described in the study. We employed the correct topology for the geometry of the PFC and LLC stages, as well as three boundary conditions, to estimate the maximum temperature reached by the semiconductor dies.

In our simulation, all dies serve as heat sources, natural convection is applied to the exterior active component boundary ($htc = 4\ W/m^2 \cdot K.$), and the bottom of the baseplate is used to simulate the cooling system. A parametric sweep for different values is also performed. The findings show a noticeable temperature rise for low htc values but starting at $htc = 1000\ W/m^2 \cdot K.$, the temperature begins to converge to an essentially constant value, indicating that the assembly has ideal thermal performance, ensuring good reliability and scalability.

Furthermore, it is completely compatible with automobile technology and is suitable for installation on board. The provided solution just applies to the system's active components; of course, the thermal contribution of the passive components should be examined afterwards, with special attention placed on the inductors, which are, without a doubt, another critical element of the system. Future development objectives include the deployment of those passive components, as well as experimental studies to validate the proposed thermal model.

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